Pseudomorphic InP/InGaAs Heterojunction Bipolar Transistors (PHBTs) Experimentally Demonstrating f_T = 765 GHz at 25°C Increasing to f_T = 845 GHz at -55°C

William Snodgrass, Walid Hafez[*], Nathan Harff[**], and Milton Feng

Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign,
208 North Wright Street, Urbana, IL 61801 Tel: (217)244-3662, Email: mfeng@uiuc.edu
[*]now with Intel Corporation, Portland, Oregon. [**]Mayo Foundation SPPDG group, Rochester, Minnesota.

Abstract

Pseudomorphic InP HBTs (PHBTs) with a vertically scaled design implementing a 12.5 nm base and 55 nm collector exhibit record current gain cutoff frequency performance of f_T = 765 GHz when measured at 25°C. When cooled to -55°C, f_T improves more than 10% to f_T = 845 GHz due to enhanced electron transport and reduced parasitic charging delays as determined by small signal equivalent circuit parameter extraction. Peak performance current density J_C = 18.7 mA/µm² and BV_{CEO} = 1.65 V.

Introduction

InP based heterojunction bipolar transistors (HBTs) dominate highest-speed transistor operation with cutoff frequencies exceeding 500 GHz first reported for single heterojunction transistors (SHBTs) in 2004 (1). Type I InGaAs/InP double heterojunction transistors (DHBTs) and type II GaAsSb/InP DHBTs broke this mark in 2006 (2, 3). As illustrated in Fig. 1, InP HBTs maintain a breakdown voltage advantage over SiGe HBTs and InP HEMT devices as the structures of each are scaled to achieve higher performance figures. The high-frequency performance of type II DHBT designs is currently limited by low electron velocities in the GaAsSb base region. Type I DHBTs must incorporate a narrow bandgap material at the base-collector interface to reduce the current blocking discontinuity of the type I base–collector junction. Type I designs thus possess a limit to vertical scaling that results in breakdown voltages approaching those of the SHBT for scaled designs with f_T greater than 500 GHz. InP pseudomorphic HEMTs (pHEMTs) have demonstrated f_T = 562 GHz (4), however the pHEMT transistor must be biased very near breakdown to achieve such speeds, suggesting that scalability of these devices for higher frequencies is limited. Recently, we have designed SHBTs utilizing pseudomorphic grading of the base and collector regions. These newly developed pseudomorphic HBTs (PHBTs) are aligned with the breakdown voltage versus f_T trend of earlier SHBT devices presented in Fig. 1, which predicts breakdown voltages exceeding 1 V as f_T approaches 1 THz.

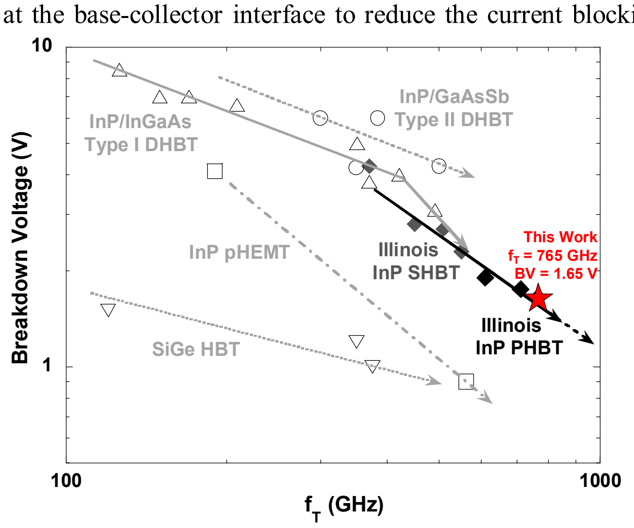

Fig. 1: Breakdown voltage (BV_{CEO}) versus f_T trends of various InP HBT devices compared to InP pHEMT and SiGe HBT reports.

Current Density Scaling Limitations

When HBT structures are vertically scaled to reduce transport delays, parasitic capacitance is increased. Collector current density must also increase to offset this capacitance, or else the benefit of transit delay reductions will be lost to increased charging delays. Plotting the inverse semi-logarithmic relationship of the cutoff frequency of several generations of SHBTs and DHBTs versus current density as presented in Fig. 2, it becomes clear that achieving THz cutoff frequencies using traditional design and scaling methodologies will require unrealistic current densities exceeding 300 mA/µm^2. Our PHBT devices, which benefit from an accelerated dependence of cutoff frequency on current density, present a potential solution to this critical issue. The PHBT trend presented in Fig. 2 indicates that THz cutoff frequencies may be obtained at a current density of only 28 mA/µm^2 using fully pseudomorphic epitaxial designs. We have previously reported record speed performance of PHBTs with f_T = 604 GHz at a collector current density J_C = 15.0 mA/µm^2 and f_T = 710 GHz with J_C = 17.9 mA/µm^2 (5, 6). Room temperature device performance reported in this work continues to follow the same trend, with f_T = 765 GHz achieved when operating at J_C = 18.7 mA/ µm^2. When cooled, electron transport is enhanced further and the cutoff frequency dependence shifts to lower current densities; at -55°C f_T = 845 GHz is achieved at the same J_C = 18.7 mA/µm^2.

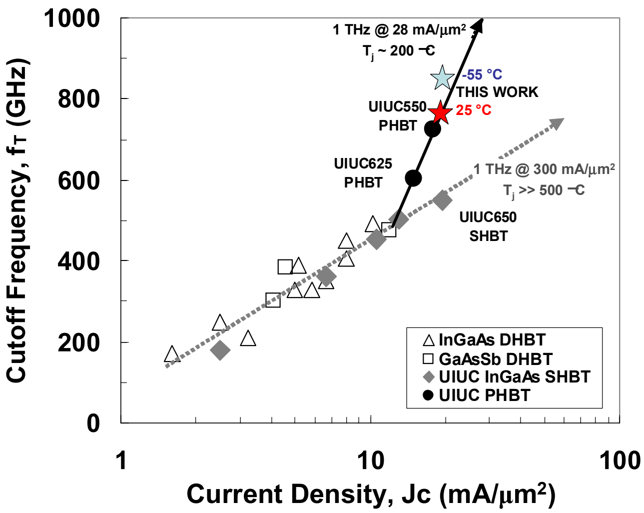

Fig. 2: Current gain cutoff frequency f_T versus collector current density J_C trend for InP based DHBTs and SHBTs (light). Accelerated trend for InP PHBT projecting 1 THz f_T at 28 mA/μm^2 (dark).

PHBT with Record Transistor Performance

Prior to this work, delay term extractions from 55 nm collector PHBT devices having f_T > 700 GHz revealed that parasitic charging delays exceeded electron transit delays. This was not the case with previous UIUC HBTs, which have collector thicknesses ≥ 62.5 nm and are dominated by transit delay. To achieve maximum benefit from the enhanced electron transport of the vertically scaled pseudomorphic structure, extrinsic capacitances were minimized by aggressive lateral scaling of the base finger mesa that dictates the base-collector junction area of the device. Two scanning electron micrographs that illustrate the reduction in extrinsic base-collector junction capacitance are shown in Fig. 3. This reduction in base-collector junction area translates directly to higher f_T via reduced collector charging delays.

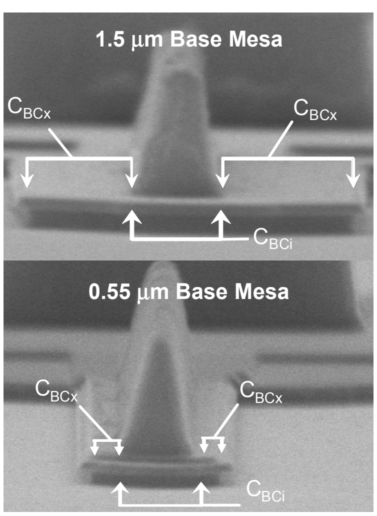

Fig. 3: Scanning electron microscope images of original base-collector mesa (top) and improved design (bottom) with reduced extrinsic base-collector capacitance.

The minimum base contact area required to achieve ohmic contact limits the extent of such scaling, and currently requires approximately 0.1 μm base contact width on each side of the base mesa. A laterally scaled 55 nm collector PHBT device with emitter area A_E = 0.32 x 6 μm^2 and 0.55 μm base mesa width achieves f_T = 765 GHz when measured at 25°C, and f_T = 845 GHz when the device is cooled to -55°C. Simultaneous f_{MAX} improves from 227 GHz to 263 GHz. Fig 4 displays the 25°C common emitter output characteristics of the transistor. The knee voltage is 0.75 V at high current densities and the collector-emitter breakdown voltage, determined at J_C = 10 μA/μm^2 when I_B = 0, is 1.65V. The DC current gain β = 105. RF measurements taken at 25°C and -55°C are detailed in Fig. 5, which presents h_{21} and U versus frequency for the peak performance bias point with -20 dB/decade lines illustrating the determination of f_T and f_{MAX}.

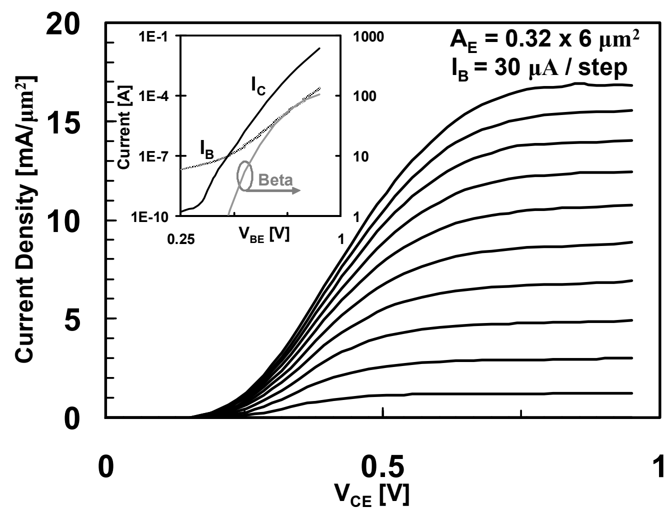

Fig. 4: Common emitter curves at 25°C presented in terms of emitter current density and Gummel I-V curves (inset) for 0.32 x 6 μm^2 PHBT.

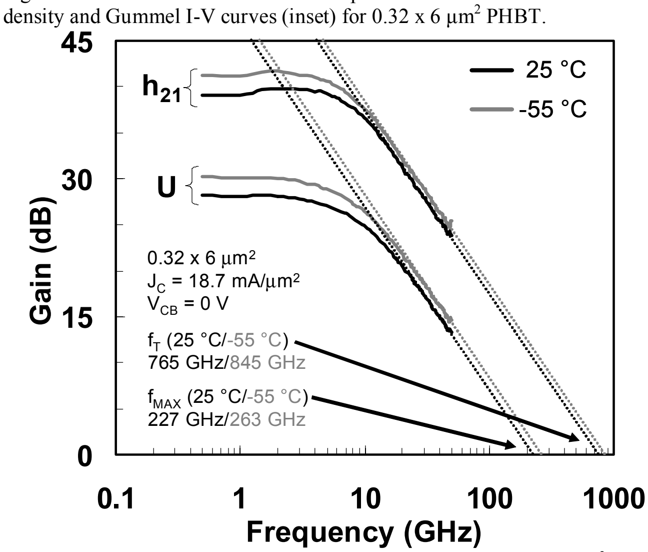

Fig. 5: -20dB/decade extrapolations of h_{21} and U for a 0.32 x 6 μm^2 PHBT indicating peak f_T = 765 GHz with an associated f_{MAX} = 227 GHz when measured at 25°C. Peak f_T improves to 845 GHz with associated f_{MAX} = 263 GHz when measured at -55°C.

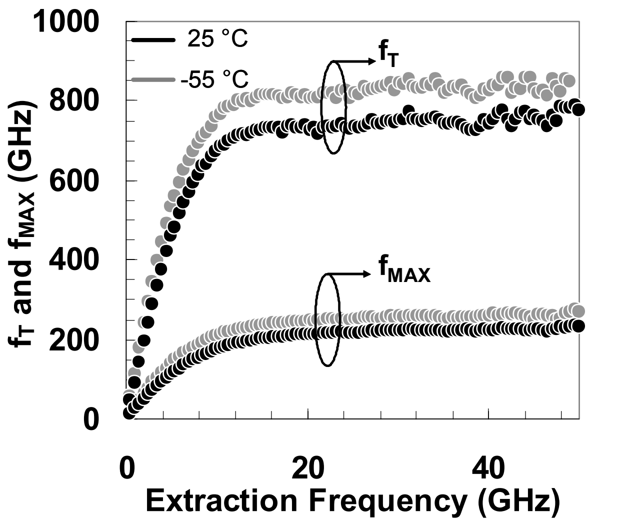

Fig. 6: Extrapolated cutoff frequency versus frequency at which extrapolation is taken for both 25°C and -55°C measurements.

Fig. 6 looks at the frequency dependence of the f_T and f_{MAX} extrapolations. The extrapolations appear flat beyond 30 GHz, indicating constant -20 dB/decade decrease in gain with frequency. Fig. 7 plots the forward delay $\tau_{ec} = 1/(2\pi f_T)$ versus $1/I_C$ at 25°C and -55°C. Extrapolating to $1/I_C = 0$ eliminates the temperature dependent dynamic emitter resistance RC charging delay term from the total delay. The remaining terms, consisting of base-collector carrier transit and base-collector junction RC charging, decrease from 171 fs at 25°C to 152 fs at -55°C. Small-signal parameter extractions detail how the transistor changes when cooled; the small-signal equivalent circuits determined from high frequency measurements taken at each temperature are presented in Fig. 8. The individual emitter charging, collector charging, base transit, and collector transit delay values for an earlier 65 nm UIUC SHBT device and the current 55 nm collector PHBT device are compared in Fig. 9. While device current density is the same for the 65 nm SHBT

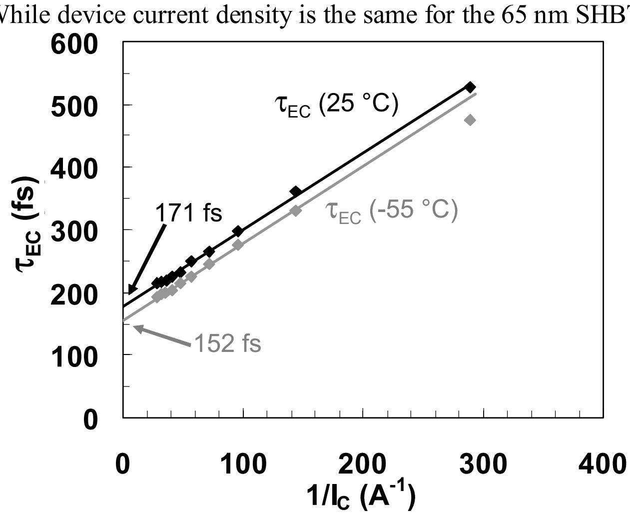

Fig. 7: Transistor forward delay versus inverse collector current at 25°C and -55°C. Extrapolating to 1/Ic equals zero eliminates the temperature dependent dynamic emitter resistance revealing enhanced electron transport.

and 55 nm PHBT (see Fig. 2), each delay term has been reduced by 15% - 40% in the PHBT through material design and process optimization. RC charging times are reduced by grading the emitter contact layer from lattice-matched $In_{0.53}Ga_{0.47}As$ to InAs for lower emitter contact resistance, while lateral scaling offsets the increased junction capacitance per unit area that arises from vertical scaling. Vertical scaling of base and collector layers lowers base and collector transit delay terms and the pseudomorphic collector design enhances electron transport through that region – further reducing the collector delay. The PHBT performance improvement at low temperatures is attributed equally to reduced base and collector transit delay as well as smaller collector charging delay. Average electron velocity through the collector increases by 15% from 4.2 x 10^7 cm/s at 25°C to 4.8 x 10^7 cm/s at -55°C, lowering the collector transit delay from 65 fs to 57 fs. Reduced dynamic emitter resistance r_e, extrinsic emitter resistance R_{EE}, and base-collector junction capacitance C_{BC} drop the collector charging time from 79 fs at 25°C to 68 fs at -55°C.

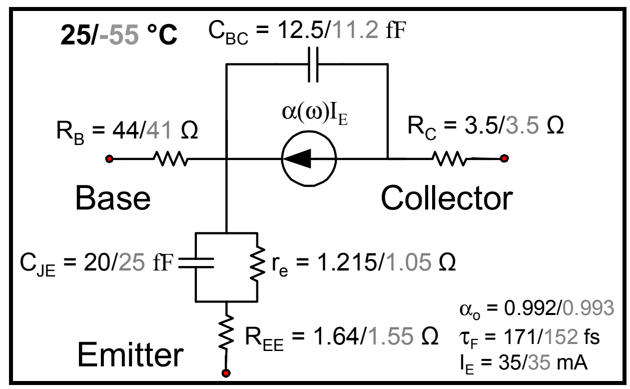

Fig. 8: Small-signal equivalent circuit model. Parameter values extracted at peak f_T bias point for 25°C and -55°C measurements.

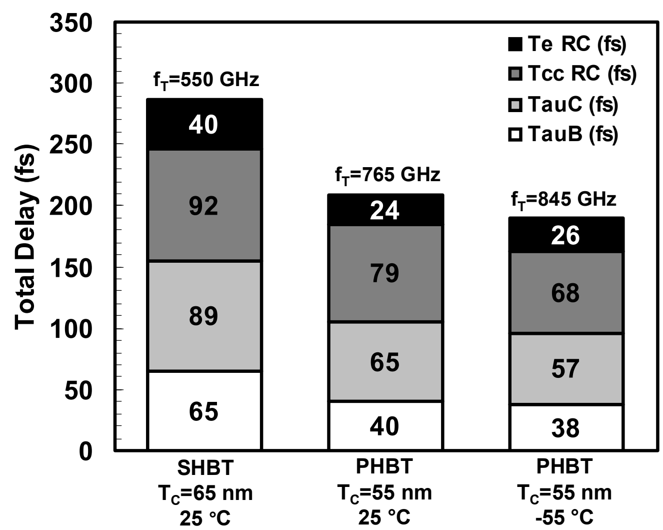

Fig. 9: Individual delay term values for 65nm collector SHBT (left), 55nm collector PHBT at 25°C (center), and 55nm collector PHBT at -55°C (right). T_e is the emitter RC charging delay, T_{cc} is the collector RC charging delay, and Tau C/Tau B are the collector/base transit delays.

RF Measurement Verification

UIUC RF measurements were taken from DC to 50 GHz utilizing an HP8510C vector network analyzer (VNA). Off-wafer short-open-load-through (SOLT) calibrations were used and de-embedding was achieved by subtracting on-wafer open and short standards. UIUC RF measurements of a 55 nm collector PHBT with dimensions 0.32 x 4 µm^2 and f_T > 700GHz were compared to those taken by the Mayo foundation SPPDG group. The Mayo measurements were taken using an Anritsu VNA and both SOLT and line-reflect-match (LRM) calibration methods. Excellent agreement between UIUC and Mayo measurements was observed as shown in Fig. 10. The f_T values extrapolated from these high frequency measurements can be verified by f_T calculations based on lower frequency measurements (7). In Fig. 10, an ideal transfer function based on the measured low frequency current gain of the device and an arbitrary f_T value (chosen for best fit) is plotted with the measured data for comparison. The function fits both measured data sets quite well over the entire frequency range when f_T = 710 GHz is chosen as the function parameter. Ref. (7) also suggests a method for the determination of f_T that is taken from the low frequency slope of the imaginary component of the reciprocal of the current gain versus frequency. Fig. 11 illustrates this calculation for the device reported in this work using the measured current gain data at 25°C and at -55°C. The f_T values obtained using this method are within 1.5% of those obtained by -20 dB/decade extrapolation from the high frequency gain.

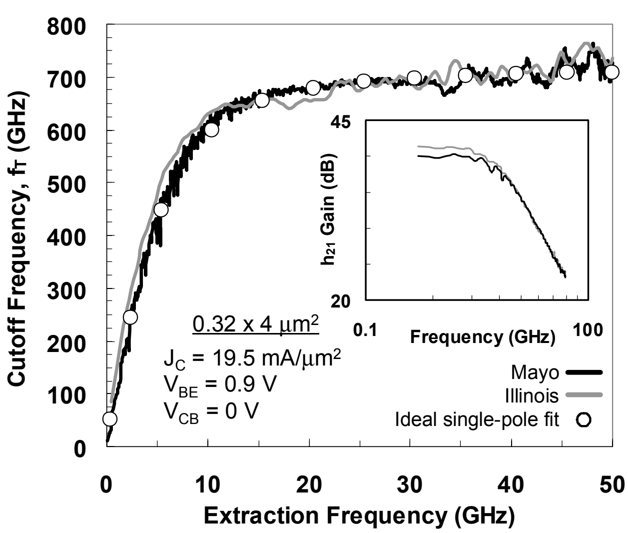

Fig. 10: Extrapolated cutoff frequency versus frequency at which extrapolation is taken for 0.32 x 4 µm^2 PHBT device with peak f_T > 700GHz. University of Illinois measurements are compared to those taken at the Mayo foundation and to an ideal 710 GHz f_T single-pole transfer function.

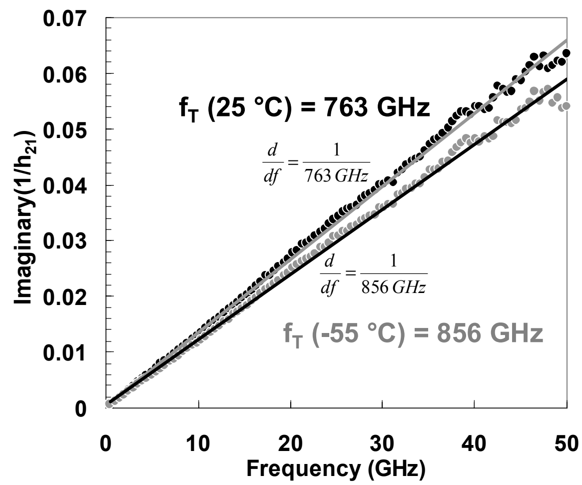

Fig. 11: Alternative determination of f_T using the slope of the imaginary component of the reciprocal of the current gain versus frequency, taken from the low frequency portion of the measurement range.

Conclusion

Combined vertical and lateral scaling of pseudomorphic InP-InGaAs HBTs has delivered record current gain cutoff frequencies, resulting in an f_T vs. current density trend that projects attainable THz performance. f_T improves by more than 10% at -55°C due to enhanced electron transport and reduced collector charging delays. Further improvement will require a balanced approach designed to reduce both transit and charging delays as the charging delays become dominant in aggressively scaled device structures.

Acknowledgements

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