18-26 GHz Low-Noise Amplifiers Using 130- and 90-nm Bulk CMOS Technologies

Shih-Chieh Shin, Szu-Fan Lai, Kun-You Lin, Ming-Da Tsai, Huei Wang, Chih-Sheng Chang*, and Yung-Chih Tsai*

Dept. of Electrical Engineering and Graduate Institute of Communication Engineering, National Taiwan University, Taipei, 106, Taiwan, R.O.C.

*Taiwan Semiconductor Manufacturing Company, Hsinchu City, 300, Taiwan, R.O.C.

Abstract **— Two 18-26 GHz CMOS low-noise amplifiers using 130- and 90-nm bulk CMOS technologies are described in this paper. The thin-film microstrip (TFMS) LNA using 130-nm CMOS process demonstrates a peak gain of 12.9 dB at 21 GHz with 3-dB bandwidth of 18.6 to 26.3 GHz and a noise figure (NF) of better than 5.4 dB between 20 and 26 GHz. The coplanar waveguide (CPW) amplifier fabricated by 90-nm CMOS process presents a peak gain of 16.2 dB with a 3-dB bandwidth of 18 to 26 GHz, and a NF of better than 4 dB from 18 to 26 GHz.**

Index Terms **— CMOS, low-noise amplifier, thin-film microstrip line, coplanar waveguide.**

I. INTRODUCTION

The rapidly growing demand for larger bandwidth motivates RF circuits to move toward higher frequencies. At frequencies above 20 GHz, GaAs-based HEMT and HBT MMICs occupied most of the applications. Recent works have illustrated the rapid development of CMOS devices to have the potential of building RF circuits at frequencies above 20 GHz. Although LNAs using SOI CMOS process demonstrated excellent performances [1], the standard bulk CMOS process is still attractive because of cost consideration. There were some reports of bulk CMOS LNAs designed for frequencies above 20 GHz, and most of them were designed using the lumped elements [2]-[3]. Several high-frequency CMOS amplifiers were designed using transmission lines to reduce the lossy substrate effect [4]-[7]. A 20- and a 40-GHz TFMS amplifiers fabricated by 90-nm CMOS technology were reported with good agreement between the simulated and measured results [4]. A 0.18-μm CMOS distributed amplifier designed using TFMS demonstrates a 4-dB gain and a 39-GHz bandwidth [5]. A 27-GHz TFMS tuned amplifier consists of three-stage cascode cells demonstrated 17-dB gain [6]. By adopting coplanar waveguide, a 60-GHz LNA cascaded by 3-stage cascode cells was presented [7]. It is observed that the CMOS circuits using either TFMS or CPW demonstrated good performance in high frequency range.

In this paper, we present a TFMS and a CPW LNAs fabricated using TSMC 130- and 90-nm bulk CMOS technologies, respectively. The TFMS amplifier was implemented with a very compact chip size since the thin-film spiral inductors can be utilized in this design. The CPW LNA fabricated by 90-nm technology demonstrates the better gain and noise performances. Table I summarizes the performances of the previously reported LNAs designed for frequencies around 20 GHz. Both of these amplifiers present the comparable gain of GaAs-based pHEMT LNA [8], with slightly higher noise performance for our 90-nm CPW CMOS design.

II. 90- AND 130-NM CMOS CHARACTERISTICS AND PROCESSES

The TFMS and CPW amplifiers are fabricated by 130-nm one-poly-eight-metal (1P8M) and 90-nm one-poly-nine-metal (1P9M) processes, respectively. The 130-nm process has an f_T of 85 GHz and an f_{max} of 90 GHz while the 90-nm process demonstrates an f_T of 160 GHz and an f_{max} of 142 GHz. Both of these two processes provide the top metallization of 2-μm thickness for low loss interconnection. MIM capacitors with 1- and 1.5-fF/μm^2 unit capacitance are also provided in 130- and 90-nm processes, respectively.

III. THIN-FILM MICROSTRIP LINE AND COPLANAR WAVEGUIDE IN CMOS PROCESS

Figure 1 shows the structures of the TFMS and CPW. The TFMS consists of the top metal (M8) as the signal strip and bottom metal (M1) as ground plane in the 130-nm CMOS process. The TFMS has the advantage of the ground plane shielding to isolate the conductive substrate. The matching elements of transmission lines can be replaced by thin-film spiral inductors or meandering lines in a very small area to reduce the circuit size. However,

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TABLE I
COMPARISON WITH PREVIOUSLY REPORTED LNAS FOR FREQUENCIES AROUND 20 GHZ.

Process	Bandwidth (GHz)	Gain (dB)	NF (dB)	Chip Size (mm^2)	P_{DC} (mW)	Supply Voltage (V)	Topology*	Ref.
0.18-μm CMOS	-	15	6 (22 GHz)	0.05#	24	1.5	3 stages, CGRF+CS+CS	[2]
0.18-μm CMOS	22 ~ 25	12.86	5.6 ~ 7 (23 ~ 24 GHz)	0.735	54	1.8	3 stages, CS+CS+CS	[3]
0.18-μm CMOS	23 ~ 28	8.9	6.9 ~ 8 (24 ~ 26 GHz)	0.735	54	1.8	3 stages, CS+CS+CS	[3]
90-nm CMOS	17 ~ 28	6	5 ~ 7 (17 ~ 20 GHz)	0.56	10	1.5	1 stage, CS, TFMS	[4]
0.15-μm InGaP/InGaAs HEMT	23 ~ 30	14.5	1.6 ~ 1.9 (19 ~ 33 GHz)	0.9	37.5	2.5	2 stages, CS+CS	[8]
130-nm CMOS	18.6 ~ 26.3	12.9	4.4 ~ 5.4 (20 ~ 26 GHz)	0.3	16.8	1.2	2 stages, CS+CS, TFMS	This Work
90-nm CMOS	18 ~ 26	16.2	2.5 ~ 4 (18 ~ 26 GHz)	0.8	26.4	1.2	2 stages, CS+CS, CPW	This Work

* CS: common source, CGRF: common gate resistive feedthrough.
\# : Test pads are not included.

the characteristic impedance of the TFMS is dominated by the signal strip width, high-impedance lines are difficult to be implemented due to the thin SiO_2 layer of 5.5 μm.

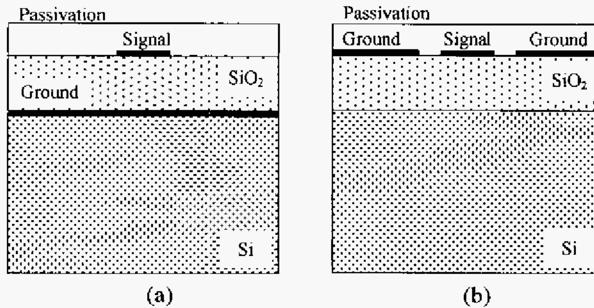

Fig. 1. The structures of the (a) TFMS, and (b) CPW on bulk CMOS process.

CPW is constructed by one signal strip and two ground metals on the same plane as shown in Fig. 1(b), and the signal and ground metals are implemented by the top metal. The characteristic impedance of the CPW is defined by the signal metal width and the gap size between signal and ground metal, thus it is more flexible to realize different impedances of CPWs. To suppress the unwanted odd-mode signal, the two ground planes of CPW should be forced to be equal potential. It is easy to implement by using the second metal to connect the two ground planes in CMOS process. The conductive substrate effect is reduced by using CPW, however it is not fully removed. Thus the substrate effect of CPW still needs to be considered. The TFMS can be meandered in very compact size, but not for CPW because CPW needs the well-defined ground planes.

IV. CMOS LNA USING TFMS

This amplifier fabricated by 130-nm 1P8M CMOS process is a two-stage single-ended design. The transistors in each stage are 18 fingers with a total gate periphery of 36 μm. Figure 2 shows the schematic, and the corresponding chip photo is shown in Fig. 3. The matching networks consist of series and shunt inductors to transform the impedance to 50 Ω. In order to minimize the circuit size, the thin-film spiral inductors are used as the matching elements. The source inductors implemented by the transmission lines are utilized in both stages for stability concern. All of the passive elements include thin-film spiral inductors, capacitors and transmission lines are simulated using the EM simulator Sonnet. The chip size is 0.77 x 0.4 mm^2.

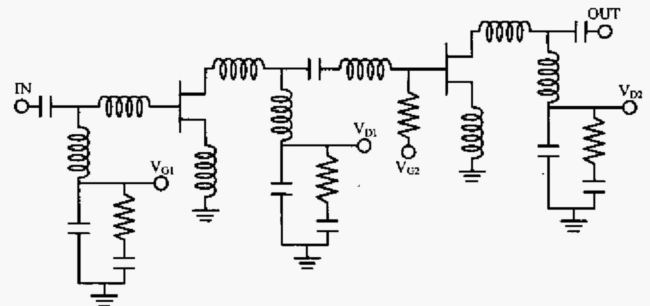

Fig. 2. Schematic of the TFMS LNA.

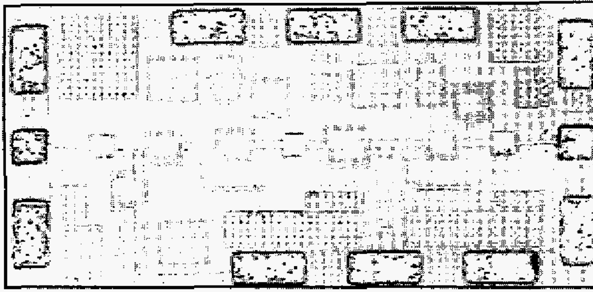

Fig. 3. Chip photo of the TFMS LNA with a chip size of 0.77 x 0.4 mm^2.

The measured small-signal gain and return losses are shown in Fig. 4 under 1.2 V with a total power consumption of 16.8 mW. The measured peak gain is 12.9 dB at 21 GHz with the gain higher than 10 dB from 18.6 to 26.3 GHz. The input return loss is better than 10 dB between 18.6 and 23.8 GHz, and the output return loss is better than 10 dB above 19.6 GHz. Figure 5 shows the measured noise figure, and this amplifier has a noise figure of better than 5.4 dB from 20 to 26 GHz.

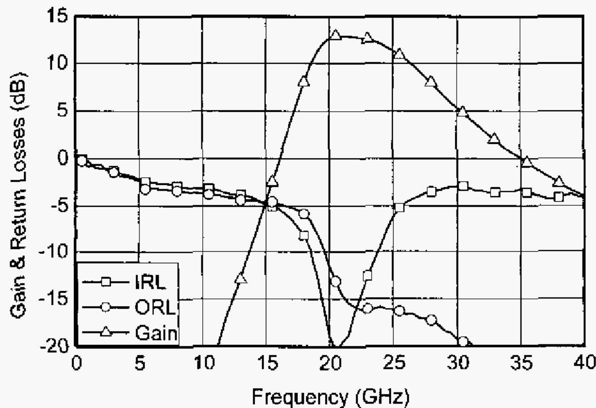

Fig. 4. Measured small-signal gain and return losses of the TFMS LNA.

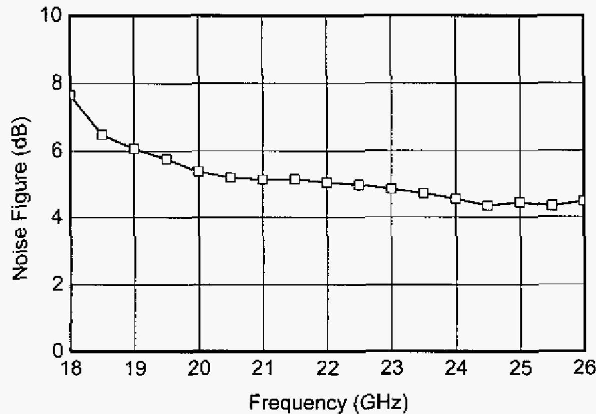

Fig. 5. Measured noise figure of the TFMS LNA.

V. CMOS LNA USING CPW

This amplifier which is fabricated in the 90-nm 1P9M CMOS process employs a two-stage cascaded common-source structure. Both transistors in this circuit are 16 fingers with a total gate width of 64 μm. Figure 6 shows the schematic, and the corresponding chip photo is shown in Fig. 7. The input and output are matched to 50 Ω by series transmission lines as well as short stubs. The technique of source degeneration is utilized in both stages for stability concern. The second stage employs a parallel resistive feedback, which leads to a broadband response. The matching elements of CPWs are meandered to achieve a smaller chip size of 0.98 x 0.82 mm^2.

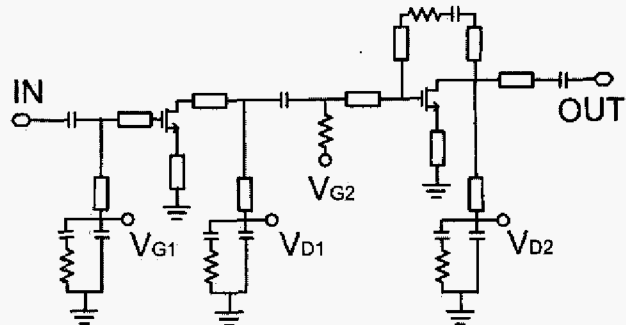

Fig. 6. Schematic of the CPW LNA.

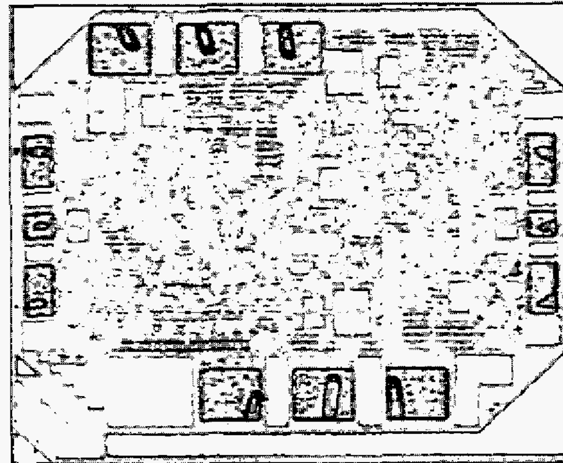

Fig. 7. Chip photo of the CPW LNA with a chip size of 0.98 x 0.82 mm^2.

The measured small-signal gain and return losses are shown in Fig. 8 under 1.2 V with a total power consumption of 26.4 mW. The measured peak gain is 16.2 dB at 20.5 GHz with the 3-dB bandwidth of 8 GHz from 18 to 26 GHz. Figure 9 shows the measured noise figure, and this amplifier has a noise figure of better than 4 dB in the entire 3-dB bandwidth. At 22.5 GHz, the noise figure achieves a minimum of 2.5 dB which is the lowest

NF among the reported MMIC LNAs using bulk CMOS processes in this frequency.

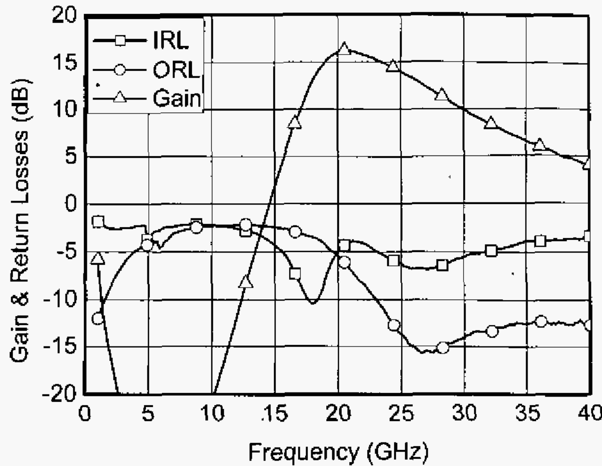

Fig. 8. Measured small-signal gain and return losses of the CPW LNA.

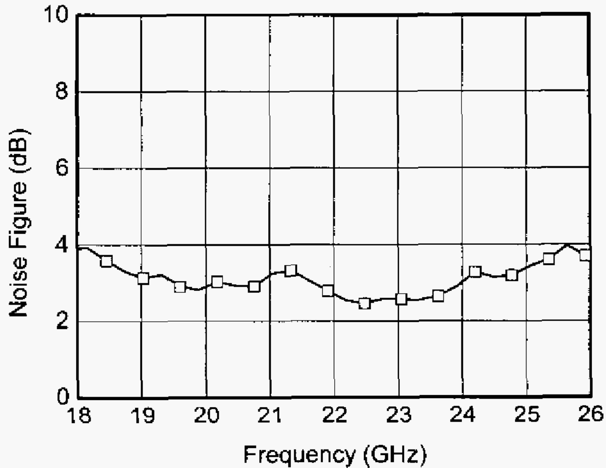

Fig. 9. Measured noise figure of the CPW LNA.

VI. Conclusion

The 130- and 90-nm CMOS LNAs were developed using TFMS and CPW, respectively. These two amplifiers demonstrate wideband characteristics and good gain and noise performance. Both of the TFMS and CPW can reduce the effect of lossy substrate, thus they are the better alternatives than the lumped elements in millimeter-wave CMOS circuit designs.

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