Novel DRAM cell with amplified capacitor for embedded application

Hyun-Jin Cho, Ming-Ren Lin
GLOBALFOUNDRIES, Inc., Strategic Technology Group, Sunnyvale, Calif., 94088
Tel: +1-(408) 749-4243, Email: jin.cho@globalfoundries.com

Abstract

Novel DRAM cell with logic process compatible and whose memory operation is the same as the conventional DRAM operation is first time introduced. The cell uses the MOS capacitor with open base NPN bipolar transistor to amplify the storage capacitor. We fabricated the prototype cell and demonstrated the memory cell operation.

Introduction

There have been various attempts to construct a DRAM cell in a logic process flow with minimal added process complexity while enjoying the benefit of large cache size. Most ideas rely on storing charges in the floating body of the device and read the active current.[1-3] Apart from the serious disturb issue, the major problem of these cells is the complicated operating schemes such as narrow timing margin and large number of power supplies, resulting in poor array efficiency. A new DRAM cell with the same operation scheme as the conventional DRAM with no extra capacitor process is introduced for the first time.

Device concept

Fig. 1 illustrates the equivalent circuit and cross sectional view of new DRAM cell. The basic idea is to transform a conventional SOI NFET into a MOS capacitor with open-base NPN bipolar transistor. Charges are stored (D1) - or not stored (D0) - in the MOS capacitor connected in the floating-base node. During the read operation or charge-sharing operation, the original stored charge, Qg, is amplified by the bipolar action, resulting in bigger effective storage charge, $Qs = (1+\beta)Qg$. The additional charge supplies are from the power supply of the collector as shown in Fig. 2. The combination of MOS capacitor and NPN bipolar amplifies the effective capacitance, $Cs = (1+\beta)Cg$, and it produces enough storage capacitance for charge sharing operation. Since it manipulates the storage capacitor without extra external signal, it functions the same as conventional DRAM operation. The behaviors of open-base bipolar effects are illustrated in Fig. 3 using device simulation. In the case of D1 read, previously stored charges lower the emitter/base junction barrier, resulting in turning ON the bipolar transistor (b). On the contrary, there is no bipolar action during the D0 read (c). The current flow shown in (a) illustrate that the current flow occurs away from the gate surface. It is due to the higher bipolar gain in the bulk over the surface where holes are accumulated by the negative gate bias. This provides the separation of the passive element (gate capacitor) and active element (bipolar transistor) in the system.

Constant negative bias in the gate node yields maximum capacitance. This is beneficial for the write operation because negative gate bias enhances the GIDL current, which is the conduction path of charging the MOS capacitor (Fig. 4). Basic cell operation was simulated by HSPICE with DRAM-compatible sensing scheme and the results are shown in Fig. 5. The simulation has no read and write-back feature, but it is easy to conceive that it is the same as conventional DRAM cell operation.

Device design point

New DRAM cell is composed of two stacked gates over straight active line as shown in Fig. 6. It is desirable to have larger gate for storage node than access transistor. Fig. 7 shows the cell size projection and its capacitance value. From the projection, we set the target bipolar gain and it is in the range between 20 and 30 at various Cb values between 50 and 70 fF (Fig. 7 (b)). We also project the target leakage current to meet the refresh time specification. The leakage current target for 100 μs refresh interval is 1.0 pA/cell (Fig. 8(a)). The write current target is about 10 μA/cell, which enables the write speed around 2.0 ns (Fig. 8(b)).

Device fabrication

Prototype device was fabricated in 180 nm SOI process flow. New type of source/drain engineering is executed to obtain the target device parameters. We skipped the extension implant on the collector side and try to minimize the leakage current. We introduced the high-angle implant on the emitter side to enhance the GIDL current. Only one extra mask step was added in the process: GIDL mask.

Transient measurement

Transient measurements were conducted on single DRAM cells, using the set up described in Fig. 9. Bit line node of the DRAM cell is connected to the gate of the sensing transistor. This node is also connected to the NFET switch, which control the pre-charge or write operation. The bit-line cap is consisted with the wire cap as well as gate cap of sense transistor. The current of the sensing NFET transistor is monitored through the voltage level across the 50 Ohm resistor in the oscilloscope.

Device characteristics

A. Bipolar Gain

Basic NPN bipolar gain was measured in 4-terminal body-contacted SOI NFET device (Fig. 10). Stable bipolar gain was obtained in wide range of collector voltages. We observed that the gain is gradually increased with increasing gate bias. It is due to the change of effective doping concentration in base region influenced by the gate field. When device is in a weak accumulation mode, surface current starts to flow and triggers bipolar "punch-through." Fig. 11 shows the bipolar gain with different base width (gate length) and base doping concentration. Bipolar gains are sensitive to the base doping concentration. We were able to achieve the target bipolar gain by modulating the base doping concentration and the base width.

B. GIDL and leakage current

GIDL current was measured at the base-emitter junction and leakage current was measured at the collector-base junction from the same structure (Fig. 12). The GIDL current is increased with base doping concentration and insensitive to the channel length. The leakage currents are relatively insensitive to both doping concentration and channel length, providing that the major leakage source is diffusion current. Good collector leakage current was achieved, provided that the process is not optimized for low junction leakage devices.

Both bipolar gain and leakage current met the desired parameters but we failed to achieve the high GIDL current necessary for high-speed operation.

C. Transient measurement

The read/write operation of DRAM cell was evaluated by transient measurement with the setup described previously. The read operation is realized by monitoring the current level of NFET source follower (sensing transistor). The write and pre-charge operation are conducted by switching the NFET transistor with proper pulse value (Vdata). Fig. 13 is the result of the cell operation. The current level before the read operation is zero (marked Λ in the figure), ensuring that the bit line is properly pre-charged to ground. The read operation kicks in by firing the access transistor (VWL). The voltage level of the bit line is then developed by charge-sharing operation, $Vb/Vin = Cs/(Cs+Cb)$, where Vin is the data input voltage, Cs is the effective storage capacitance, and Cb is the bit-line capacitance. It is difficult to measure the actual bit-line voltage due to the non-linear nature of the gain in source follower but simple approximation was made to extract the data. It is proper to compare the delta of D1/D0 voltage level at standby rather than read because of the extra noise from the WL signal during read operation. It is shown that good sensing margin between D1 (marked [1]) and D0 (marked [2]) are observed. Note that the output voltage shown in Fig. 13 is the voltage measured at 50 Ohm resistor and the actual bit line voltage is extracted later.

The sensing margin, voltage level difference between D0 and D1, was measured with respect to various Vcollector and Vgate (Fig. 14). The optimum Vcollector is around 0.6 V, large enough to drive the bipolar transistor and small enough to reduce the junction leakage. An interesting D0/D1 trend was observed in the Vgate case. When the Vgate is near ground, the bipolar transistor is always ON regardless of the charge state of the base region, resulting in high bit-line voltage in both D0/D1. On the contrary, when the negative Vgate is too strong, it pulls the stored charge through the gate oxide and reduces the D1 margin. It is shown that the optimal Vgate bias is around -0.5 V.

D. Static and dynamic refresh characteristics

Both static and dynamic refresh characteristics are no different from the conventional DRAM cell on SOI substrate. The major component of the static refresh characteristics are junction leakage and the subthreshold leakage current of the access transistor. The only disturb mode is the bit-line disturb where other cells in the same bit-line are in read or write operation continuously. Bit-line disturb mode is studied using a device simulation as shown in Fig. 15. Figure shows the faster charge loss by dynamic than static mode. It is due to the increased subthreshold leakage current caused by the injection of charges into the floating body of the access transistor. Further improvement of disturb characteristics are obtained by decreasing VSSWL voltage. It is noticed that the potential at the capacitor drop quickly and flatten out. This is due to the charge balance at the body between bit-line high and low states, resulting in charge "steady state".

Conclusion

We demonstrated new logic-compatible DRAM cell whose operation is the same as the conventional DRAM. Even the extra voltage levels, Vc and Vg, are not different from the voltage level used in conventional DRAM. Therefore it provides true "plug & play" compatibility.

The usage of bipolar component for amplifying cell capacitor is not limited in the conventional MOS capacitor. Same amplification operation can be achieved in the DRAM cell with dedicated capacitor; stack or trench capacitor. The additional gain element will provides large signal margin on the read operation with much simpler capacitor process.

Acknowledgement

The authors would like to thank SVTC technology for their wafer fabrication support.

References

[1] K.-W. Song et al., IEDM 2008, p 797.
[2] F. Morishita et al., ICICC 2005, p 435.
[3] H.-J. Cho et al., IEDM 2005, p 321.
[4] J. Barth et al., ISSCC 2007, p 486.

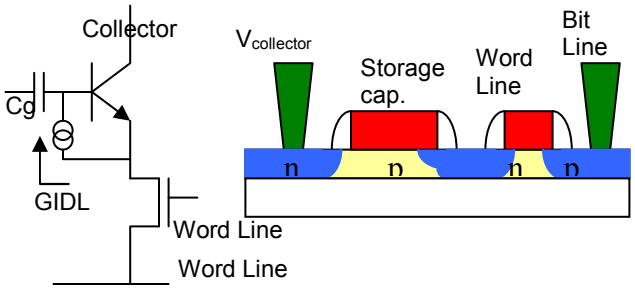

Figure 1 – Schematic and cross sectional view of the novel DRAM cell with amplified capacitor.

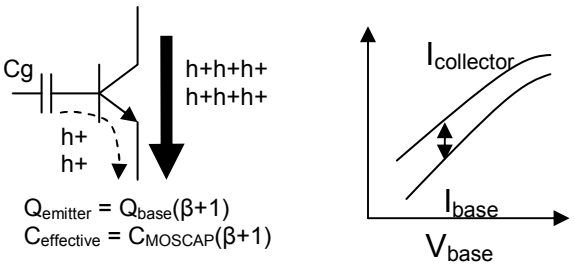

Figure 2 – Illustration of amplifying capacitor. Storage capacitor is connected to the base of the NPN bipolar transistor. When stored charges are flowing to emitter, additional charges are supplied from the collector, amplifying effective storage capacitance.

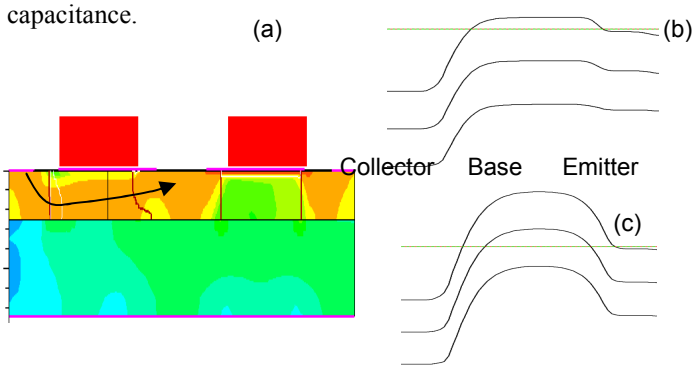

Figure 3 – Device simulation result showing (a) current flow and (b) band diagram at the start of D1 read. Previously stored charges lower the emitter/base junction barrier, resulting in turning ON the bipolar transistor. Band diagram of D0 read (c) showing no bipolar action.

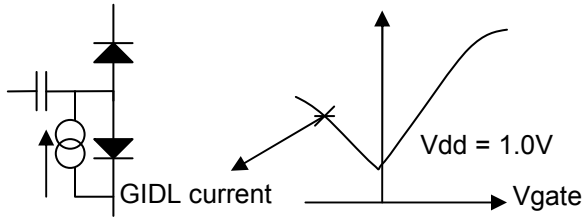

Figure 4 – Illustration of the write mechanism. GIDL current is used to write the cell. Constant negative bias of the gate and junction engineering improve the GIDL current.

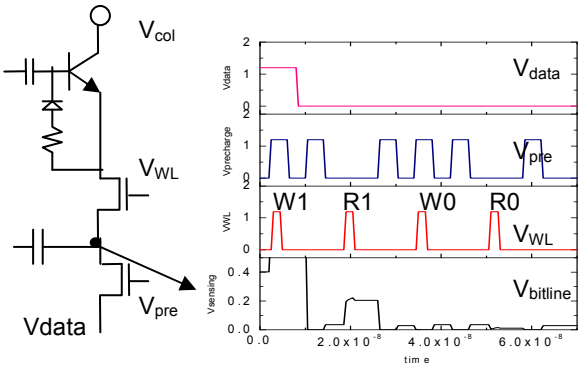

Figure 5 – HSPICE result of cell operation. The $V_{bitline}$ level difference between the Read-0 and Read-1 operation is observed. Target bipolar gain and Cb/Cs ratio is extracted using the simulation.

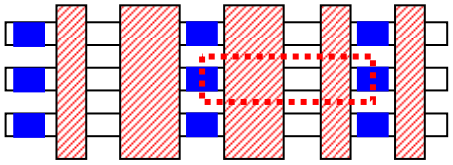

Figure 6 – Layout of the new DRAM cell. Cell is comprised of two gate lines over straight active line. Approximate cell size is 10 F^2, F = half-bit line pitch.

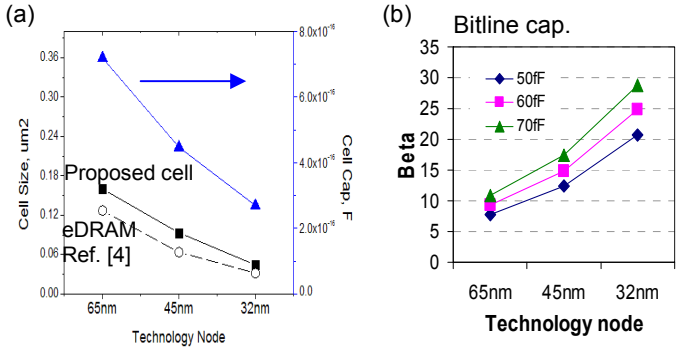

Figure 7 – (a) Cell size and gate capacitance projection. The cell size is 25% bigger than published eDRAM. (b) Target bipolar gain in various technology nodes. For the DRAM cell in 32 nm node, the target beta is between 20 and 30.

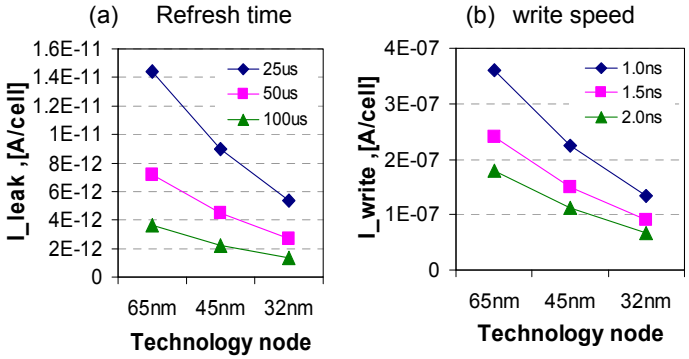

Figure 8 – Target leakage current (a) and write current (b). The DRAM operation speed is limited by the write current.

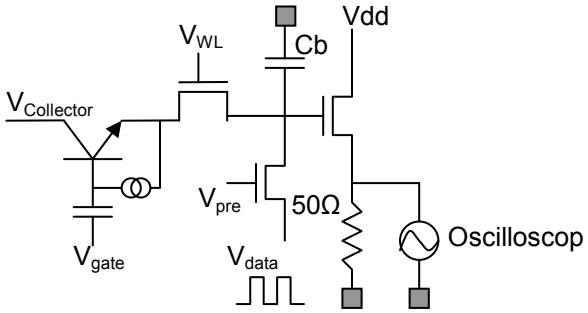

Figure 9 – Circuit setup for transient measurement. Current of the sensing NFET transistor is monitored through the voltage level across the 50 Ohm resistor in the oscilloscope. Write and pre-charge operation is performed by the NFET transistor switch with proper pulse from V_{data}.

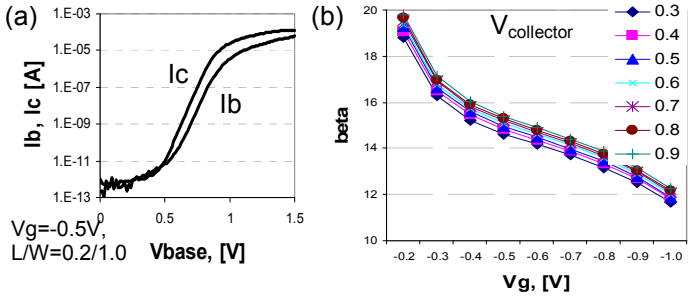

Figure 10 – (a) I-V characteristics of bipolar device measured from 4-terminal body-contacted SOI NFET structure. (b) Bipolar gain with various collector and gate voltage.

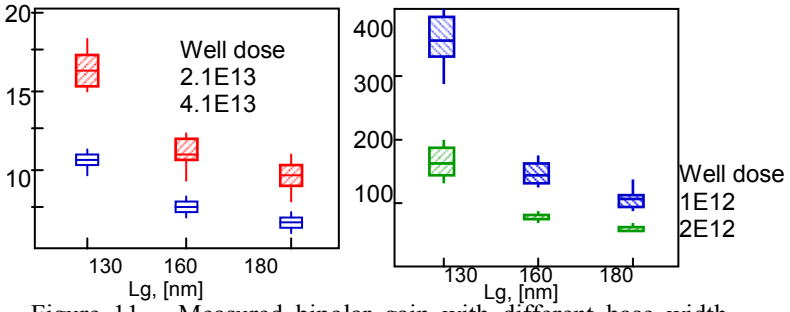

Figure 11 – Measured bipolar gain with different base width (gate length) and base doping concentration. Bipolar gains are sensitive to the base doping concentration. Gain is extracted at Vbase = 0.7 V, $V_{collector}$ = 1.0 V and V_{gate} = -0.5 V.

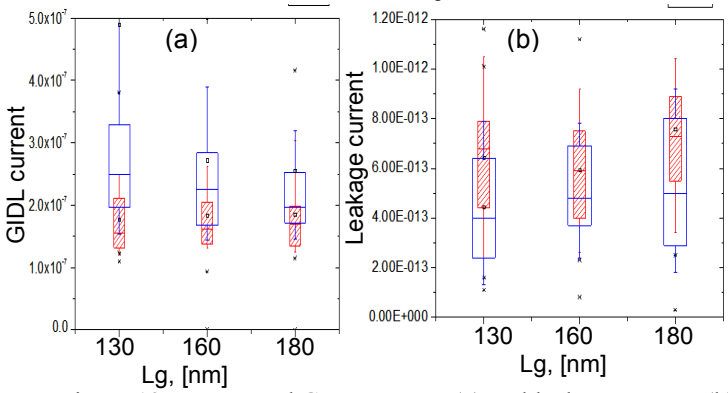

Figure 12 – Measured GIDL current (a) and leakage current (b) in various gate lengths and base implant dose condition (open box: 4.1E13, filled box: 2.1E13). Note that the current level is per μm.

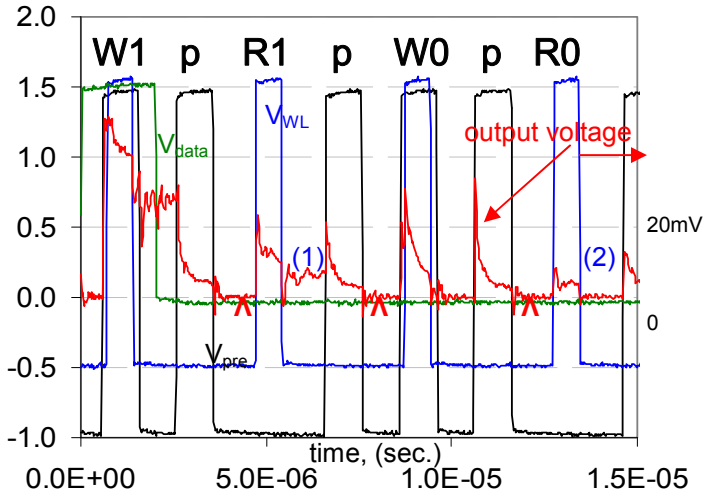

Figure 13 – Transient measurement result of amplified capacitor DRAM cell read/write operation. The read operation kicks in by firing V_{WL}. Successful memory operation was achieved.

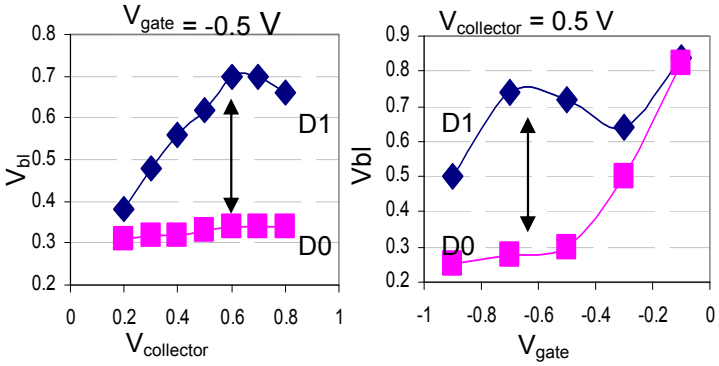

Figure 14 – Estimated V_{bl} level with respect to the $V_{collector}$ and V_{gate} bias.

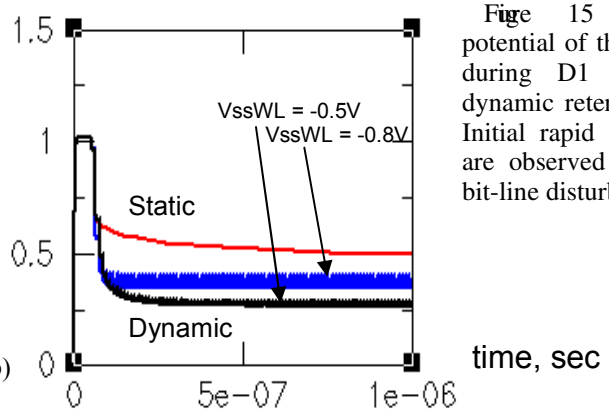

Figure 15 – Body potential of the capacitor during D1 static and dynamic retention mode. Initial rapid charge loss are observed during the bit-line disturb.