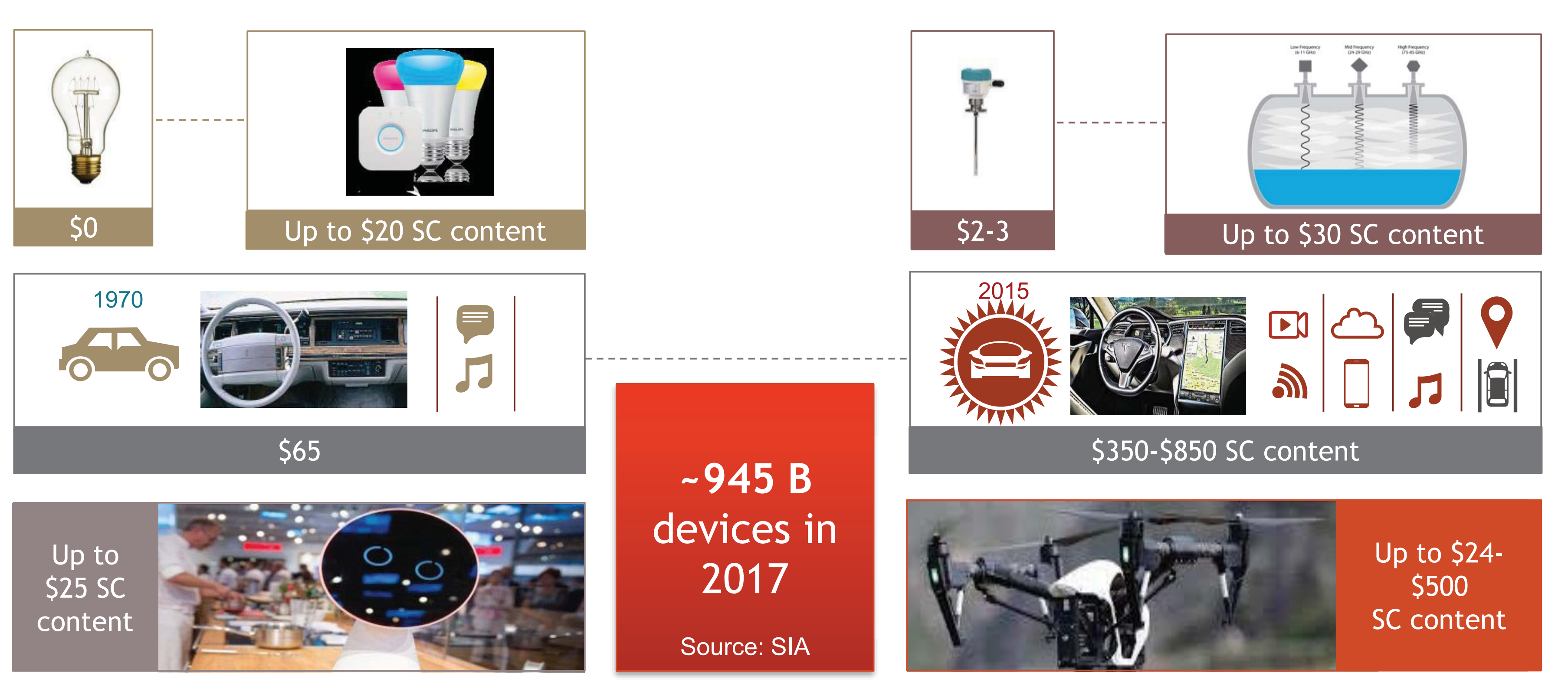
High Voltage Devices, Topologies and Gate Drivers

Yogesh Ramadass

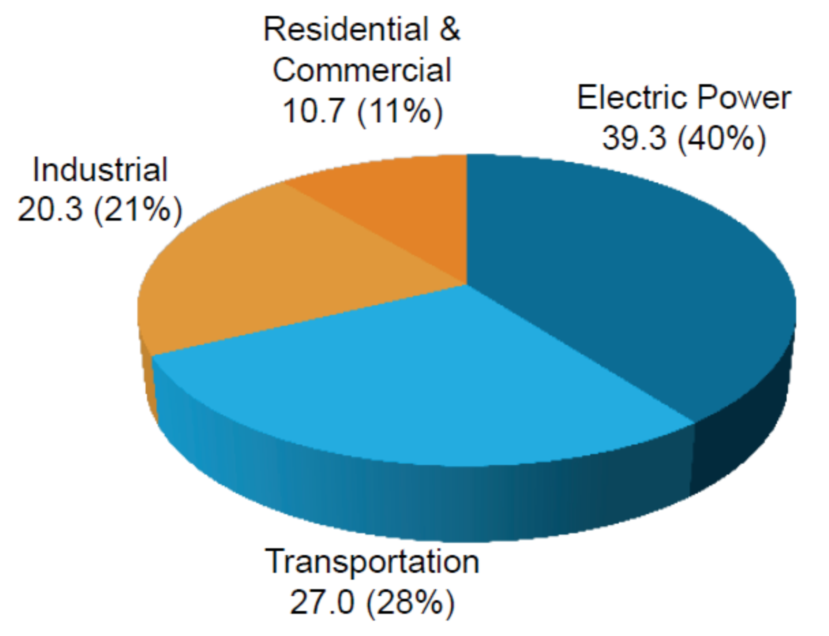
Texas Instruments

Semiconductor Growth



- More electronics adding intelligence and connectivity

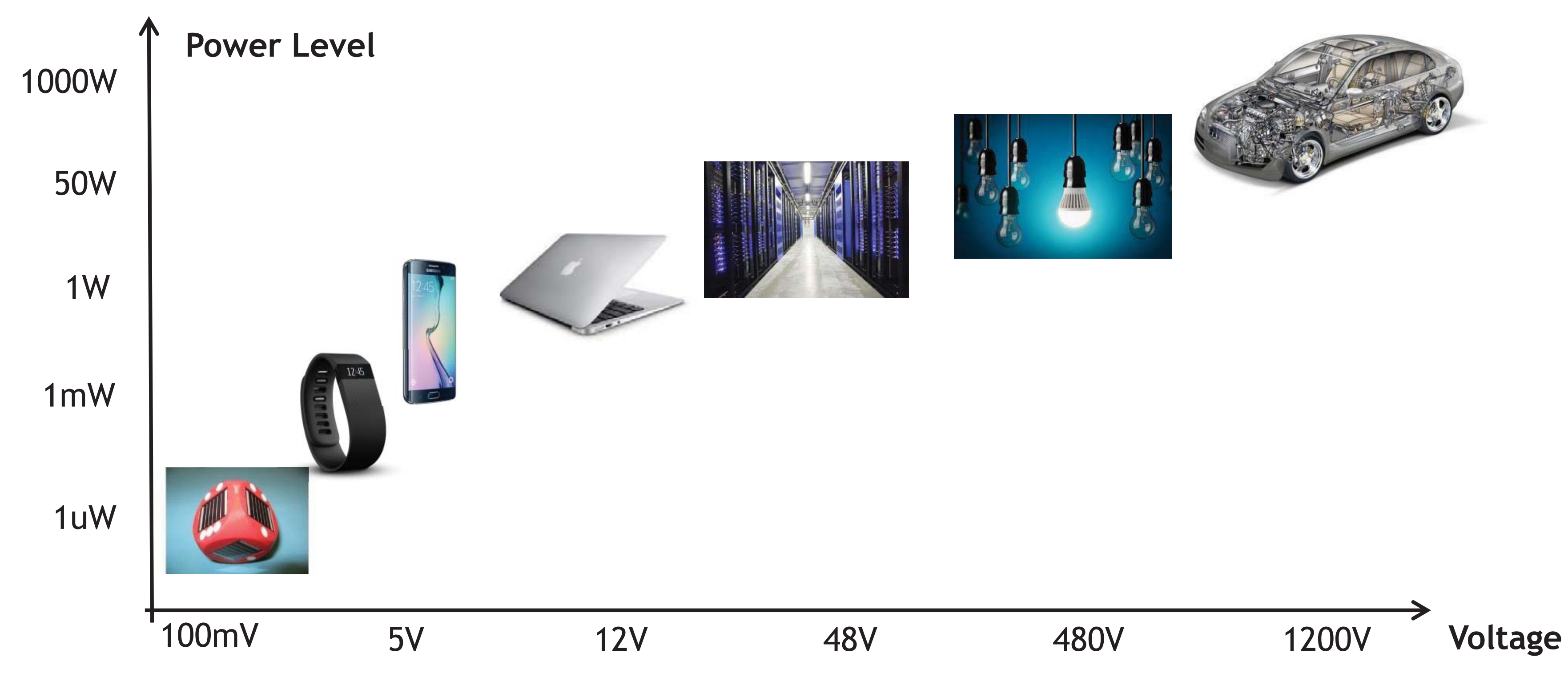
High Voltage Applications



- **2005: 30%** of electricity in flowed through power converters
- **2030: 80%** of electricity could flow through power converters

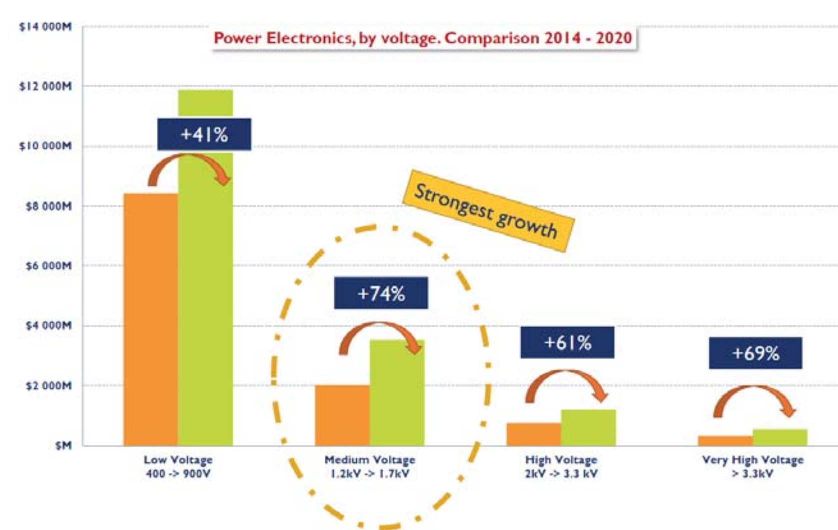
- Electricity accounts for 40% of US energy consumption

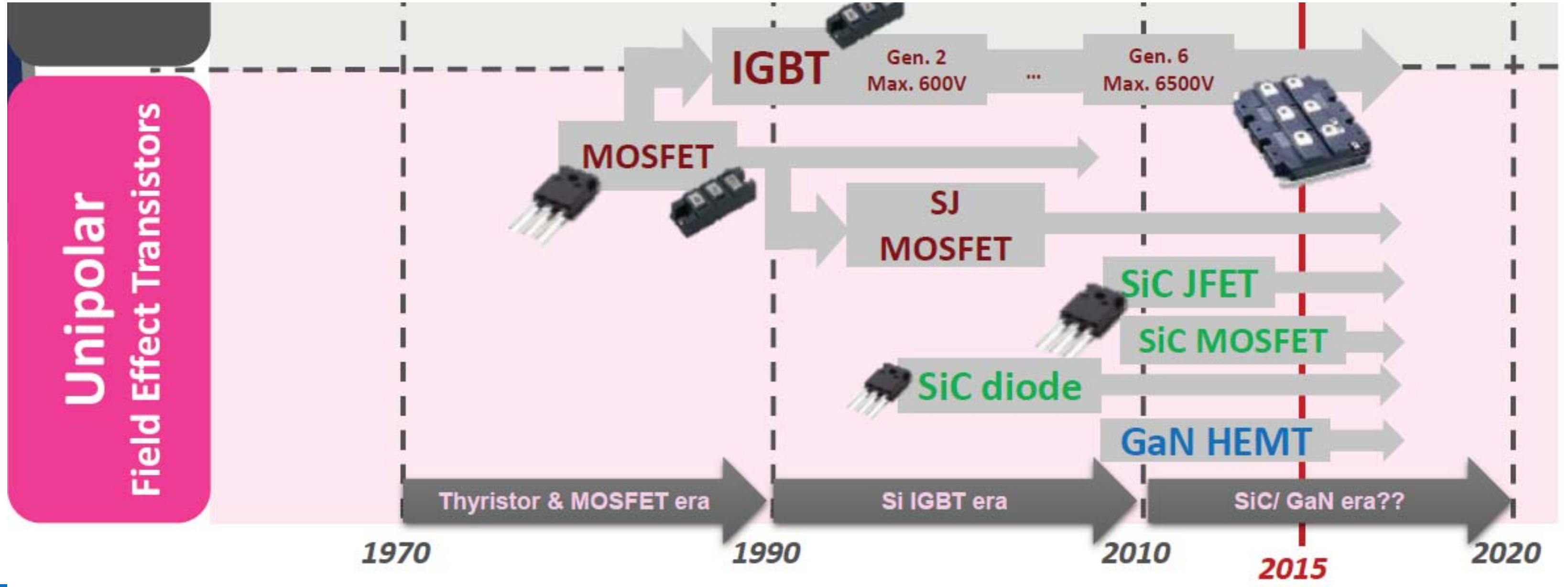
Power Electronics Landscape



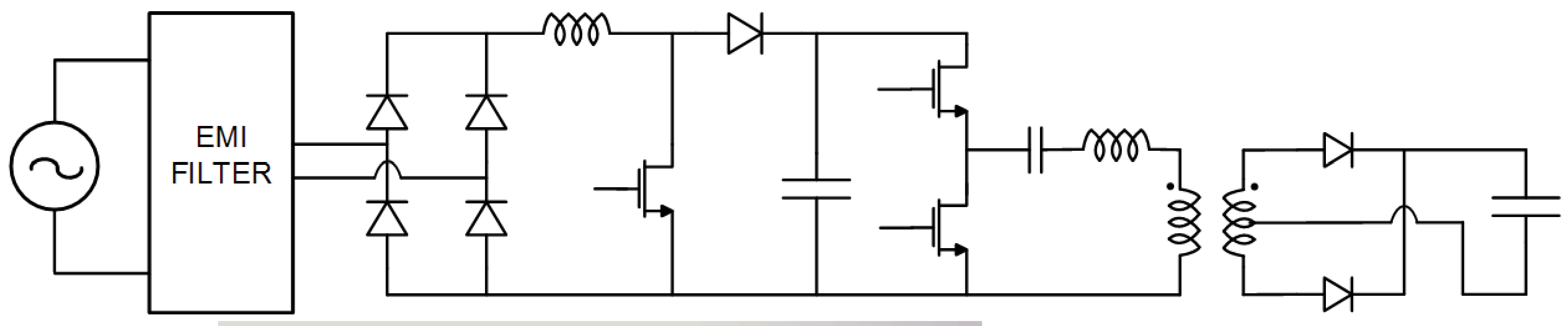
High Voltage Power Device Market

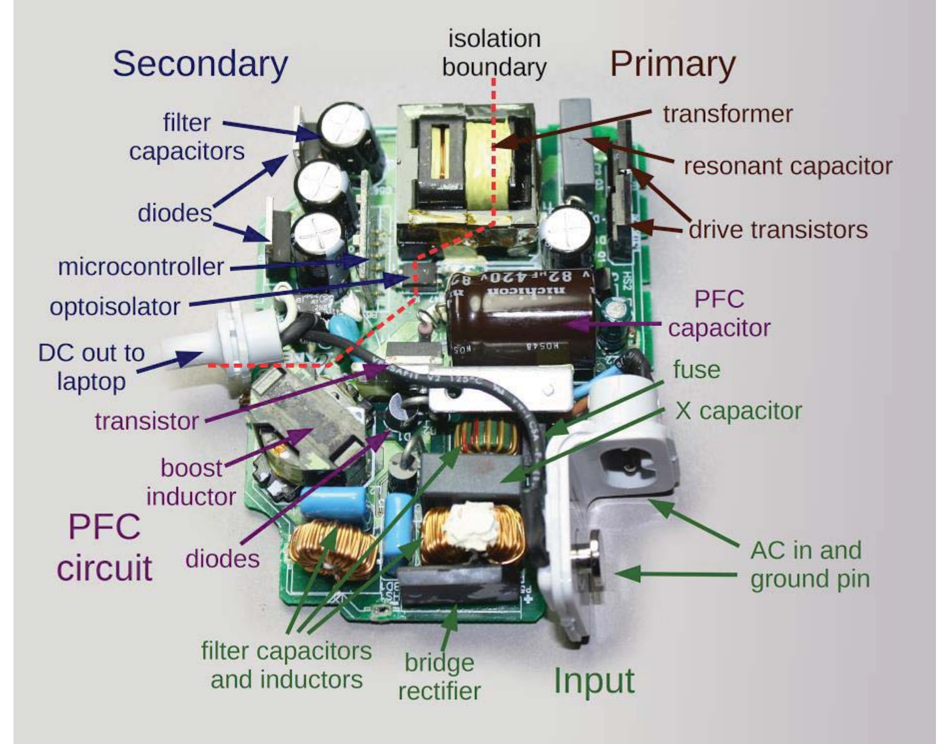
c. Yole Development, 2015





AC-DC Power Supply





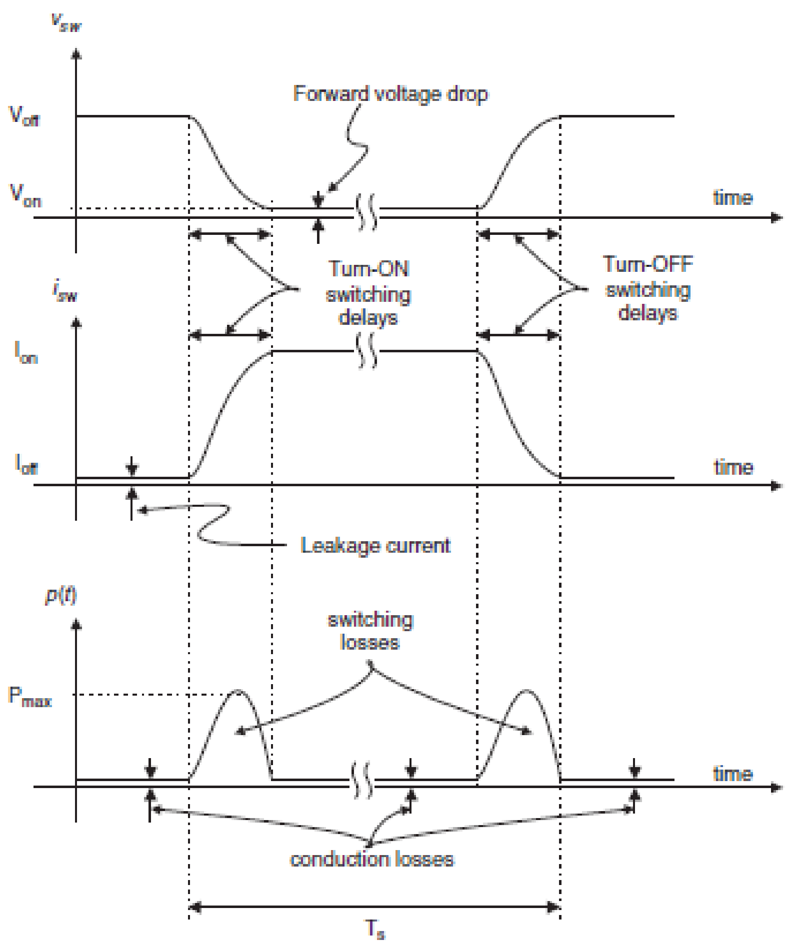
Apple Macbook 85W adapter teardown
c. www.righto.com

Outline

- Power devices
  - MOS
  - GaN
  - SiC, IGBT
- Power system topologies
  - Hard-switched
  - Soft-switched
  - Buck, flyback
- Gate Drivers
  - Drive Requirements
  - Isolation
  - Protection Circuits
- Summary

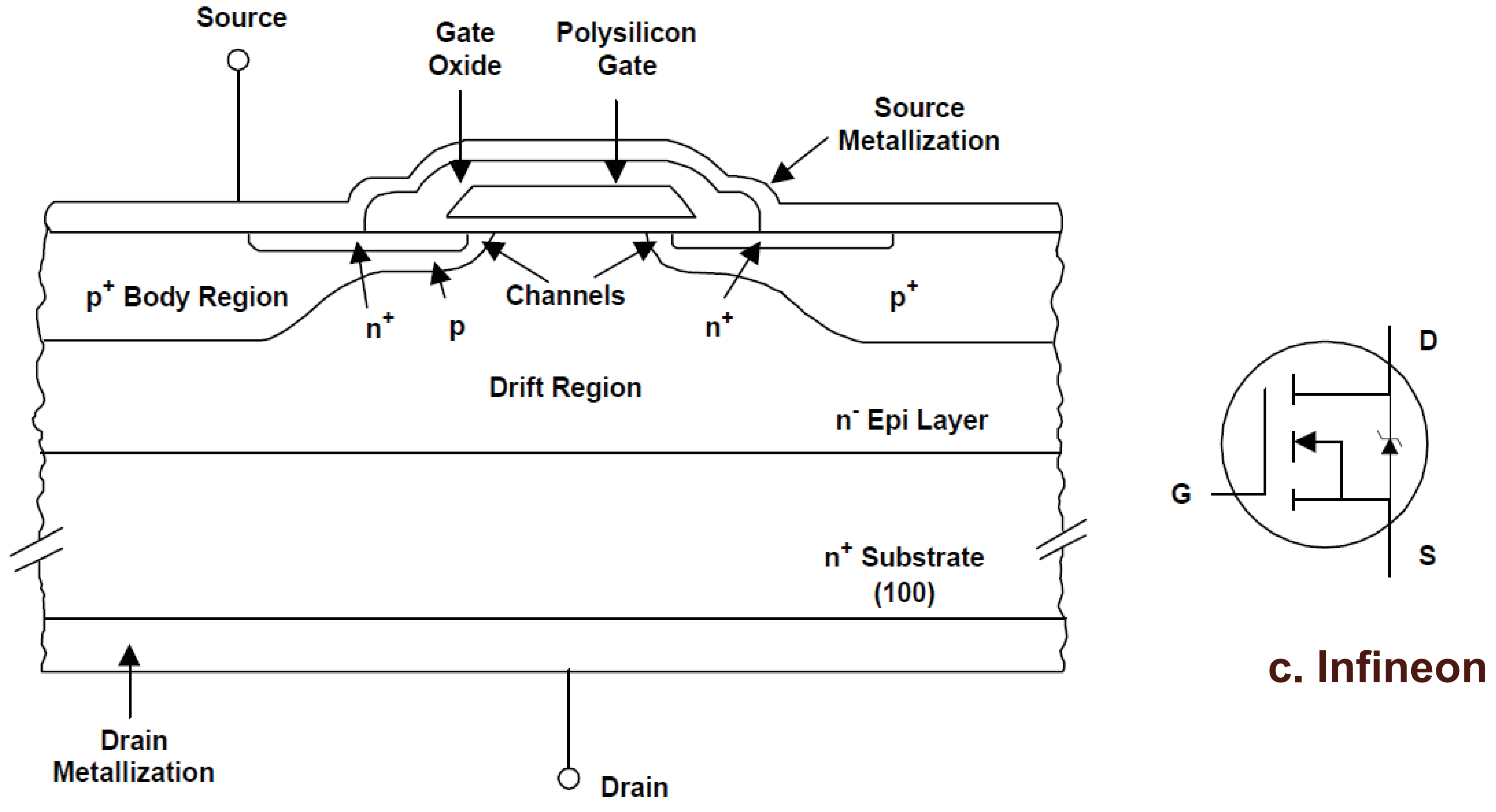
Ideal Power Switch

- Block infinite voltage
- Carry infinite current
- Zero turn/off time
- Zero power to drive
- Normally Off
- Zero cost



Real switch characteristics

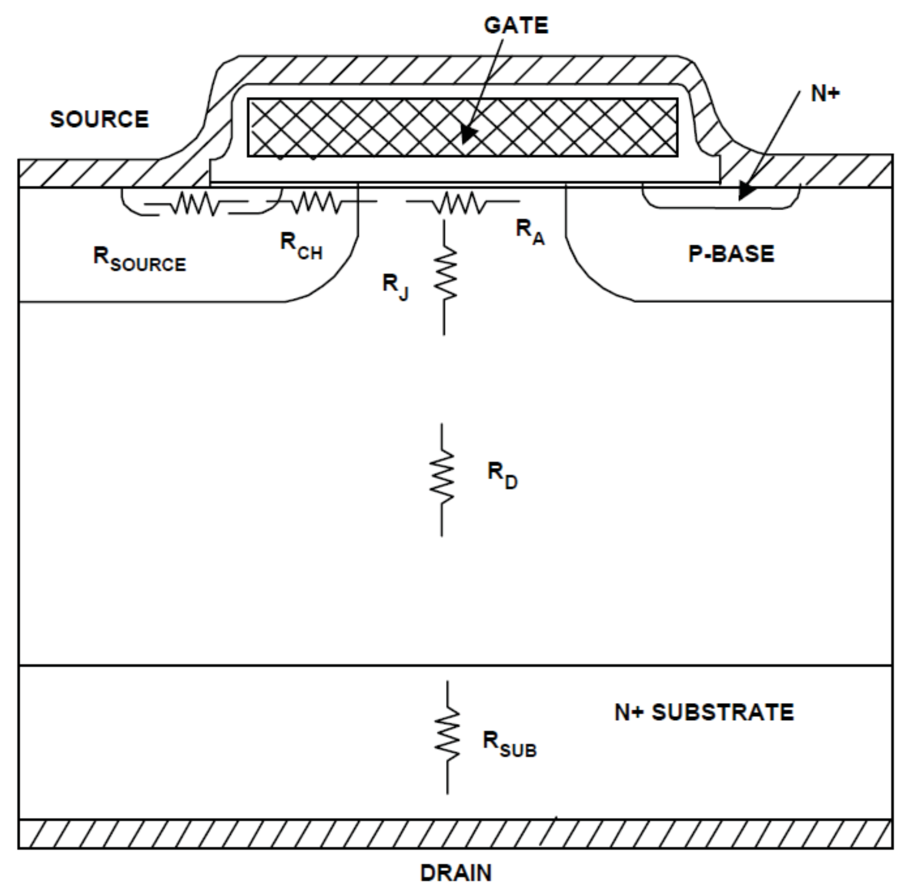
Power MOSFET construction



c. Infineon

- Vertical power MOSFET with n-type drift region

MOSFET Internal Resistance

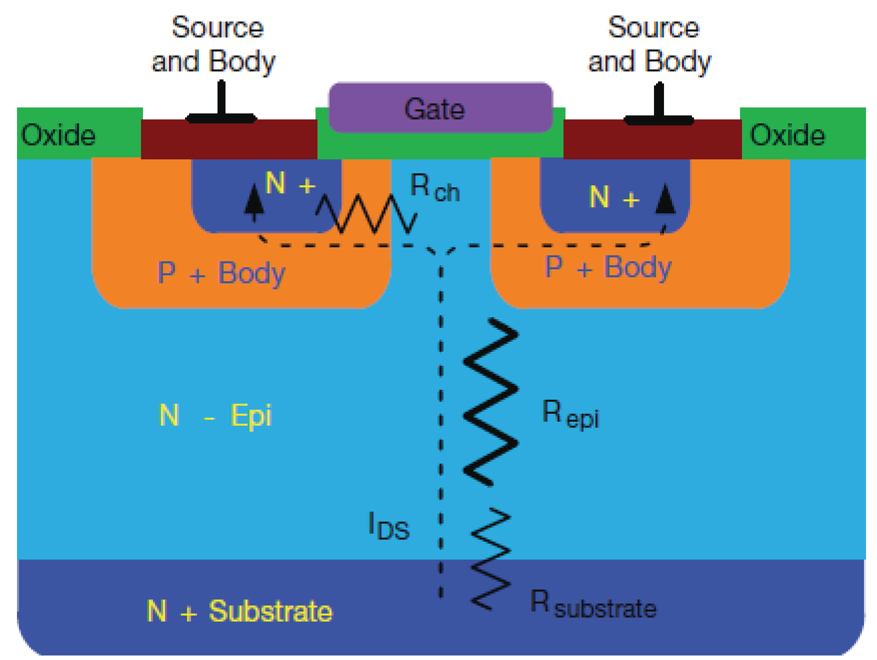


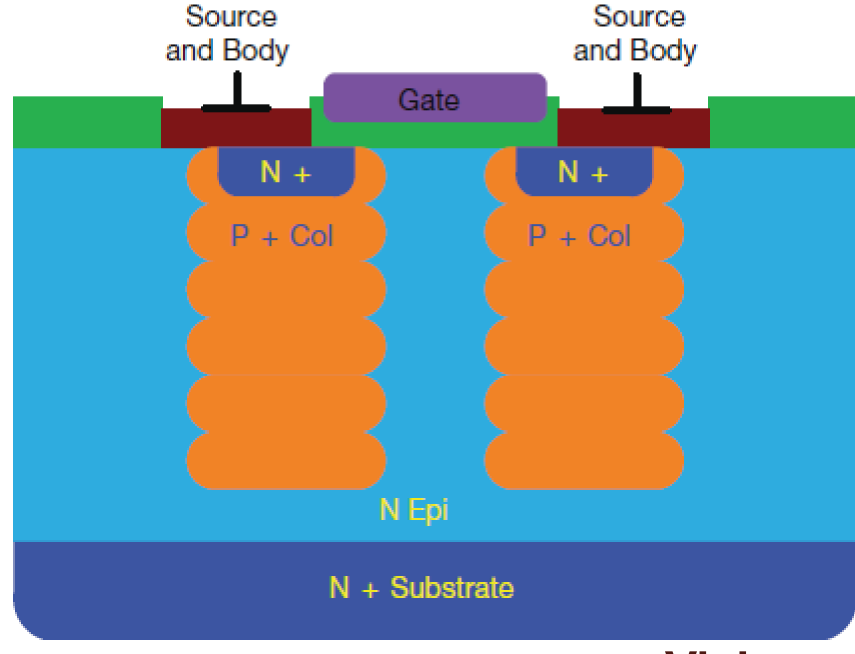
BV_{DSS}	30 V		100 V		600 V
R_{ch}	35 %	→	8 %	→	3 %
R_{epi}	35 %	→	88 %	→	96 %
R_{sub}	30 %	→	3 %	→	1 %

c. Vishay

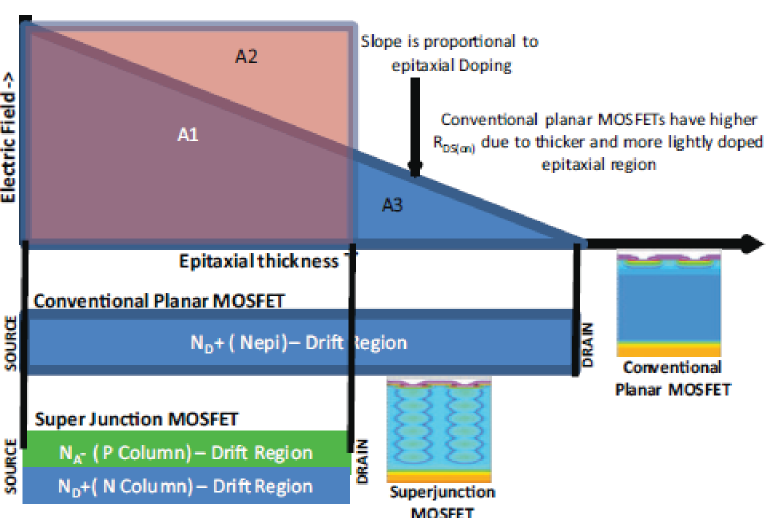
- EPI region resistance dominates at high voltages for conventional power MOSFET

Super-junction MOSFET



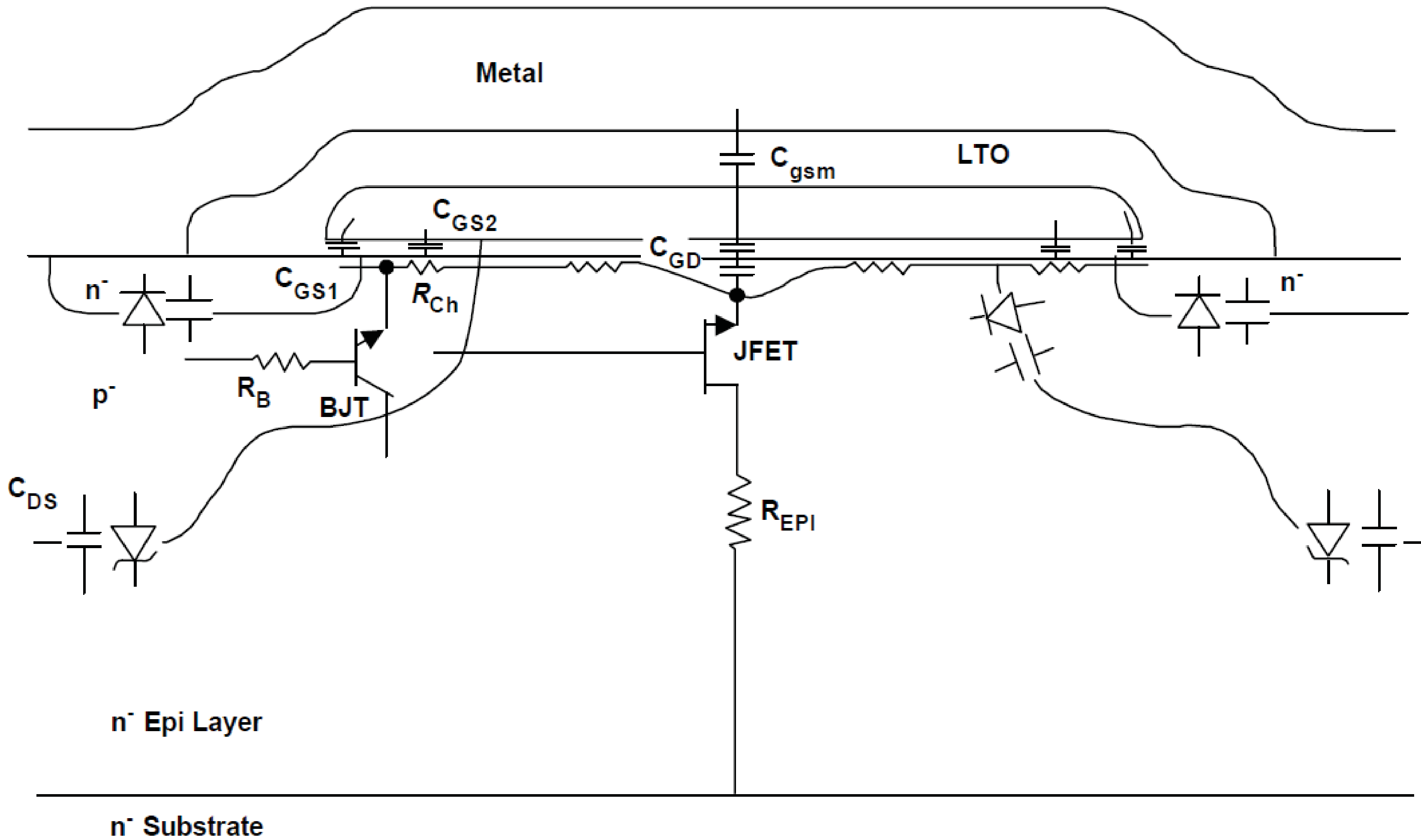


c. Vishay



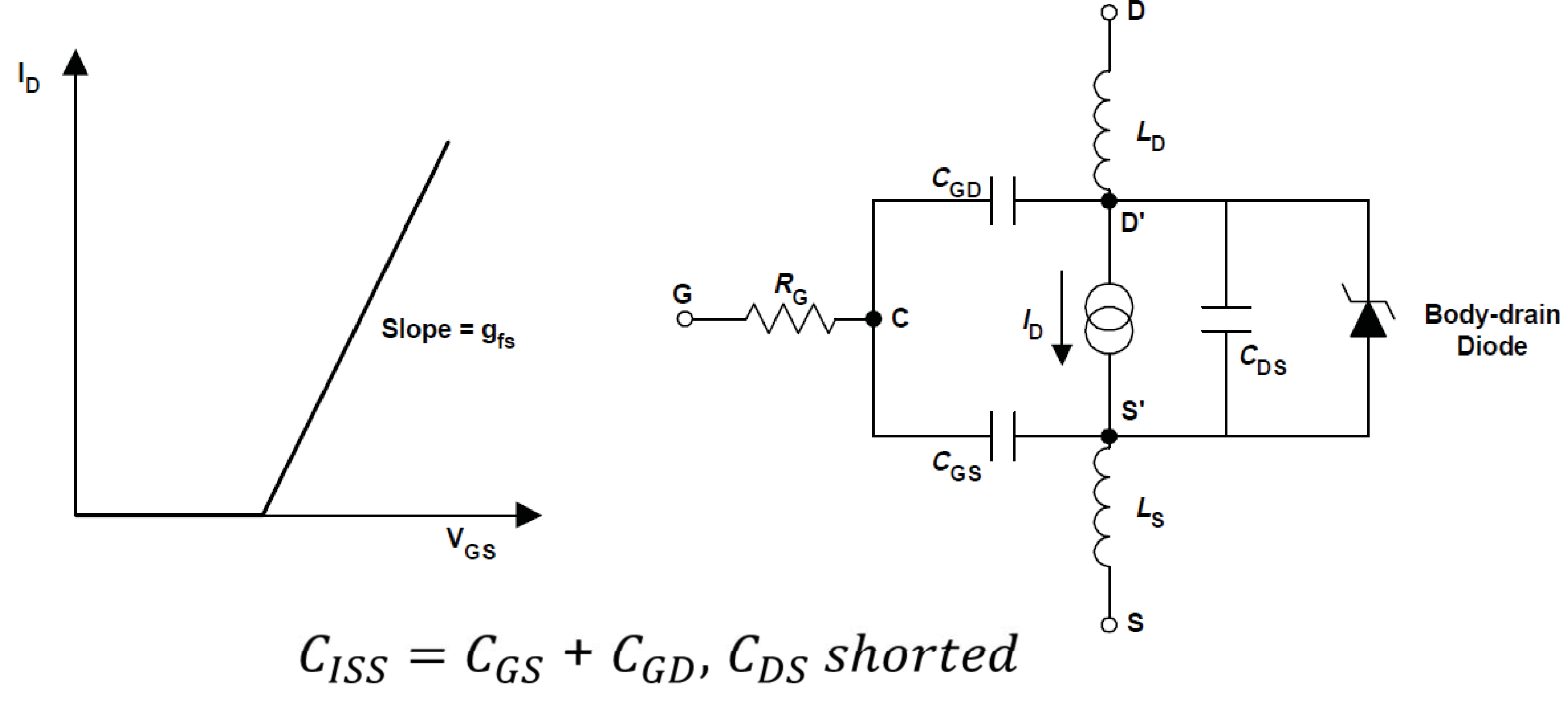
- Improved RDSON at higher voltages

MOSFET Parasitics



- Multiple parasitics define operation of power switch

MOSFET Equivalent Circuit



$$C_{ISS} = C_{GS} + C_{GD}, C_{DS}\ shorted$$

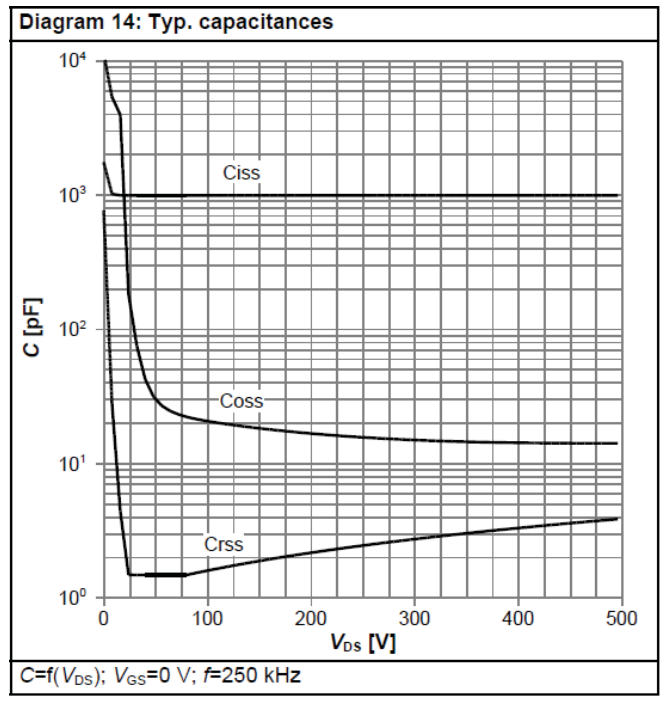
$$C_{RSS} = C_{GD}$$

$$C_{OSS} = C_{DS} + C_{GD}$$

MOSFET Capacitance

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	996	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	14	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	29	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	313	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V

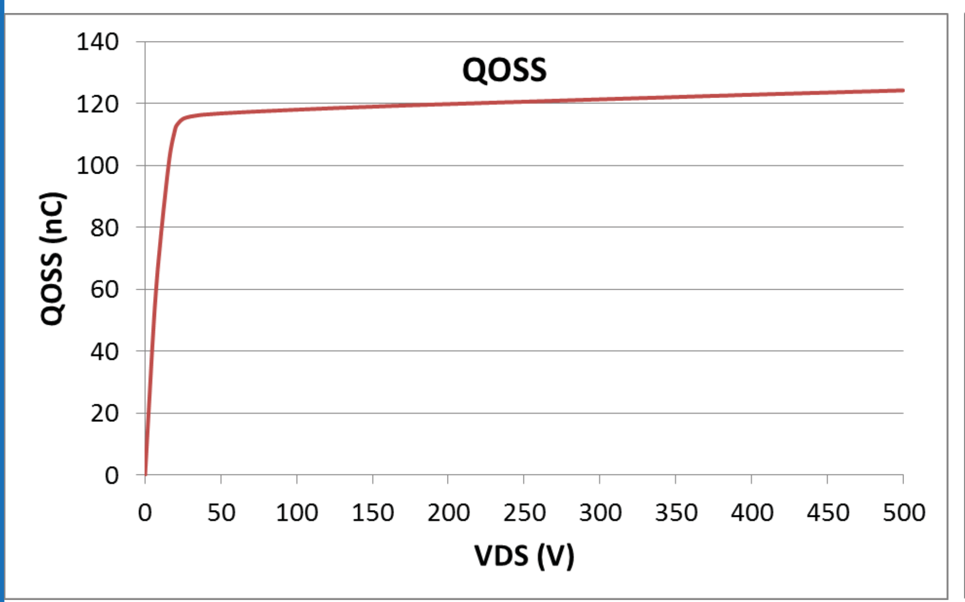


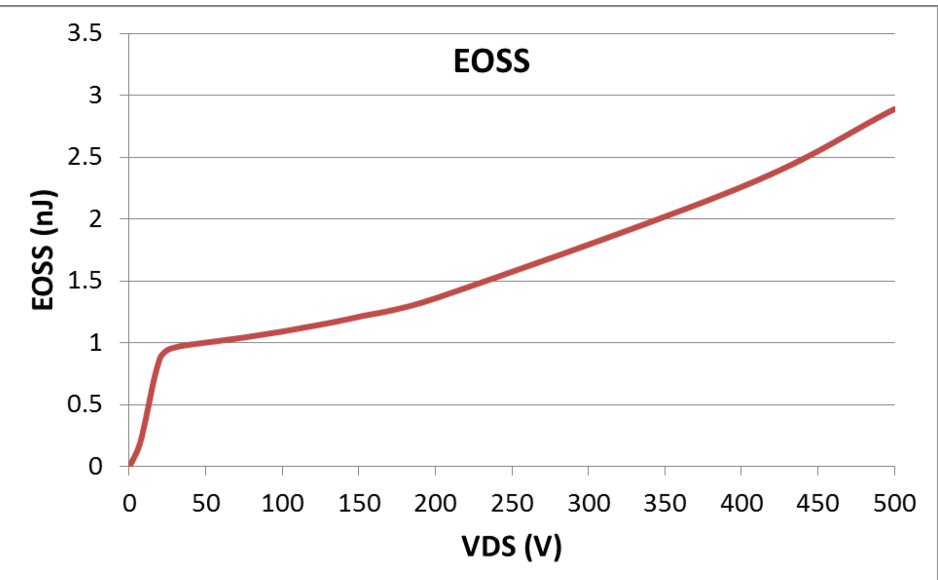
IPD65R225C7 datasheet

- Device capacitances are heavily voltage dependent

- Rated capacitance is different for time and energy related calculations

MOSFET Q_{OSS} and E_{OSS}





$$Q_{OSS} = \int C_{OSS}\, dV \qquad E_{OSS} = \int C_{OSS} V\, dV$$

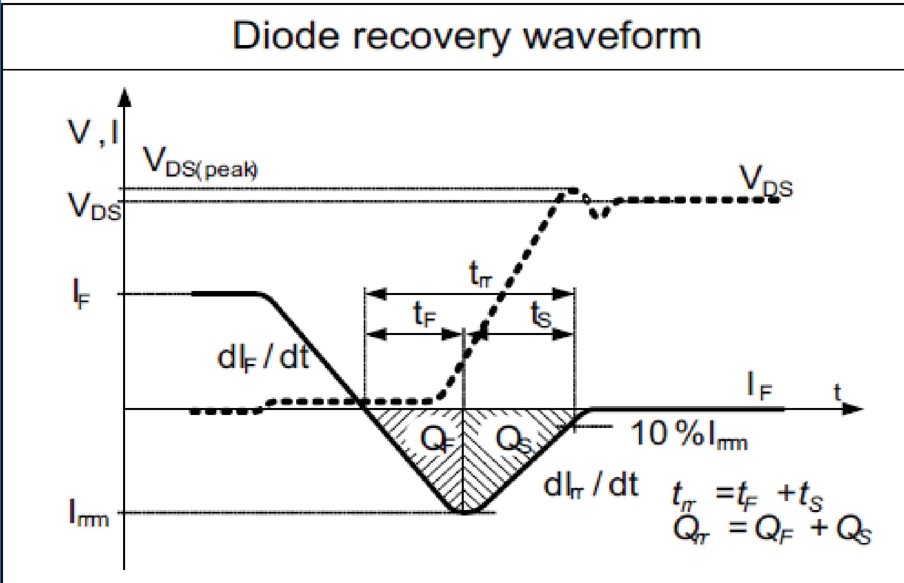
- Q_{OSS} from datasheet = 313pF x 400V = 125.2nC
- E_{OSS} from datasheet = ½ x 29pF x 400^2 = 2.32µJ

Reverse Recovery

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=17.1A, T_j=25°C
Reverse recovery time	t_{rr}	-	800	-	ns	V_R=400V, I_F=33A, di_F/dt=60A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	10	-	µC	V_R=400V, I_F=33A, di_F/dt=60A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	30	-	A	V_R=400V, I_F=33A, di_F/dt=60A/µs; see table 8

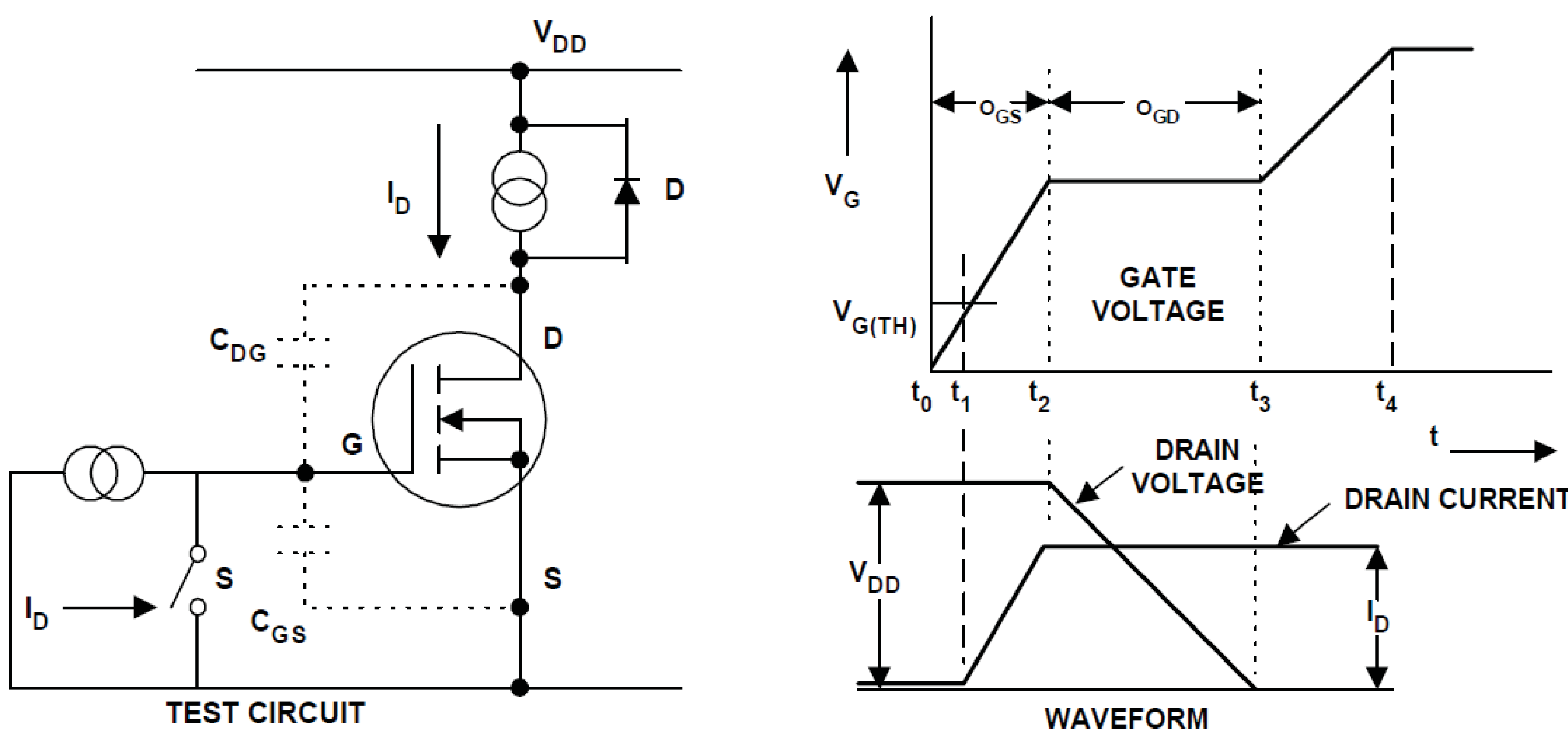
IPB65R065C7 datasheet



- Dominant loss factor in hard-switched applications

- Dependent on I_F, dI_F/dt and time for which diode was ON

MOSFET Switching



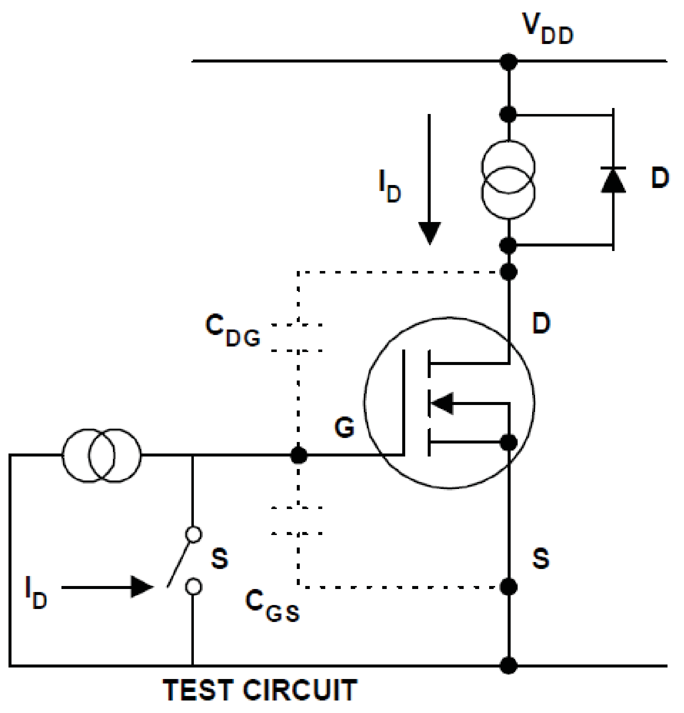
- Drain voltage starts switching when gate reaches plateau

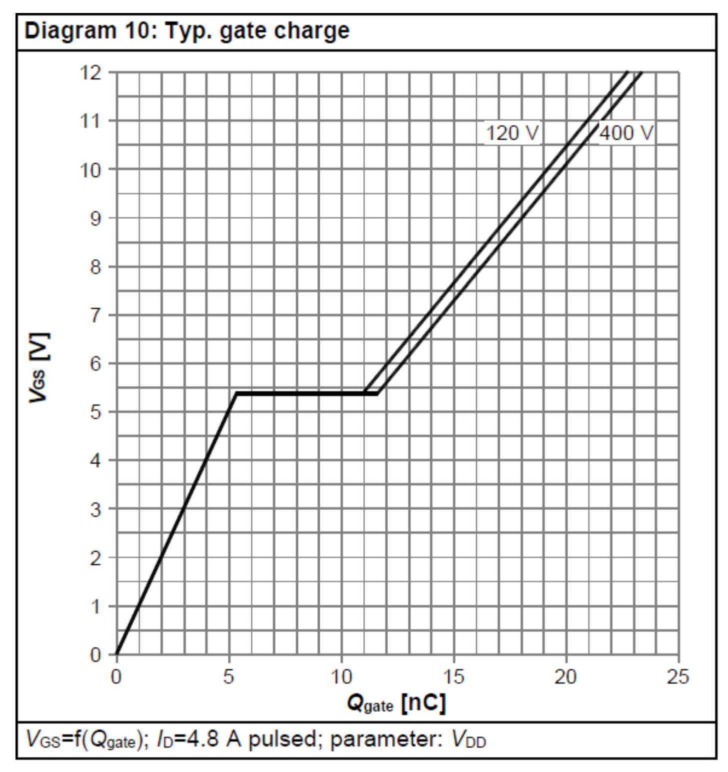
MOSFET Gate Capacitance

IPD65R225C7 datasheet

Table 6 Gate charge characteristics

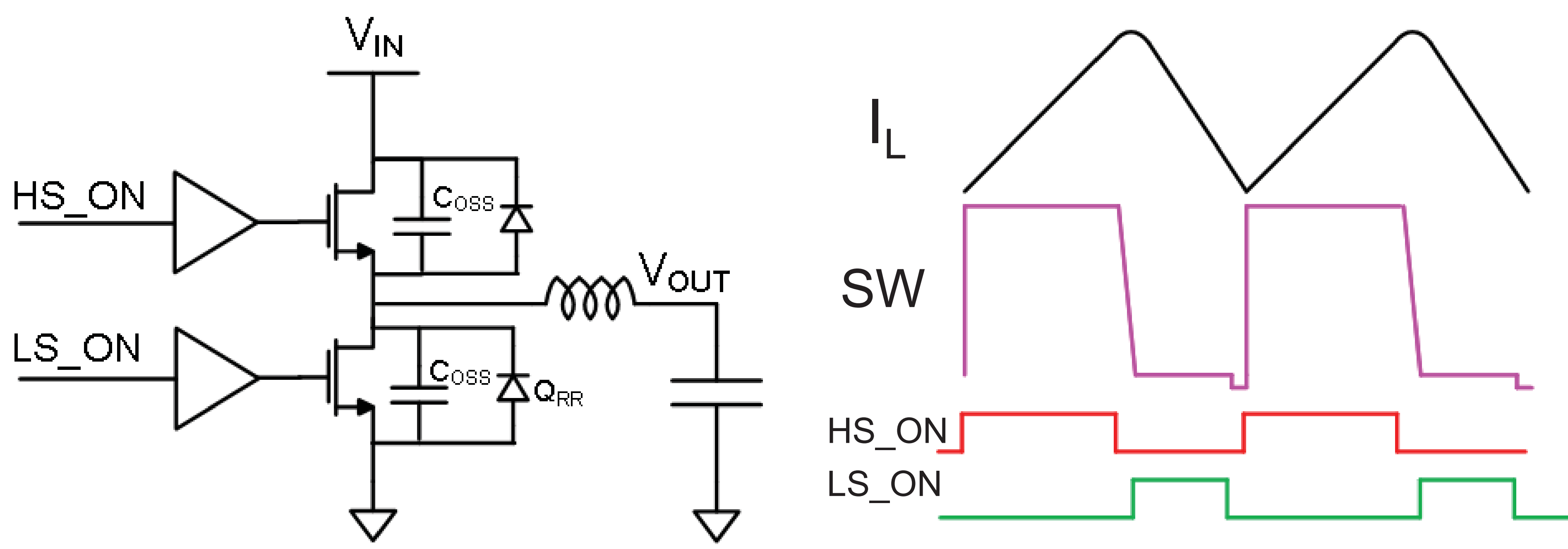
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5	-	nC	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	6	-	nC	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	20	-	nC	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V





V_{GS}=f(Q_{gate}); I_D=4.8 A pulsed; parameter: V_{DD}

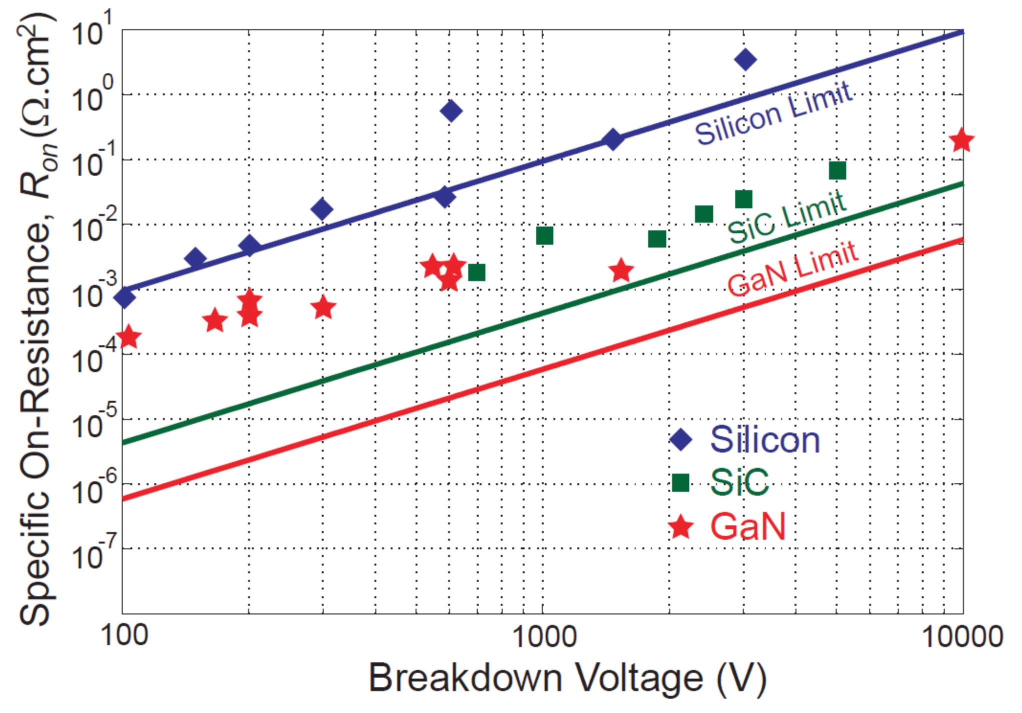
Buck converter switch related losses



Hard-Switched Buck FET Losses

Conduction	$I_{rms}^2 R_{DS}$
Switching	$Q_{OSS} V_{IN} f_{SW}$
Reverse Recovery	$Q_{RR} V_{IN} f_{SW}$
Cross Conduction	$I_{L,AV} V_{IN} t_{ov} f_{SW}$
Gate Drive	$2 Q_G V_{DRV} f_{SW}$

The wide bandgap promise



Current density

$$J = n\mu e E_c$$

Power density

$$J.E_c = n\mu e E_c^2$$

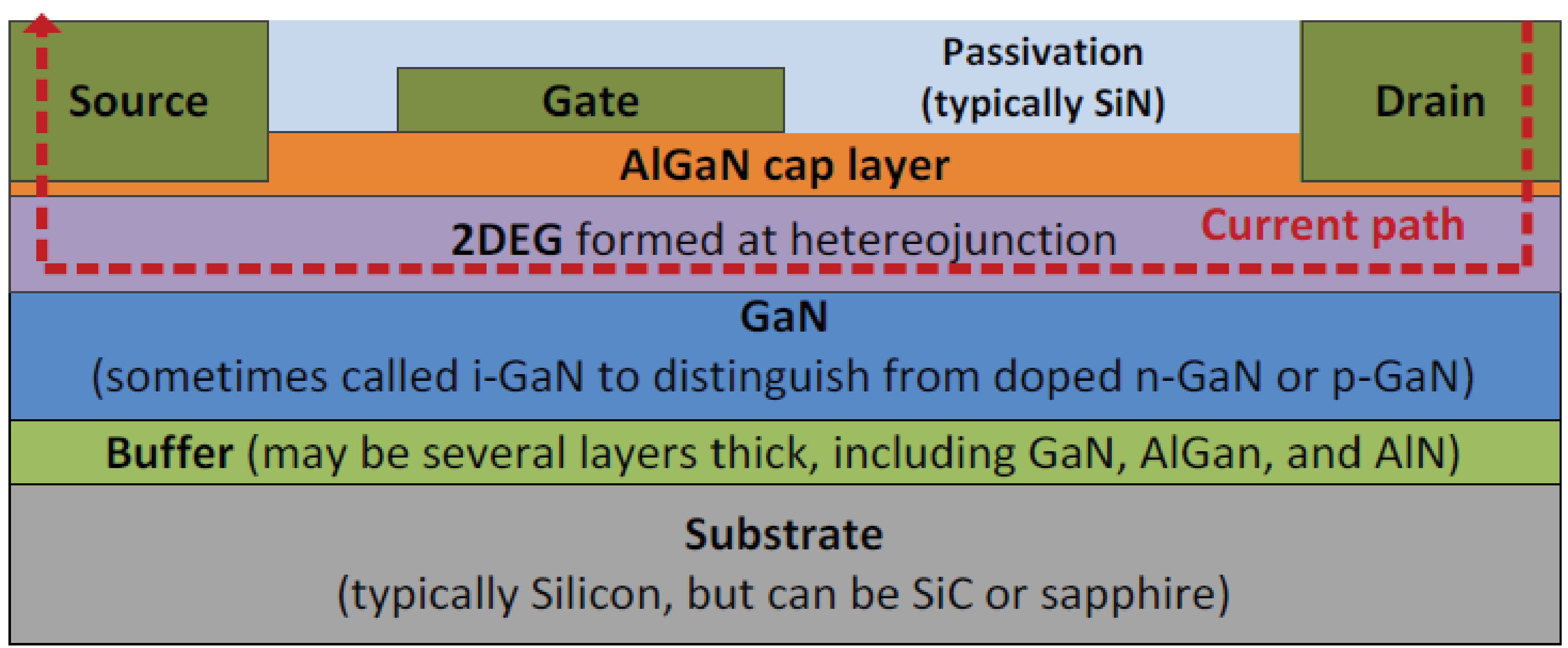
Switching speed

$$\tau_{SW} \sim v_{sat}$$

S. Bandyopadhyay, PhD Thesis, 2013

Property	Si	GaN	SiC
Bandgap Energy (eV)	1.12	3.4	3.3
Breakdown Field (MV/cm)	0.3	3.5	3.2
Electron mobility (cm^2/Vs)	1400	2000	950
Saturated Electron velocity (10^7cm/s)	1	2.5	2.5

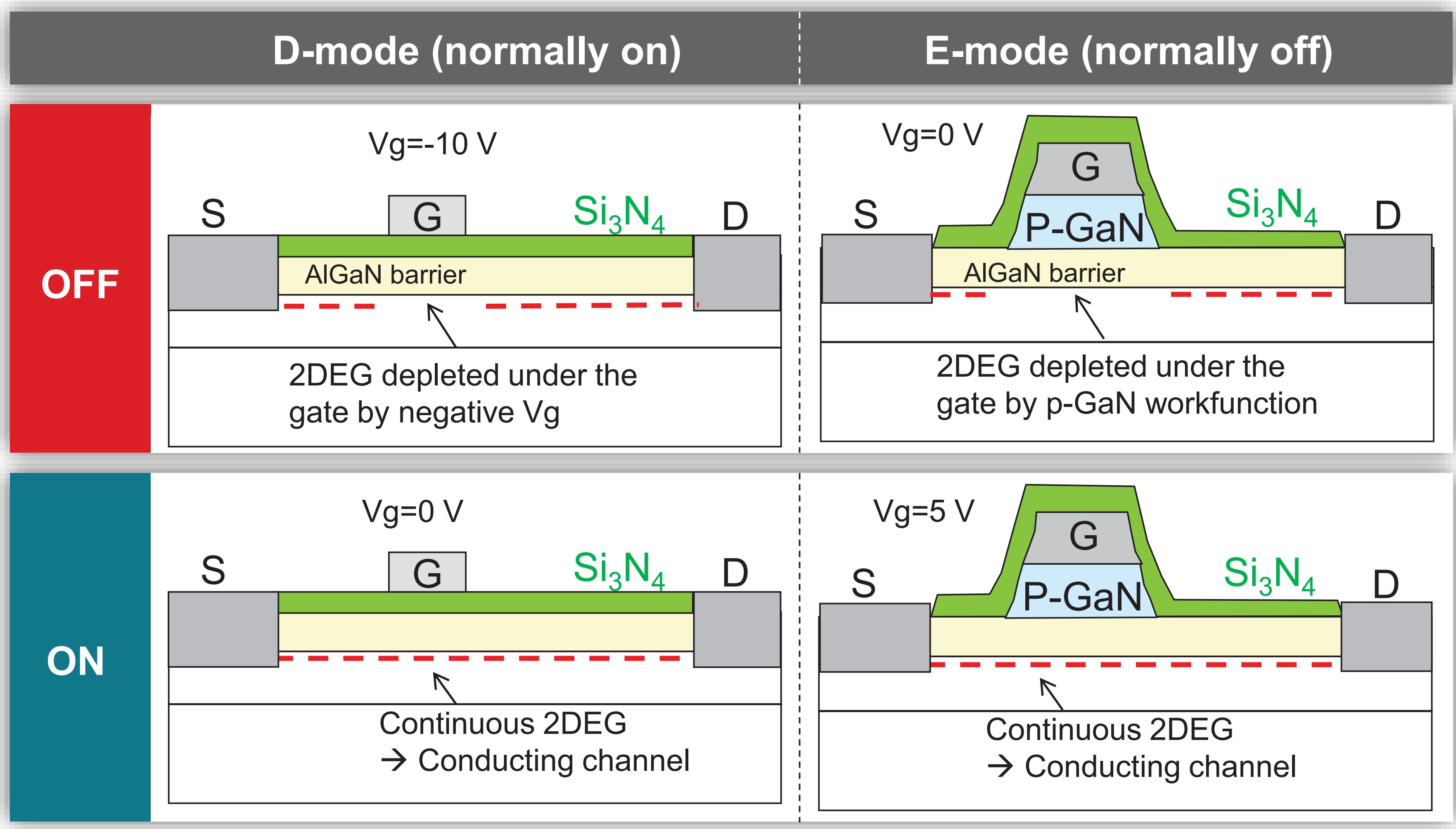
GaN construction



Ref: Jones, E.A.; Wang, F.; Ozpineci, B., "Application-based review of GaN HFETs," Wide Bandgap Power Devices and Applications (WiPDA) 2014

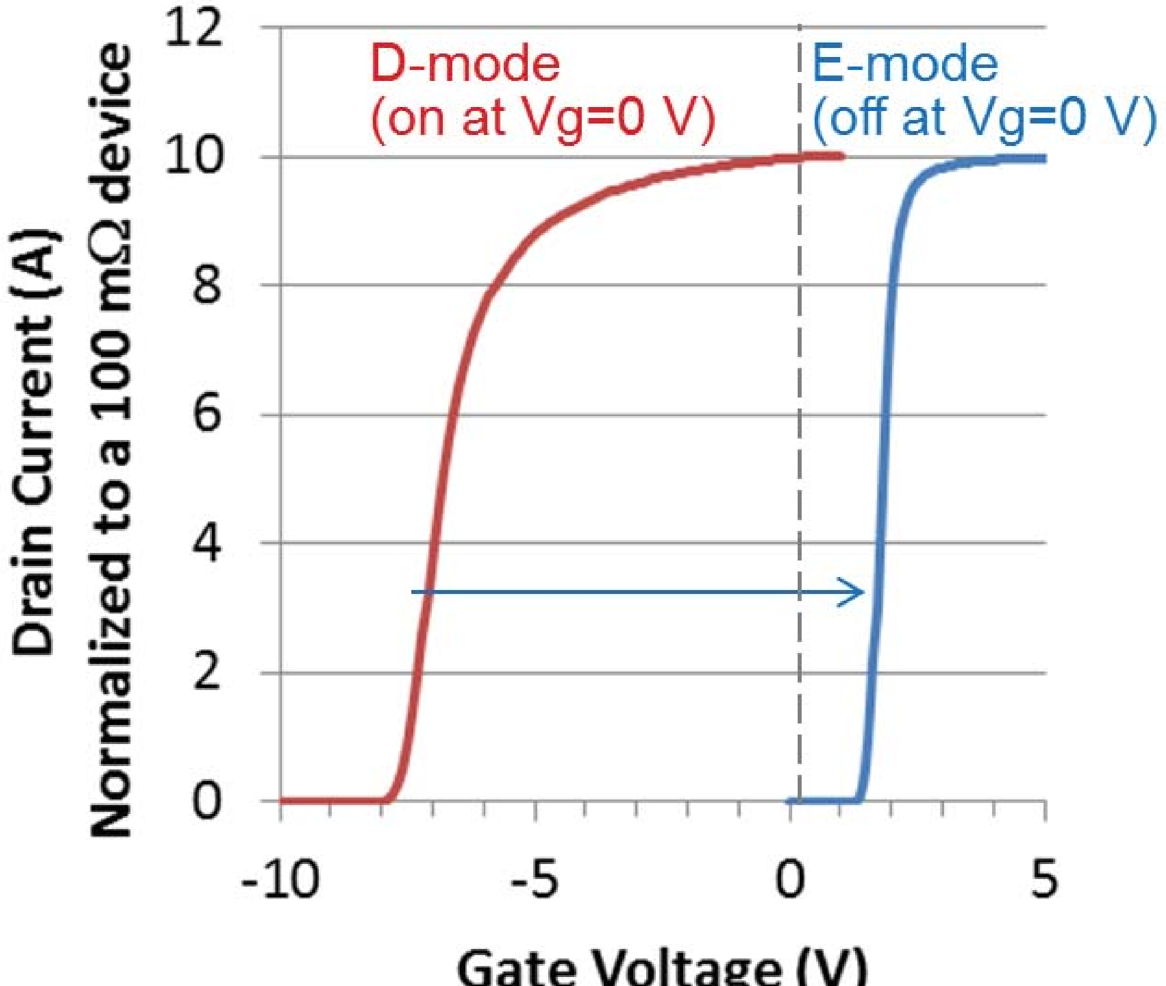
- Lateral device structure
- 2D Electron Gas layer significantly lowers RDSON

GaN construction



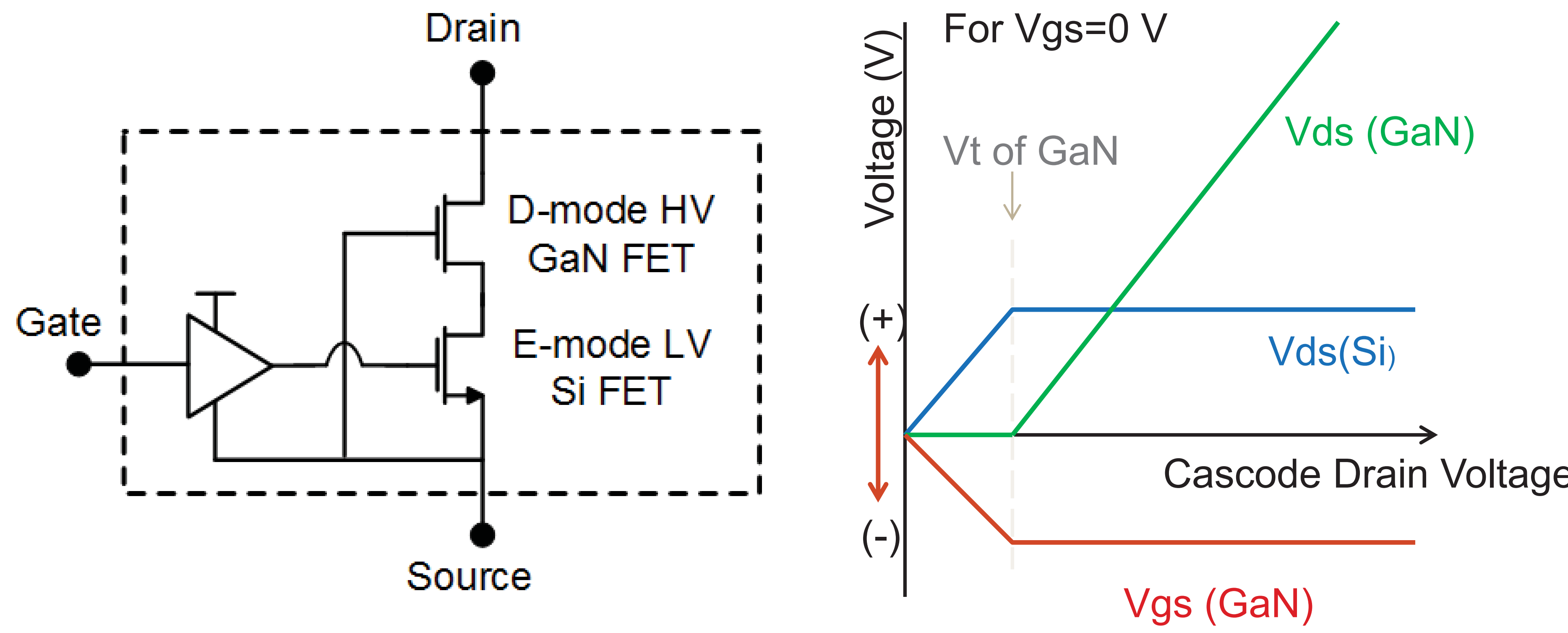
- Normally OFF devices are important in power electronics for safety

GaN High Electron Mobility Transistor



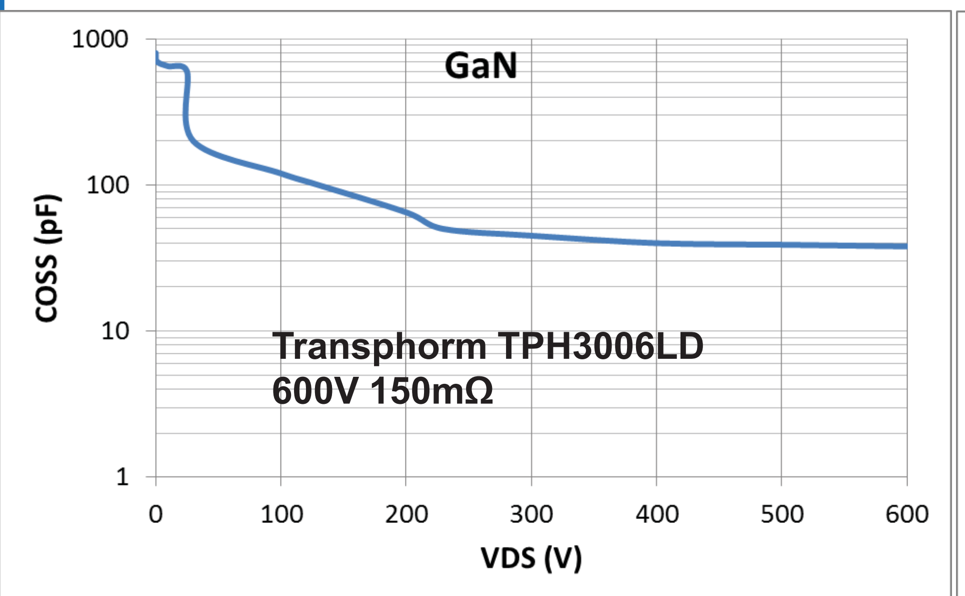
- Normally OFF devices are important in power electronics for safety

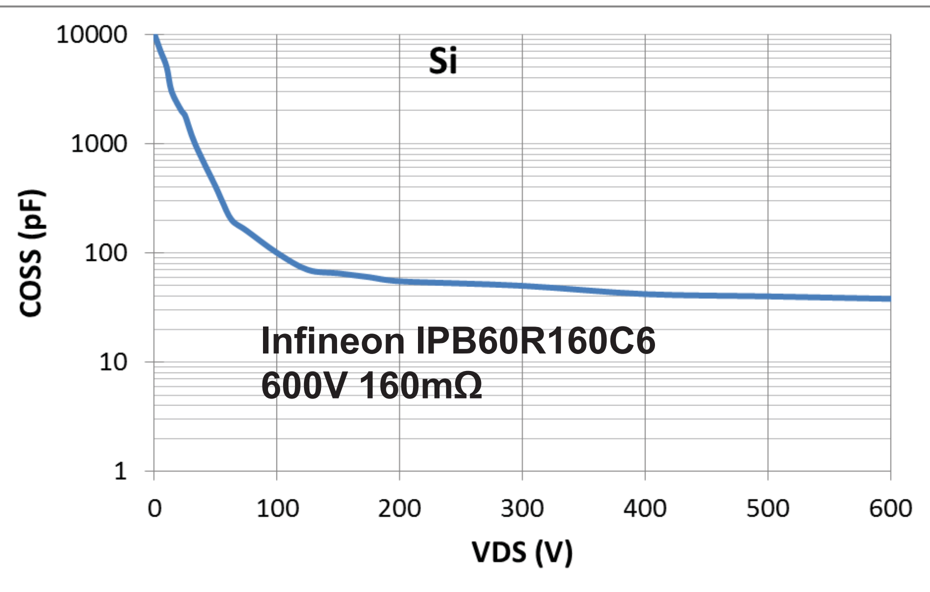
E-mode by cascoding d-mode GaN + Si



- Si FET is used to switch the GaN FET ON/OFF
- GaN FET provides the voltage blocking capability while the Si FET sets the VT

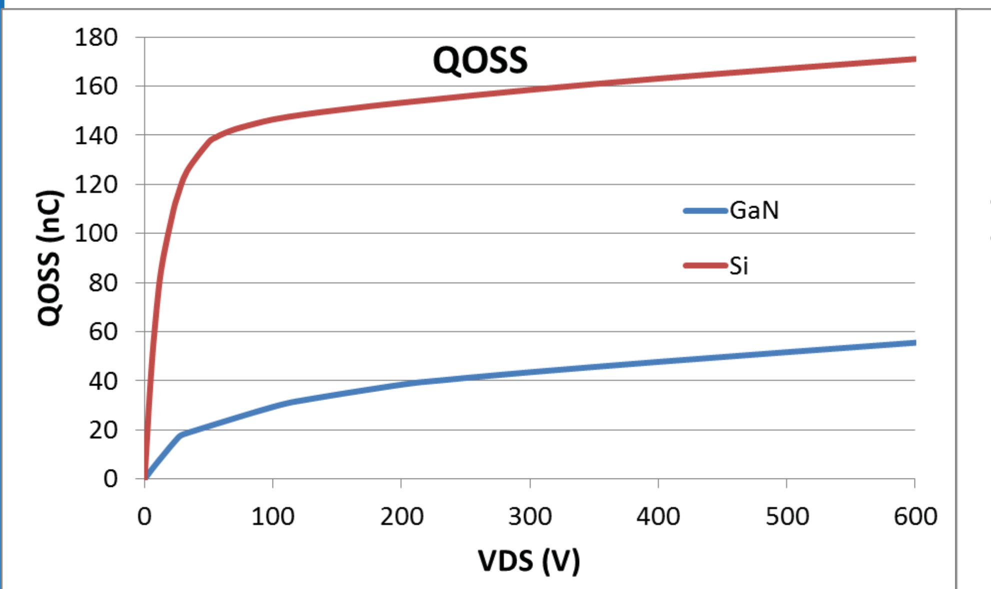
GaN vs Si - C_{OSS} comparison

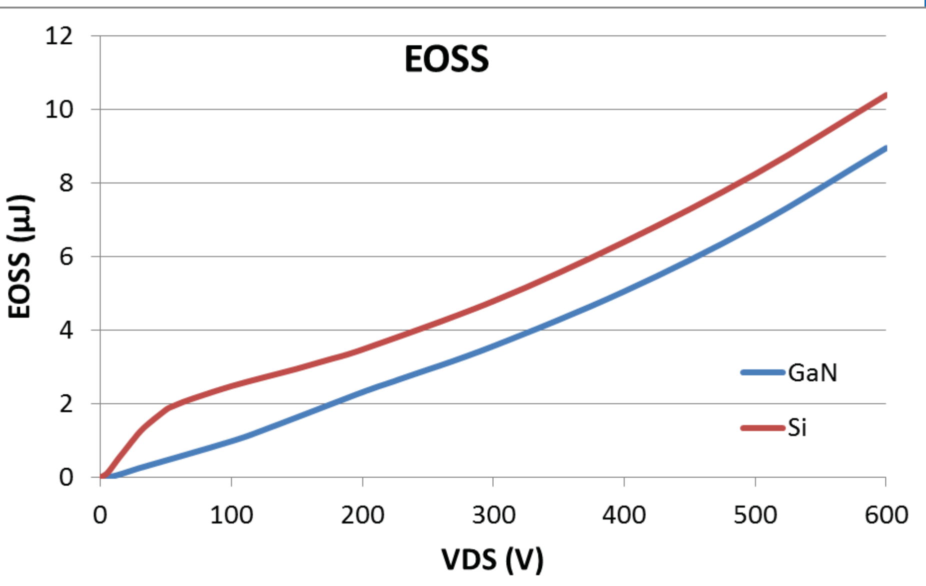




- 600V GaN and Si SJ FET comparison
- GaN output capacitance is significantly lower

GaN vs Si - Q_{OSS}, E_{OSS} comparison





- Significant Q_{OSS} benefits
- E_{OSS} benefit is smaller

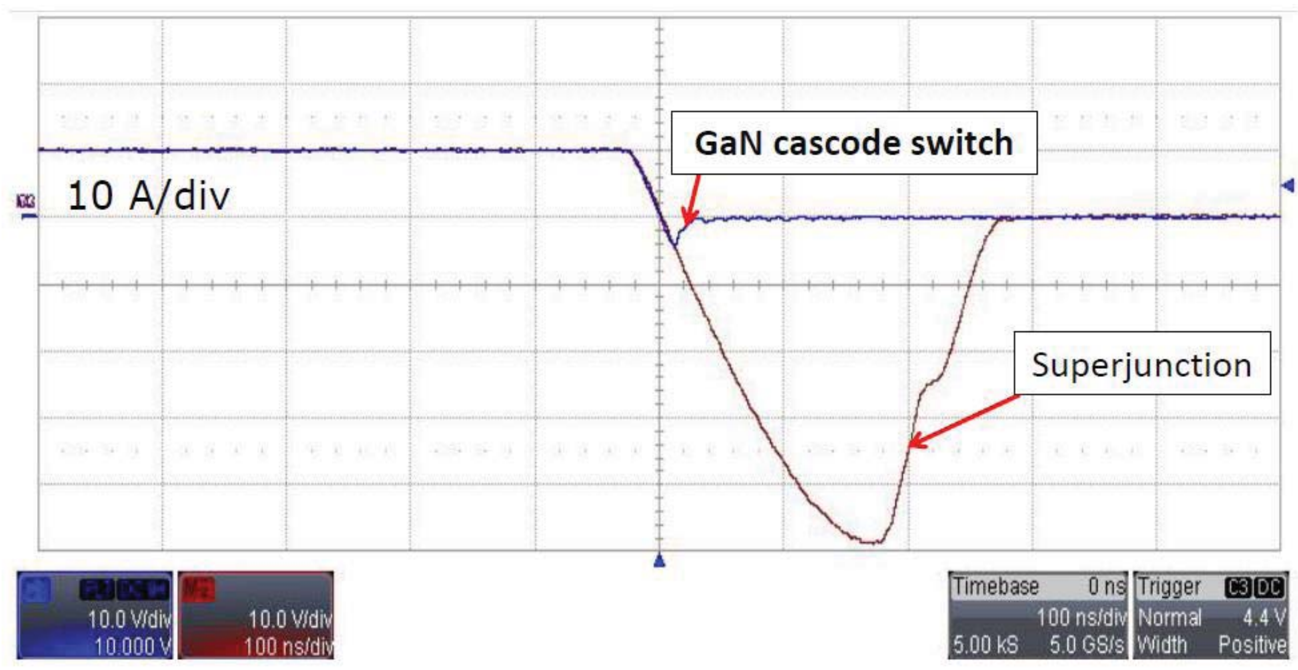
GaN vs Si - Q_{RR} comparison

GaN

t_{rr}	Reverse Recovery Time	-	30	-	ns	I_S=11 A, V_{DD}=480 V, di/dt =450 A/µs, T_J=25 °C
Q_{rr}	Reverse Recovery Charge	-	54	-	nC	

Si

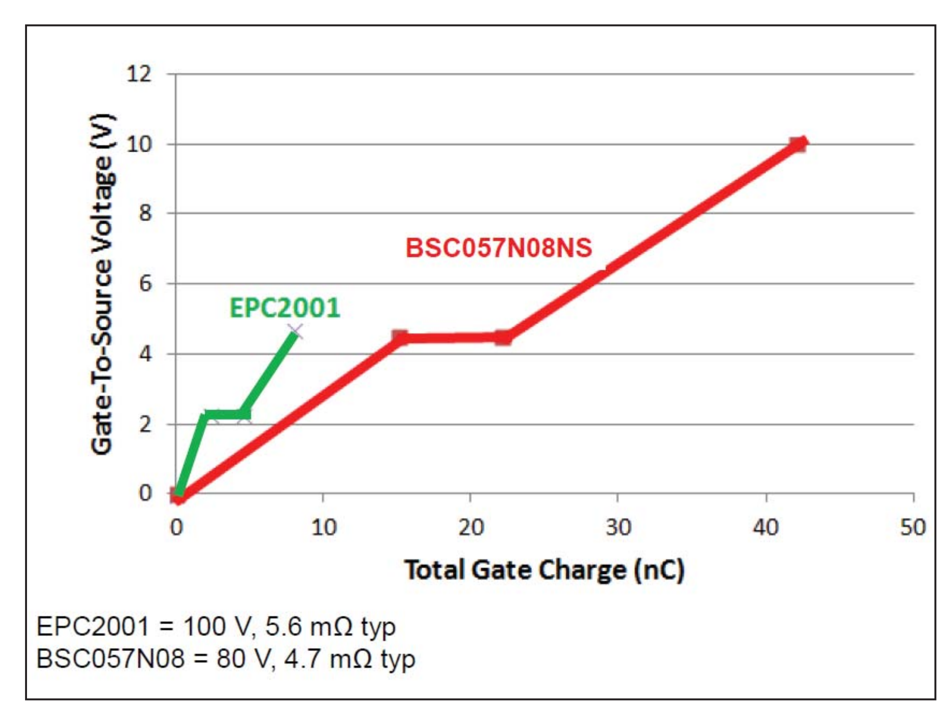
Reverse recovery time	t_{rr}	-	460	-	ns	V_R=400 V, I_F=11.3 A, di_F/dt=100 A/µs (see table 22)
Reverse recovery charge	Q_{rr}	-	8.2	-	µC	

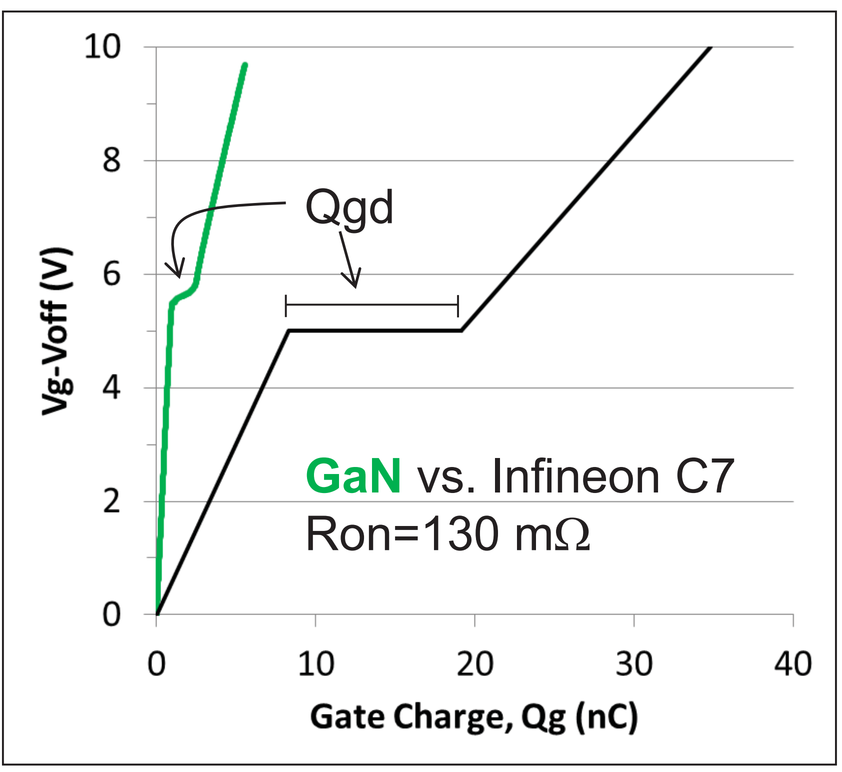


- Significantly lower Q_{RR} for GaN
- Lack of p-n diode prevents avalanche protection

E. Persson, APEC 2015

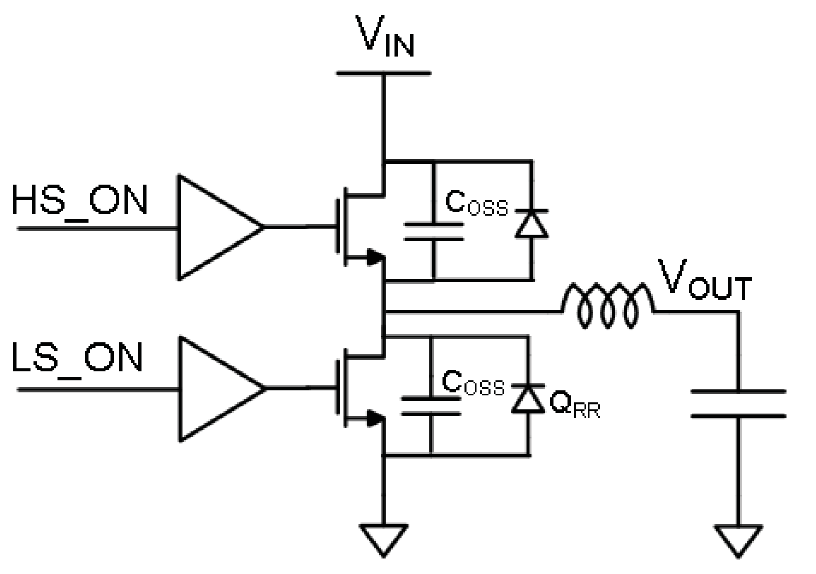
GaN vs Si - Q_G comparison





- Significant Q_G improvement in both 200V and 600V devices
- Lower Q_{GD} also leads to faster switching thereby reducing overlap losses

Benefits of GaN

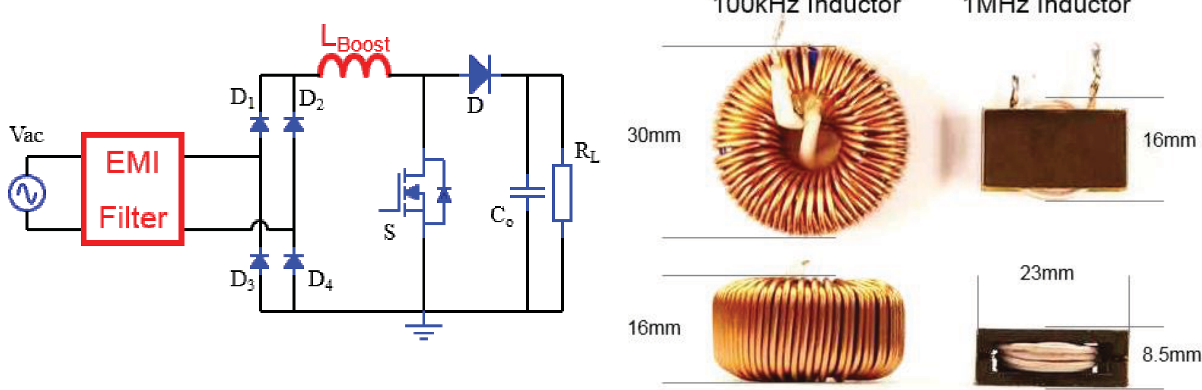


Hard-Switched Buck FET Losses

Conduction	$I_{rms}^2 R_{DS}$
Switching	$Q_{OSS} V_{IN} f_{SW}$
Reverse Recovery	$Q_{RR} V_{IN} f_{SW}$
Cross Conduction	$I_{L,AV} V_{IN} t_{ov} f_{SW}$
Gate Drive	$2\, Q_G V_{DRV} f_{SW}$

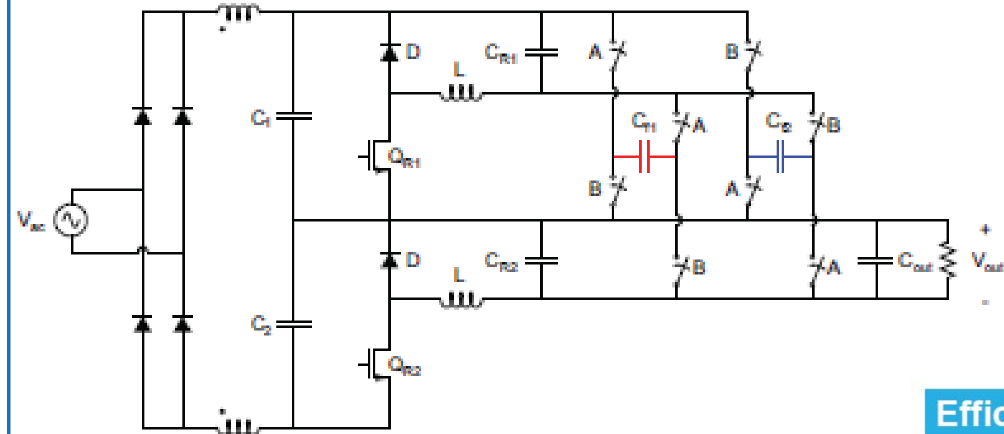
- Better FoM (Q_{OSS} * R_{DS})
- Low terminal capacitances (Q_{OSS}, Q_G)
- No reverse recovery (Q_{RR})
- Lower Q_{GD} → faster switching (low t_{ov})
- High frequency operation → lower passive volume

Size improvement with frequency

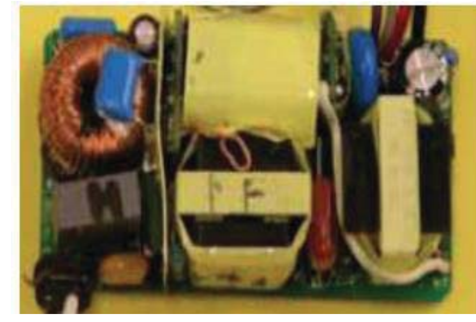


c. CPES, Virginia Tech, April 2014

	100kHz Inductor	1MHz Inductor	Ratio
Volume	14.4cm³	3.1cm³	21.5%
Weight	44.2g	9.0g	20.4%



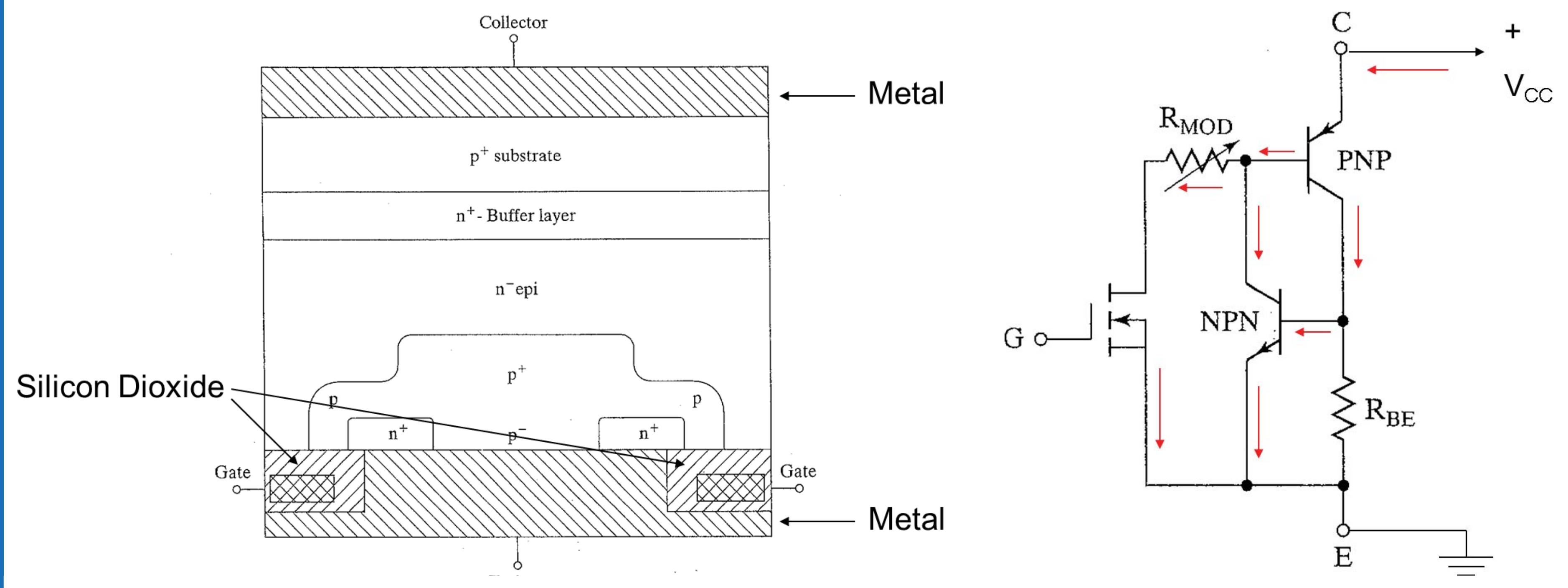
c. S. Lim, APEC 2014



- EMI filter size reduction
- New topologies enabled

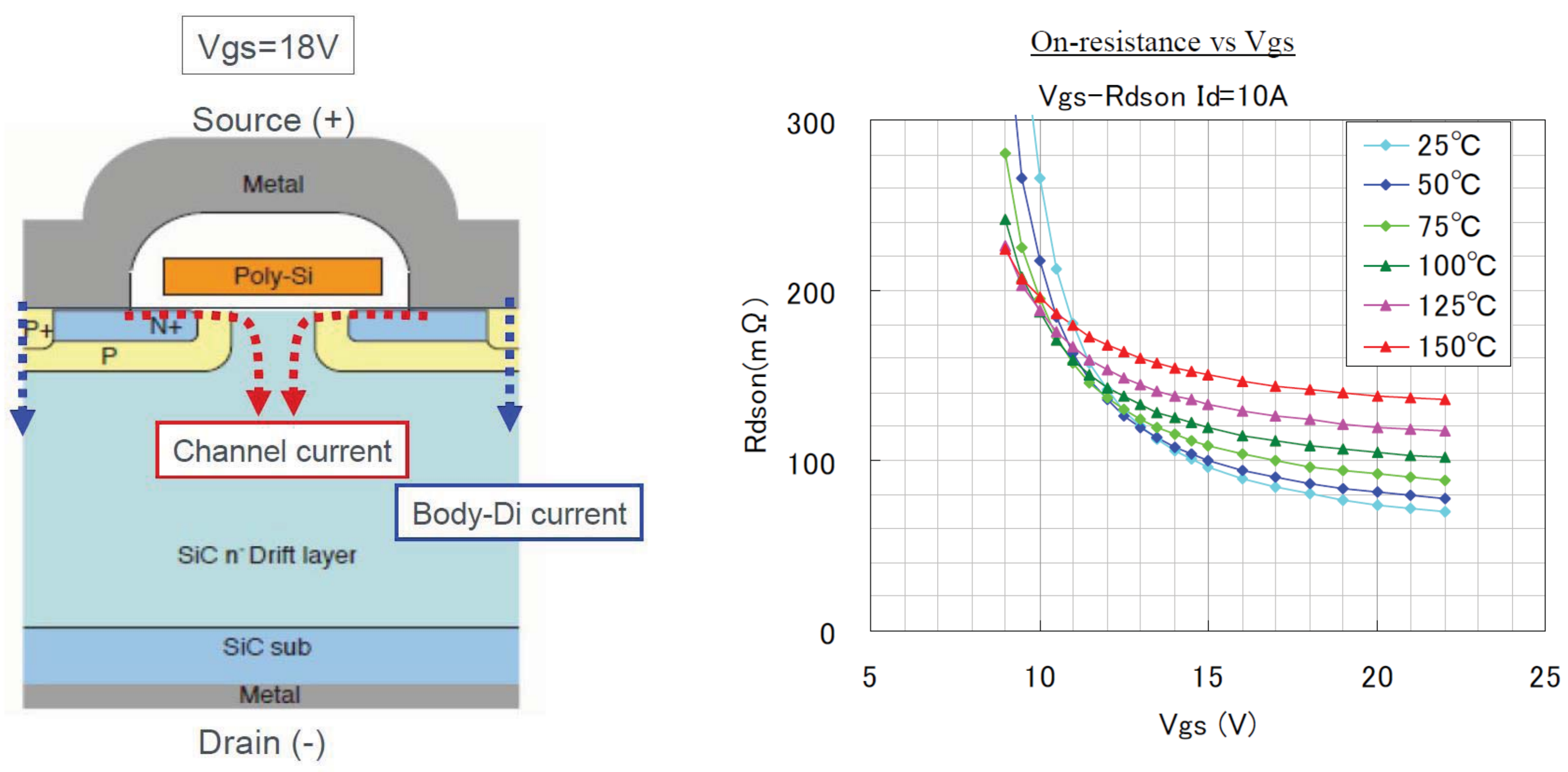
	Commercial	PowerChip
Efficiency	64 - 83 %	93 %
Switching Frequency	57 - 104 kHz	5-10 MHz
Power Factor	0.73-0.93	0.89
Power Density	< 5 W/in³	> 50 W/in³

IGBT



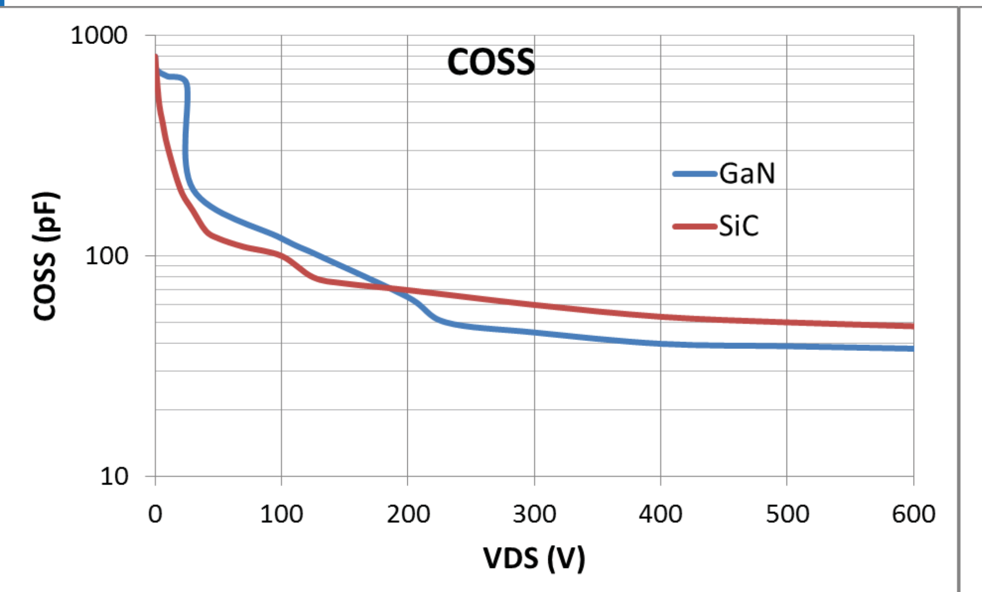
- Used for voltages greater than 1000V
- Behaves like a bipolar controlled through a gate
- Can carry very large currents at slow switching speeds

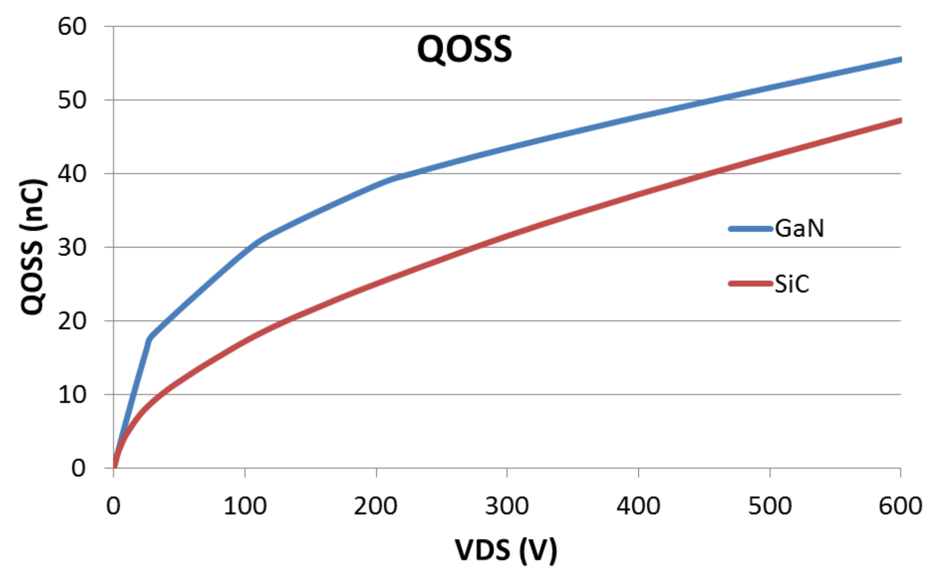
SiC construction



- High voltage, high temperature capable device
- Capable of reduced switching losses leading to more power dense solutions

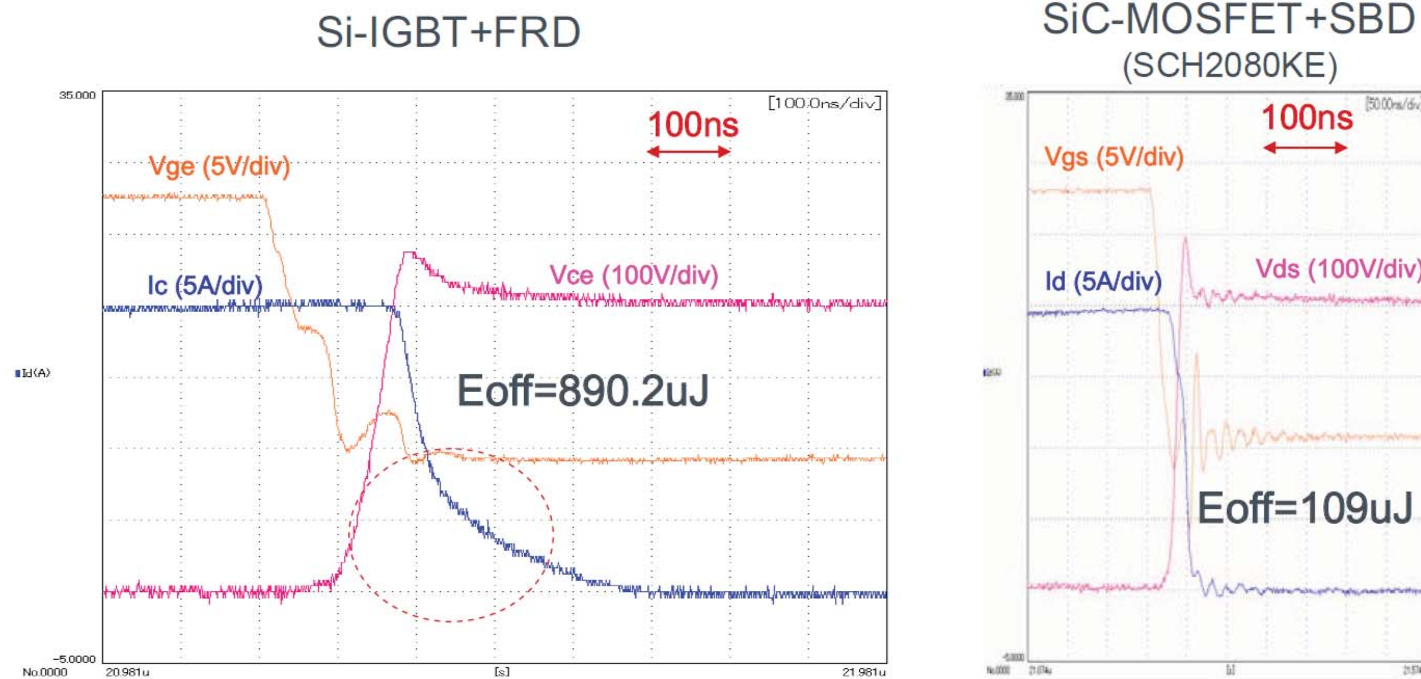
GaN vs SiC - C_{OSS}, Q_{OSS} comparison





- 1200V, 160mΩ CREE CPM2-1200-0160B SiC device
- C_{OSS} and Q_{OSS} comparable to 600V GaN device of similar $R_{DS,ON}$

Switching Loss Comparison

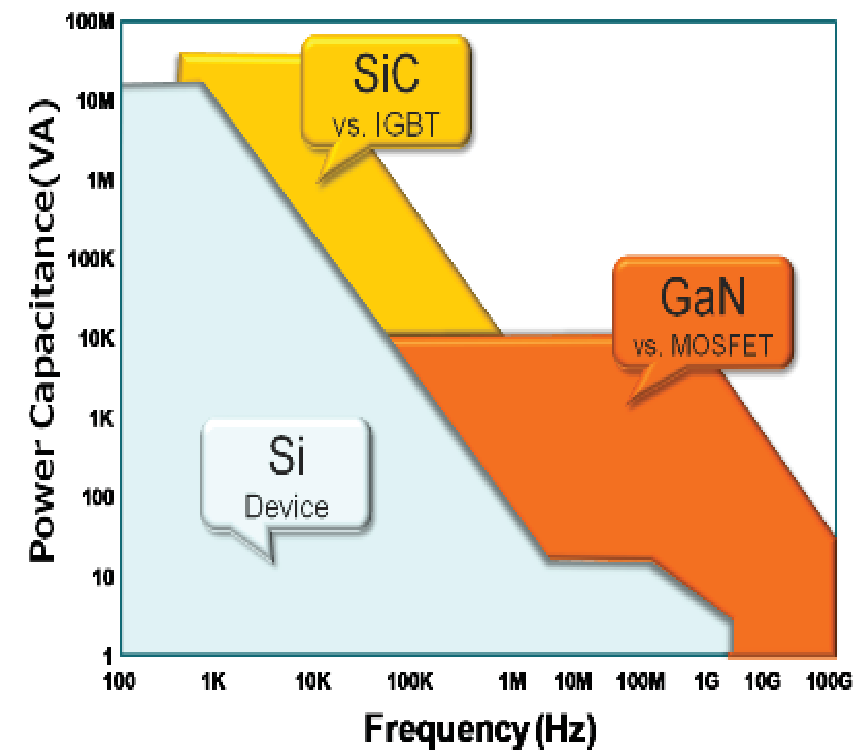


c. ROHM "SiC Power Devices and Modules", Application Note

- SiC versus Si IGBTs -- 90% lower switching losses
- Enables 3X frequency increase
- Rds on vs Temp only 20% increase

WBG Value Propositions

- Si SJ (500V - 900V)
  - Proven Reliability
  - Robust operation
  - Low Cost
  - High Q_{OSS} and Q_{RR}
- Si IGBT (1kV – 6kV)
  - Reliable, high temp operation
  - Very Low Cost
  - High switching losses
- GaN on Si (40V – 600V)
  - Extremely fast switching
  - Low terminal capacitance
  - Moderate cost
  - Reliability concerns, Lateral device



- SiC (600V – 6kV)
  - High power, high temp operation
  - Very good thermals
  - Low Q_{RR} and switching losses
  - Expensive

Outline

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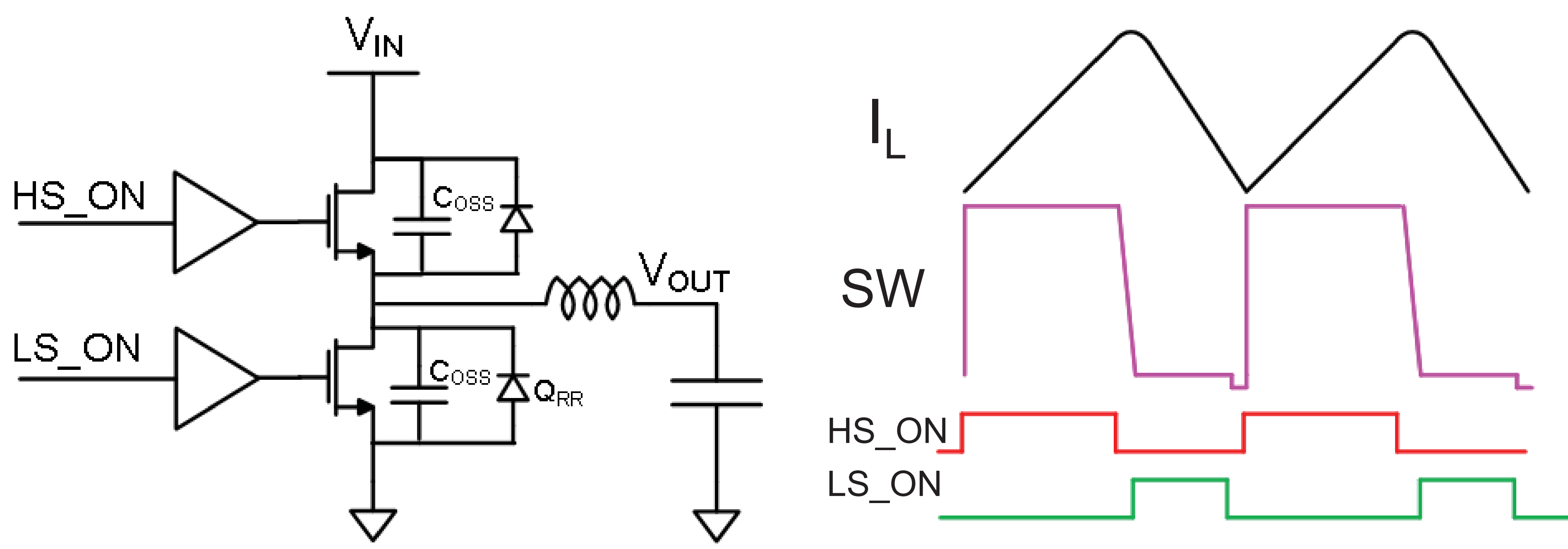
Buck converter switch related losses



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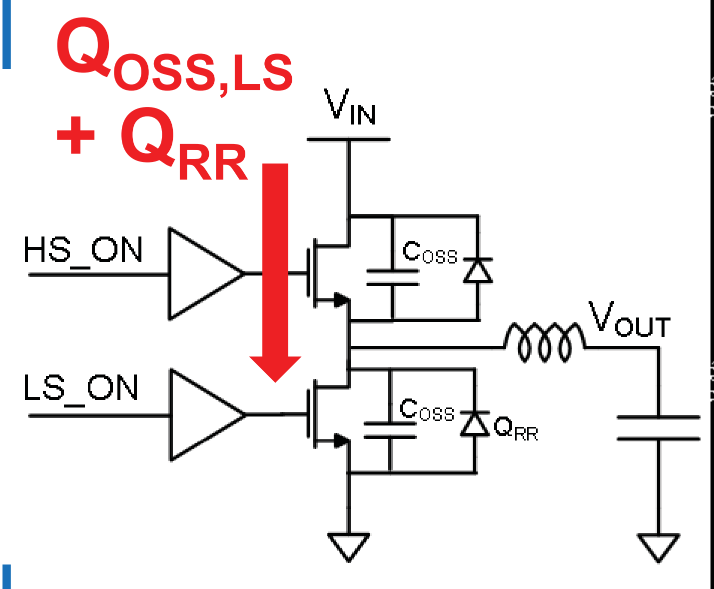
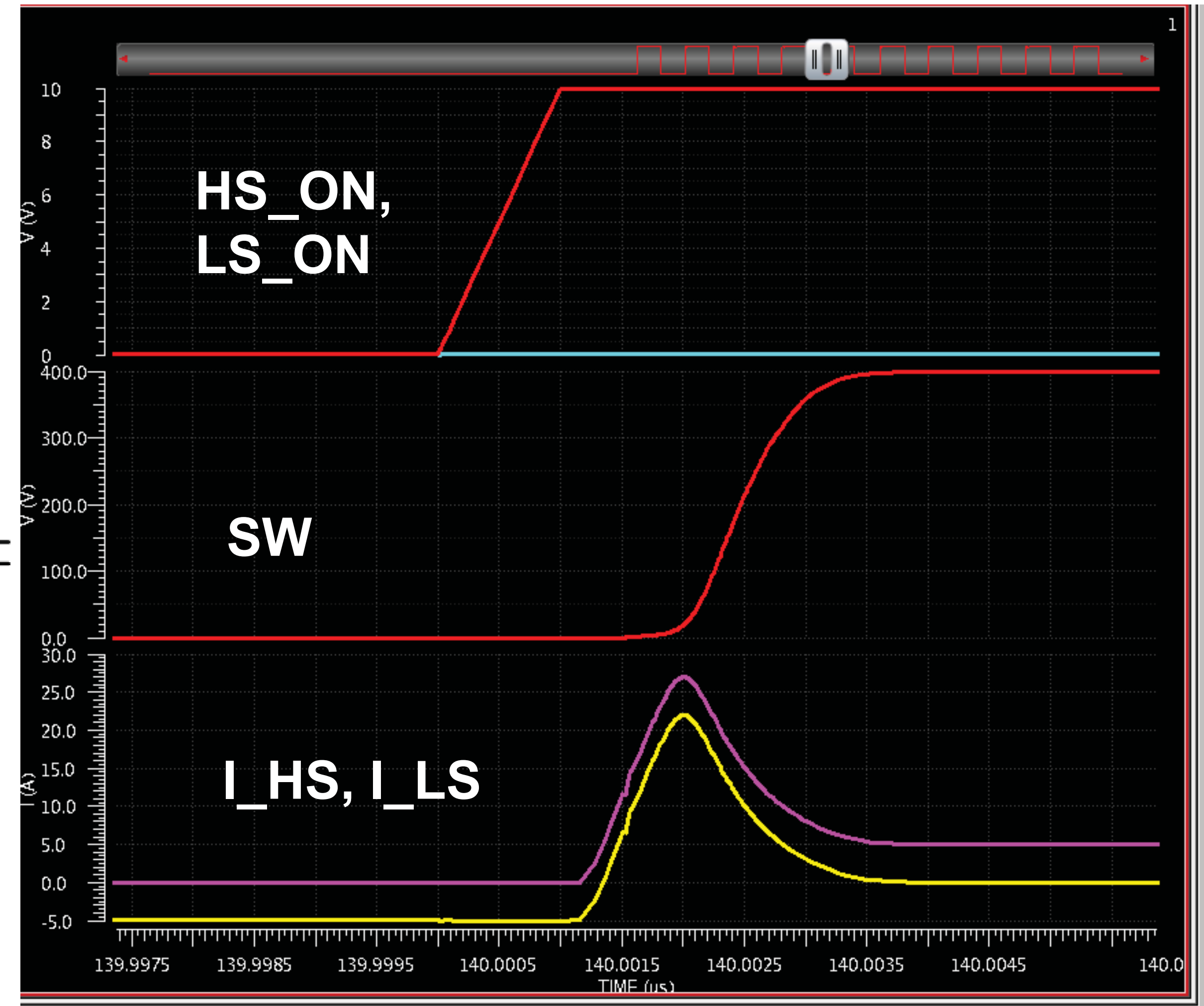
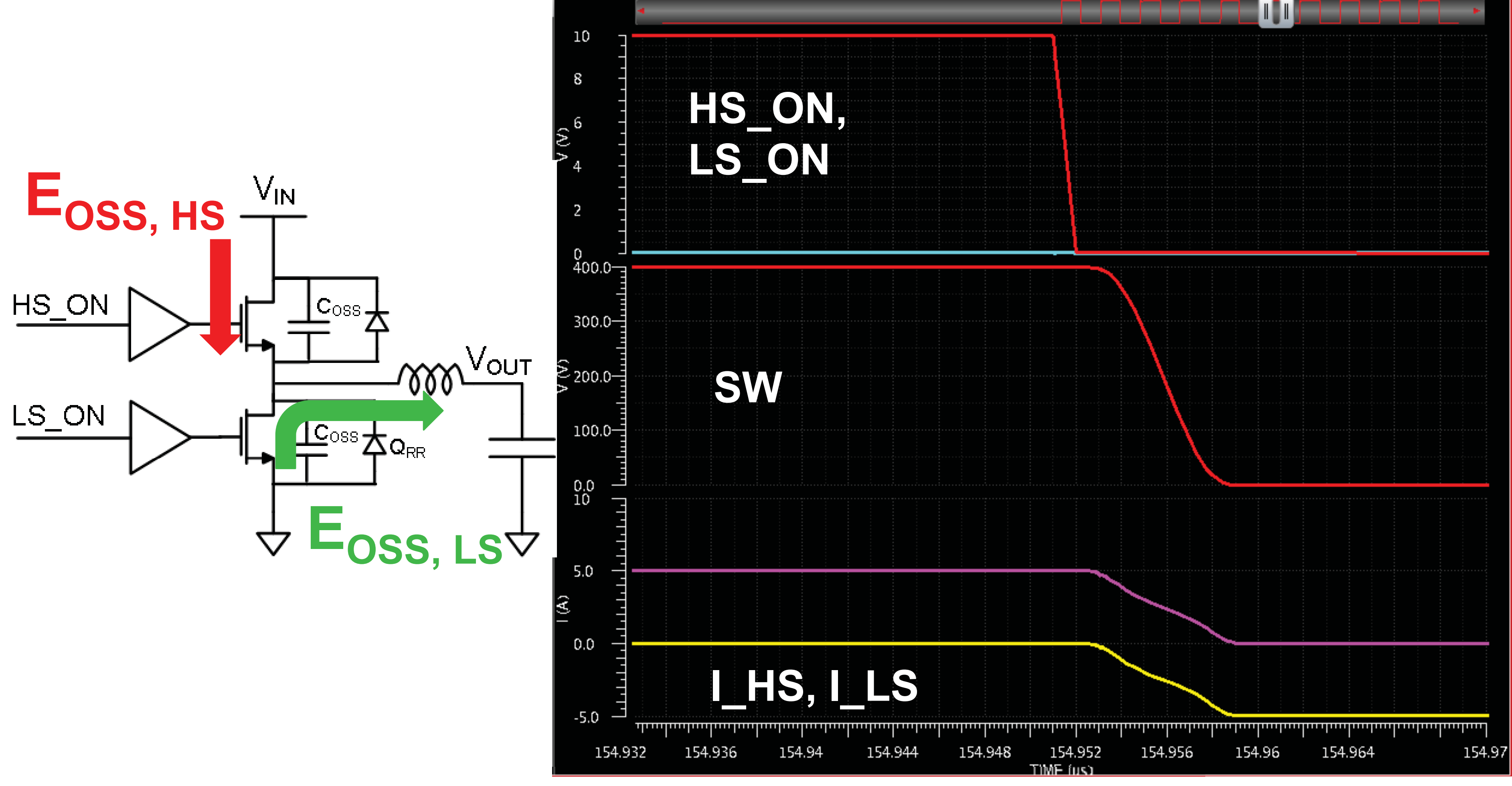
HS Turn ON





$$Energy\ from\ V_{IN} = (Q_{RR} + Q_{OSS\ LS}) \times V_{IN}$$

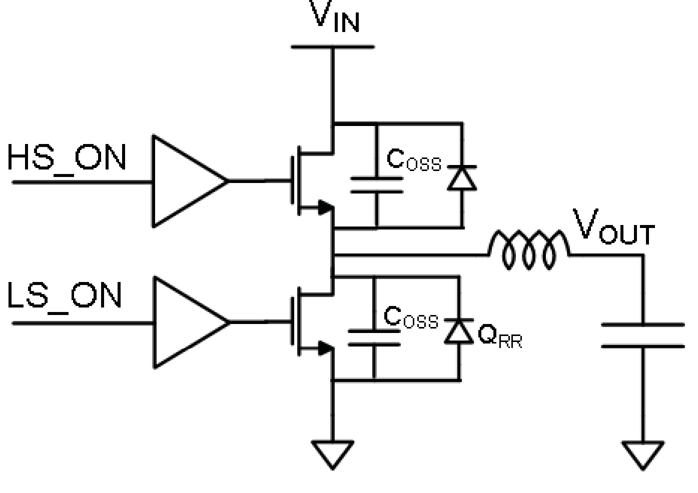
HS Turn OFF

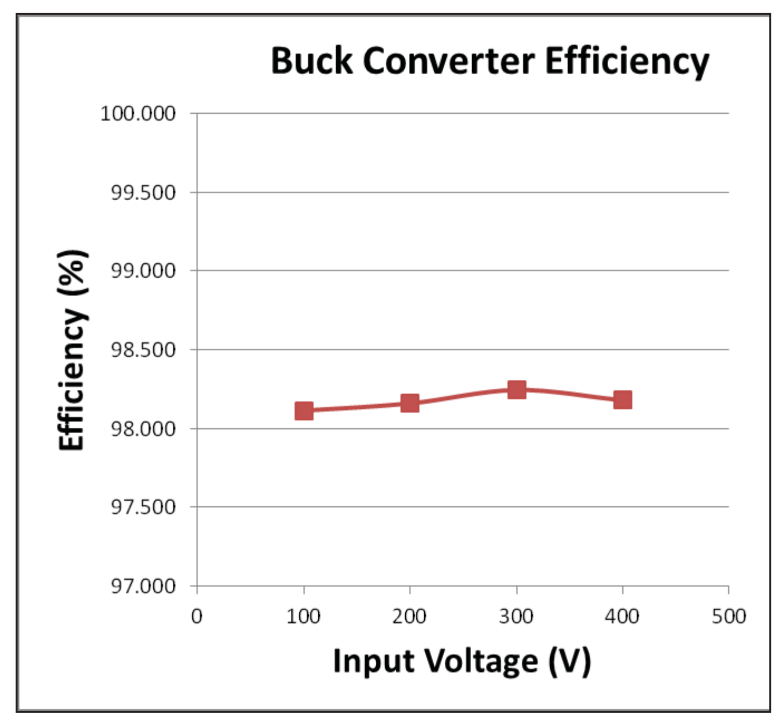


$$Energy\ from\ V_{IN} = E_{OSS\ HS}$$

$$Energy\ to\ V_{OUT} = E_{OSS,\ LS}$$

100kHz Hard-switched buck converter





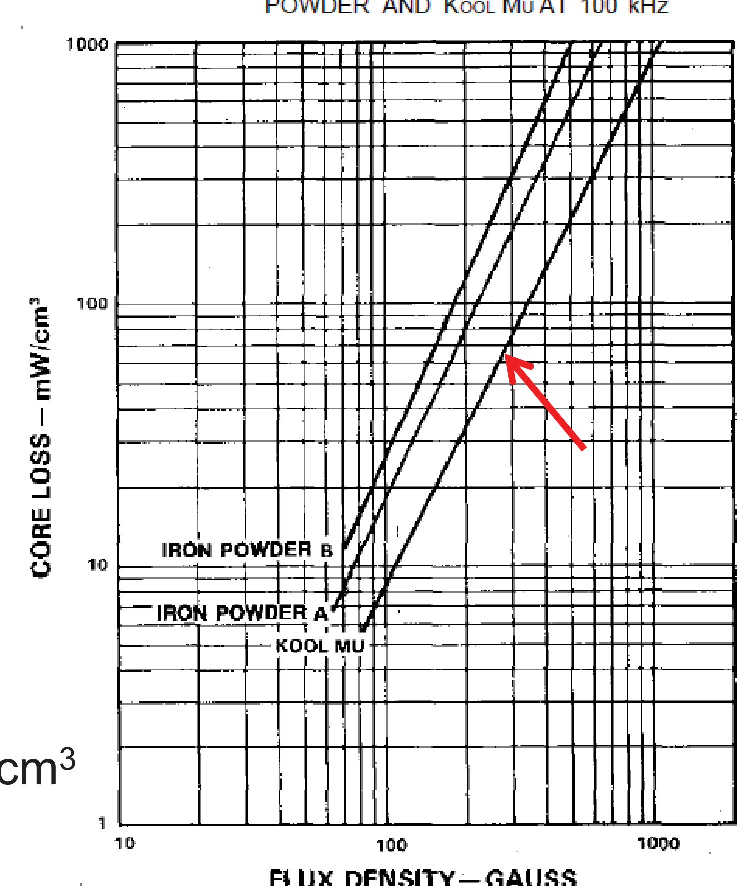
- L = 750µH
- Rind = 0.17Ω
- Ipeak = 3.4A
- Ivalley = 2.1A

Loss breakdown (calculations)

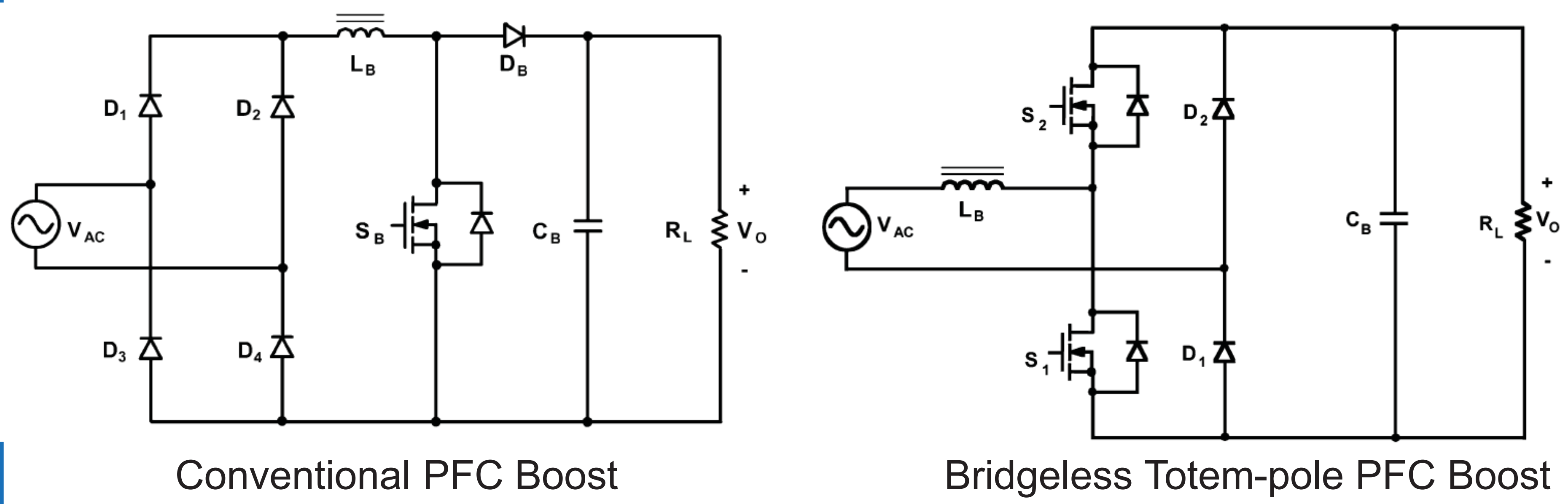
- HS_cond: (Iav^2+ΔI^2/3)*RHS/2 = 7.7*.152/2 = 0.6W
- LS_cond: (Iav^2+ΔI^2/3)*RLS/2 = 7.7*.152/2 = 0.6W
- HS_switching: Qoss*VBUS*fsw = 40e-9*400*100e3 =1.6W
- HS_overlap: Ivalley*VBUS*tr*fsw = 2.1*400*8e-9*100e3 = 0.67W
- LS_deadtime: Iav*Vdiode*tdead*2*fsw = 2.75*4.5*200e-9*100e3 = 0.24W
- IND_winding: (Iav^2+ΔI^2/3)*RIND = 7.7 * 0.17 = 1.31W
- IND_core: (see next page) = 2.9W
- Total Loss = 8W
- If a 600V Si power FET was used (QRR = 700nC), then reverse recovery loss due to body diode: QRR*VBUS*fsw = 0.7e-6*400*100e3 = 28W

Inductor core loss

- IND is obtained by winding 45 turns on 2 Magnetics 0077071A7 Kool Mu cores
- Core mean length (lm) = 8.33cm
- Cross-section area (A) = 1.64cm2
- Bmax = μ*n*Ipeak/lm
  = 60*4π*1e-7*45*3.4/8.33e-2 = 0.138T
- Bmin = μ*n*Ivalley/lm
  = 60*4π*1e-7*45*2.1/8.33e-2 = 0.086T
- ΔBpeak = (1380 – 860) / 2 = 260Gauss
- From core loss curve at 100kHz, Loss = 70mW / cm^3
- Total core loss = 70m*3*13.66 = 2.9W



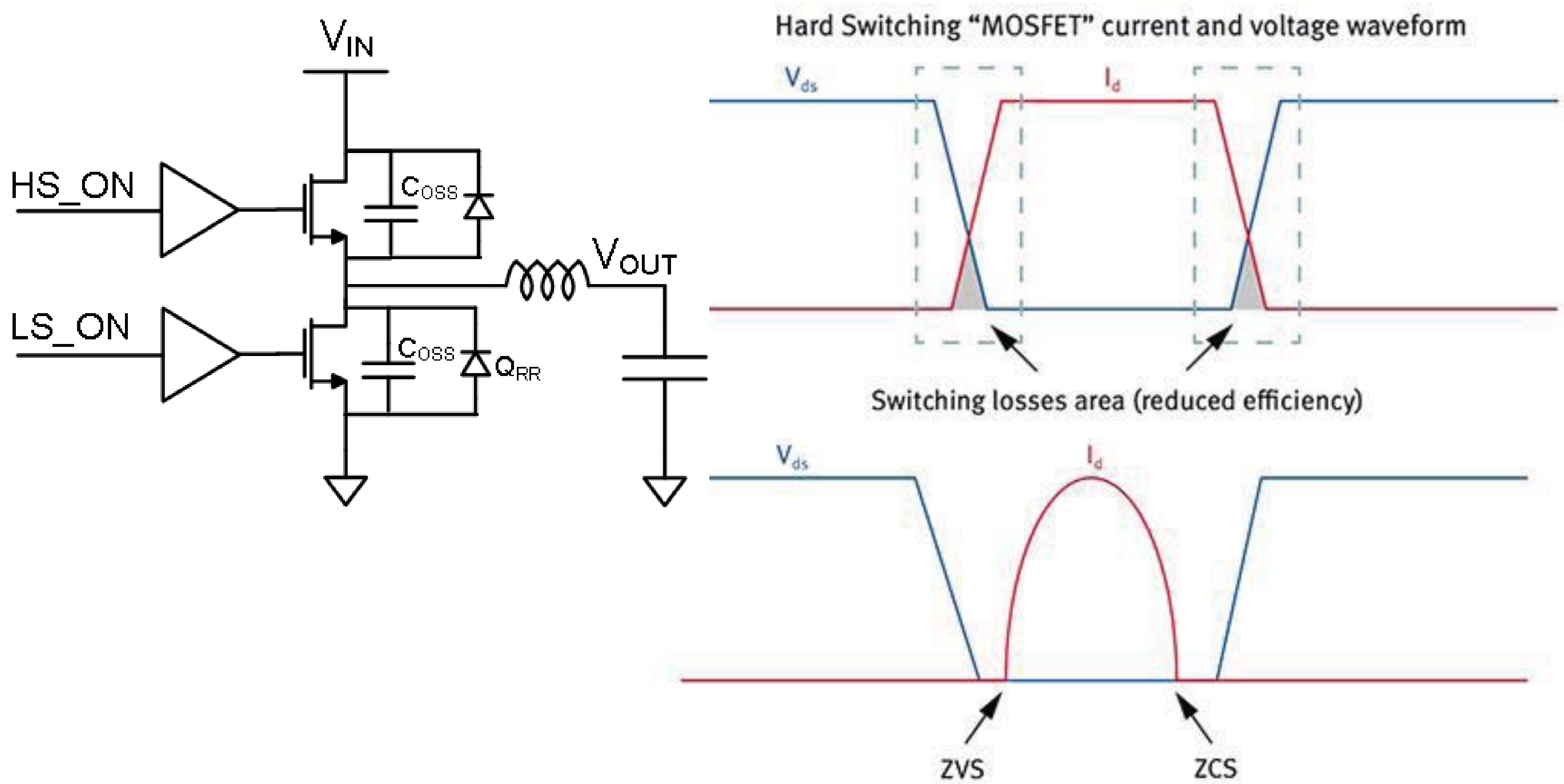
Boost PFC



L. Huber et. al, "Performance Evaluation of Bridgeless PFC Boost Rectifiers,"
IEEE TRANSACTIONS ON POWER ELECTRONICS, MAY 2008

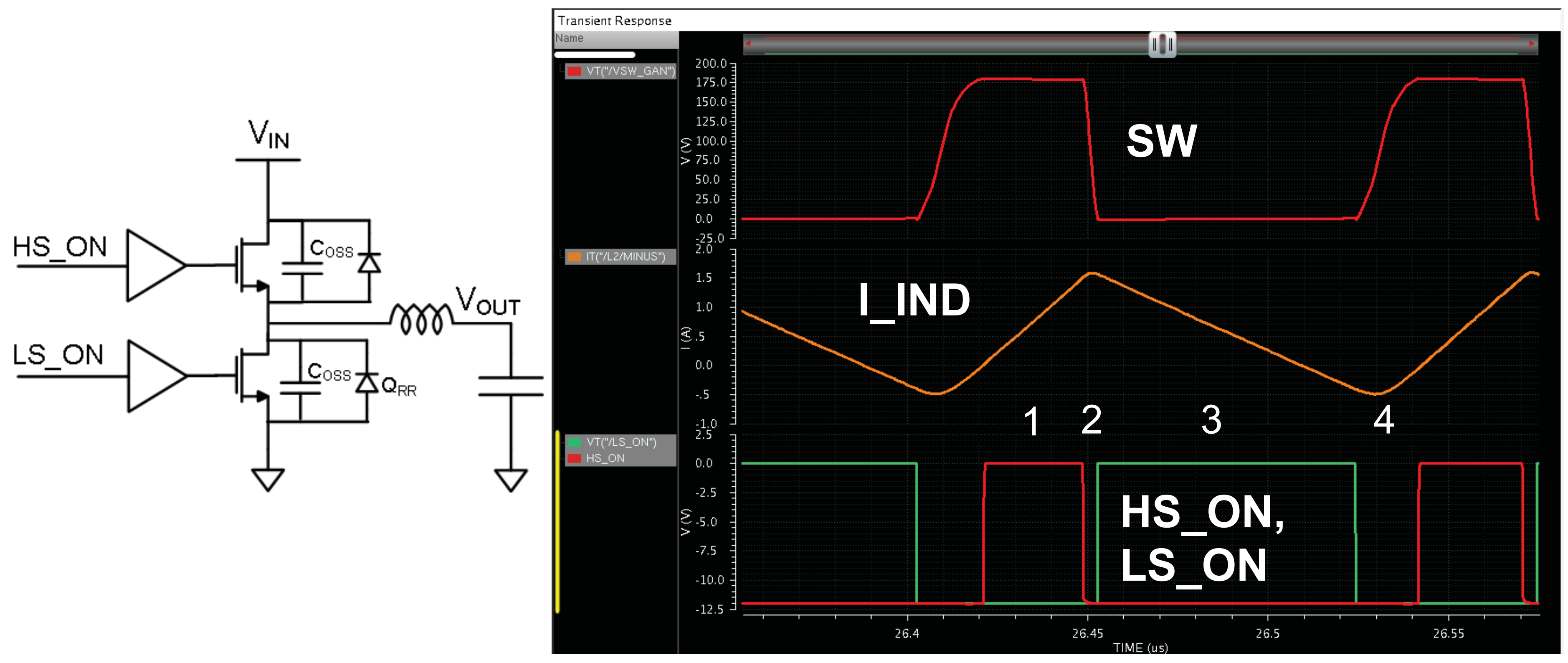
- Universal line input power supplies handling above 75W are required to have power factor correction (IEC61000-3-2 standard)
- 1-2% efficiency loss due to input bridge
- Totem-pole bridgeless topology requires good hard-switching performance for high efficiency

Soft-switching



- Voltage across switch or current through switch brought to zero before switch transition

Quasi Resonant buck



1. HS ON : Inductor current gets ramped up to peak current
2. SW OFF : Inductor current softly discharges LS C_{oss} and softly charges HS C_{oss}. Remain in this state till VSW reaches 0V
3. LS ON : Inductor current gets ramped down to valley current
4. SW OFF : Inductor current softly charges LS C_{oss} and softly discharges HS C_{oss}. Remain in this state till inductor current reaches 0

Efficiency breakdown of QR-buck

- Net loss due to C_{oss} is close to 0 and there is no overlap or reverse recovery losses
- Loss mechanisms:

$$P_{cond} = {I_{rms}}^2 \times RDS_{ON}$$

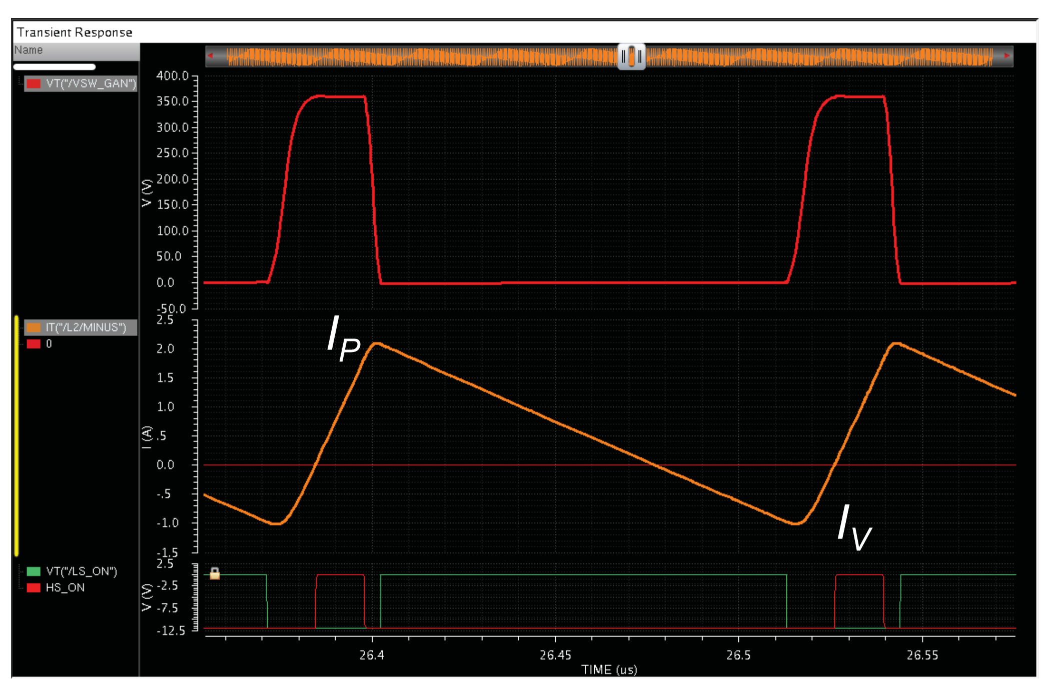
$$P_{L,copper} = {I_{rms}}^2 \times RIND_{DC} + {I_{AC}}^2 \times RIND_{AC}$$

$$P_{L,core} = a \times {B_{pk}}^b \times {f_{sw}}^c$$ (B_{pk} is proportional to $I_{L,\ pk\text{-}pk}$)

$$P_{GD} = 2 \times Q_G \times V_{GS} \times f_{sw}$$

- Other than gate-drive loss, the other losses are a function of I_{rms} or $I_{pk\text{-}pk}$
- How does Q_{oss} affect these parameters?

How Q_{oss} affects efficiency



$$I_{LOAD} \sim \frac{I_P + I_V}{2}$$

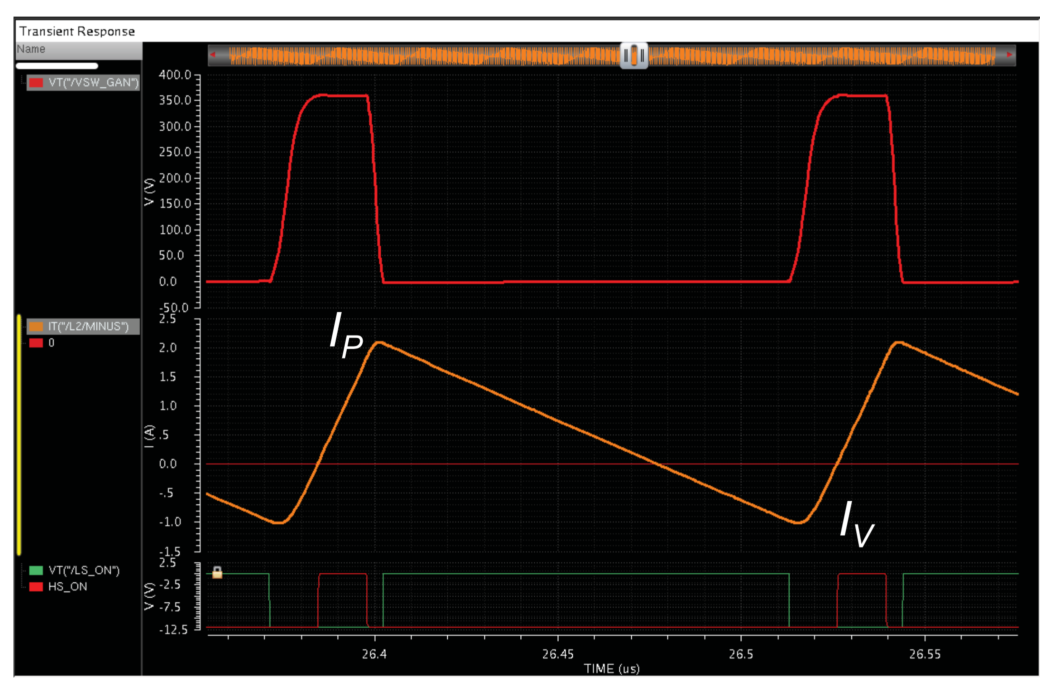
$$I_{pk-pk} \sim 2 \times (I_{LOAD} - I_V)$$

$$I_{rms} \sim \sqrt{\frac{4{I_{LOAD}}^2 - I_P I_V}{3}}$$

$$= \sqrt{\frac{4{I_{LOAD}}^2 + {I_V}^2 + 2 I_{LOAD} I_V}{3}}$$

- The inductor current needs to reverse to build enough energy in the inductor to charge HS and LS C_{OSS}
- Energy in system when inductor current begins reversing = E_{oss} (HS)
- Energy delivered to switches and input during negative inductor current = Q_{oss} (HS)* V_{IN} + E_{oss} (LS)
- Energy drawn from load ~ k * L * I_V^2

How Q_{oss} affects efficiency



$$I_{pk-pk} \sim 2 \times (I_{LOAD} - I_V)$$

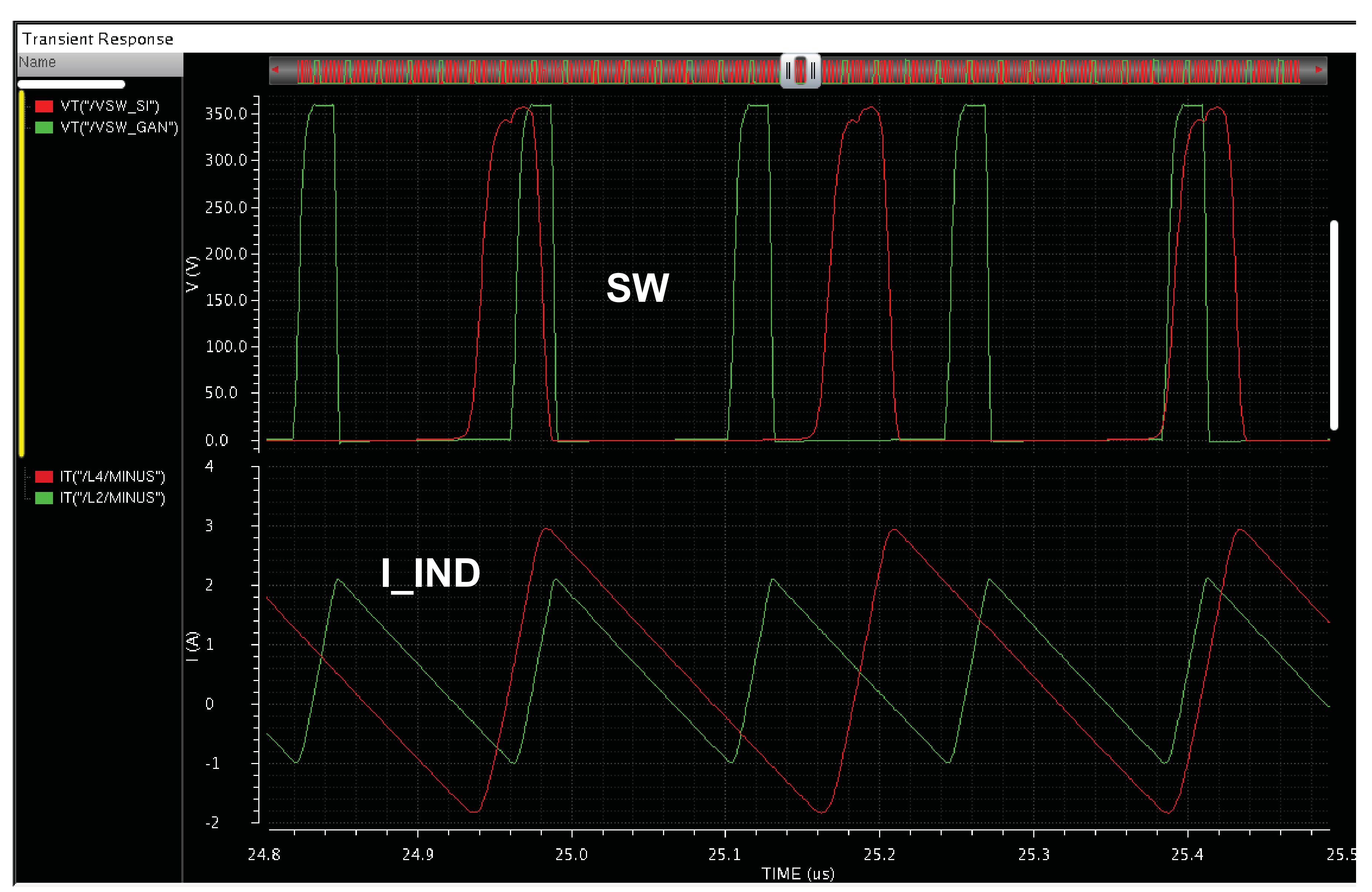
$$I_{rms} = \sqrt{\frac{4I_{LOAD}^2 + I_V^2 + 2I_{LOAD}I_V}{3}}$$

$$kLI_V^2 = Q_{oss,\,HS} \times V_{IN} + E_{oss} - E_{oss}$$

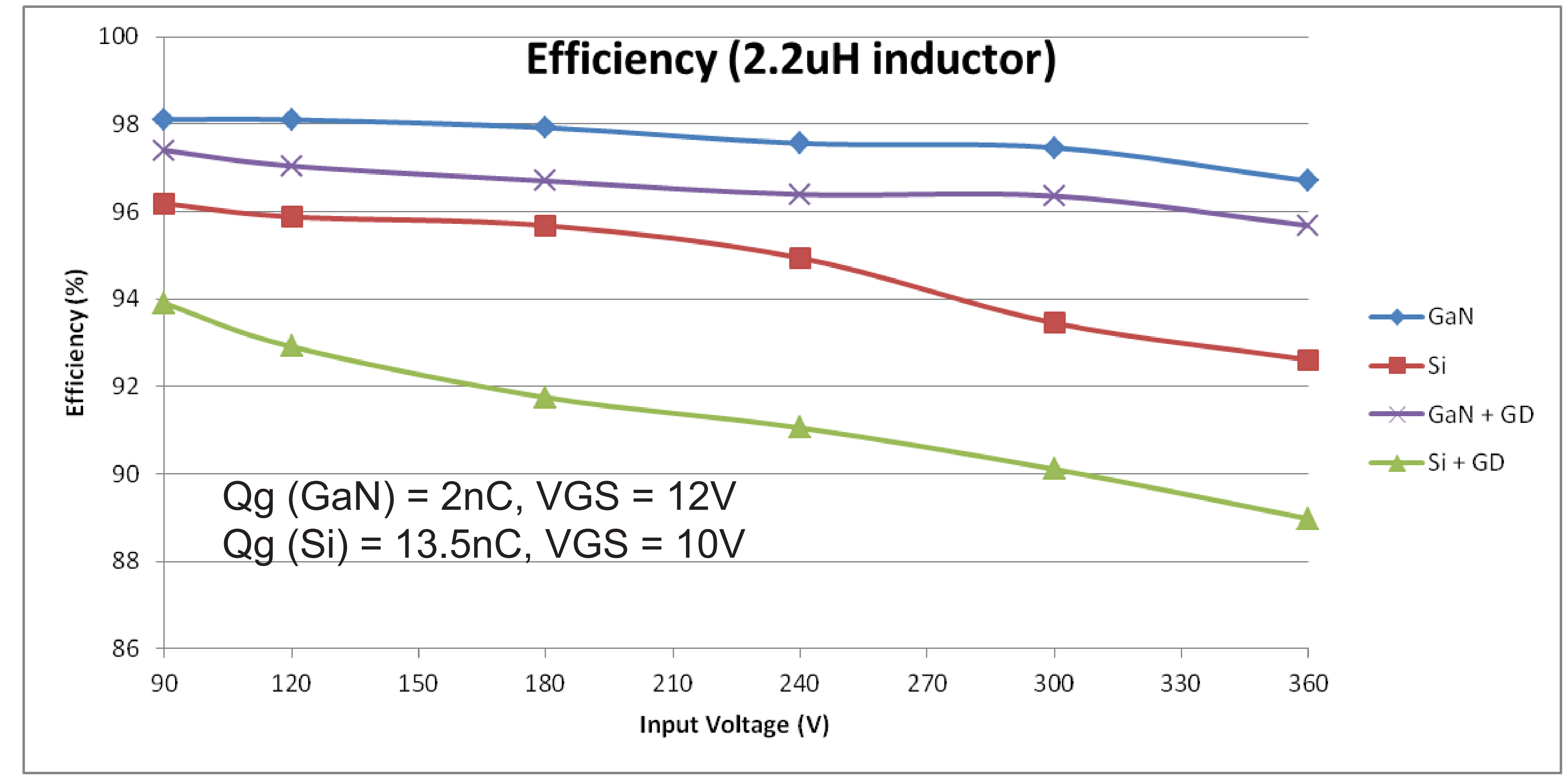
$$I_V = -\sqrt{\frac{Q_{oss,HS} \times V_{IN}}{kL}}$$

- High Q_{oss}, high V_{IN} and low inductance (higher f_{sw}) lead to a higher I_V
- A higher value of I_V directly increases the total I_{rms} and $I_{pk\text{-}pk}$
- Q_{oss} is the important metric, not E_{oss}
- The effect of Q_{oss} diminshes at higher I_{LOAD}

Switching waveforms

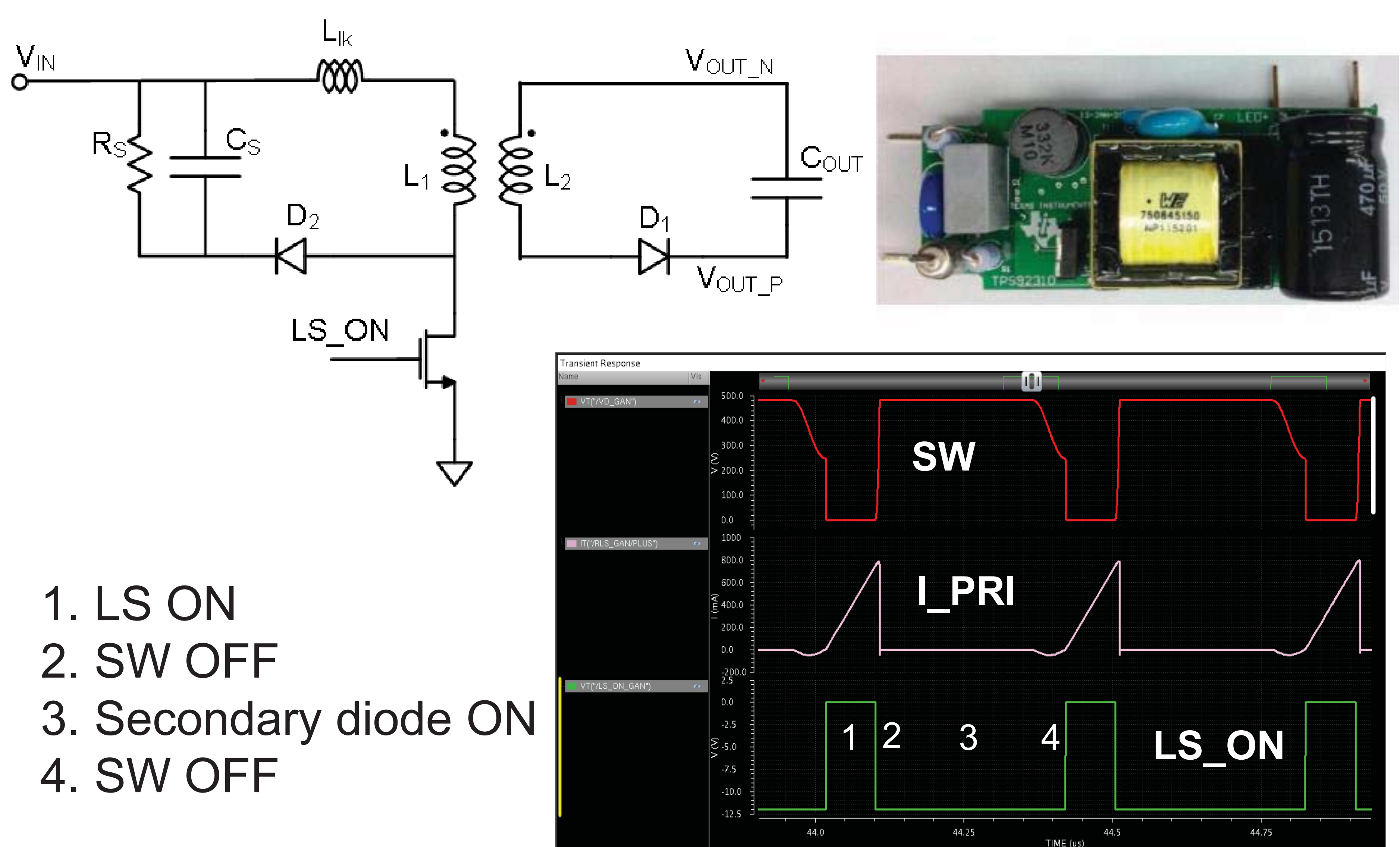


Efficiency Comparison

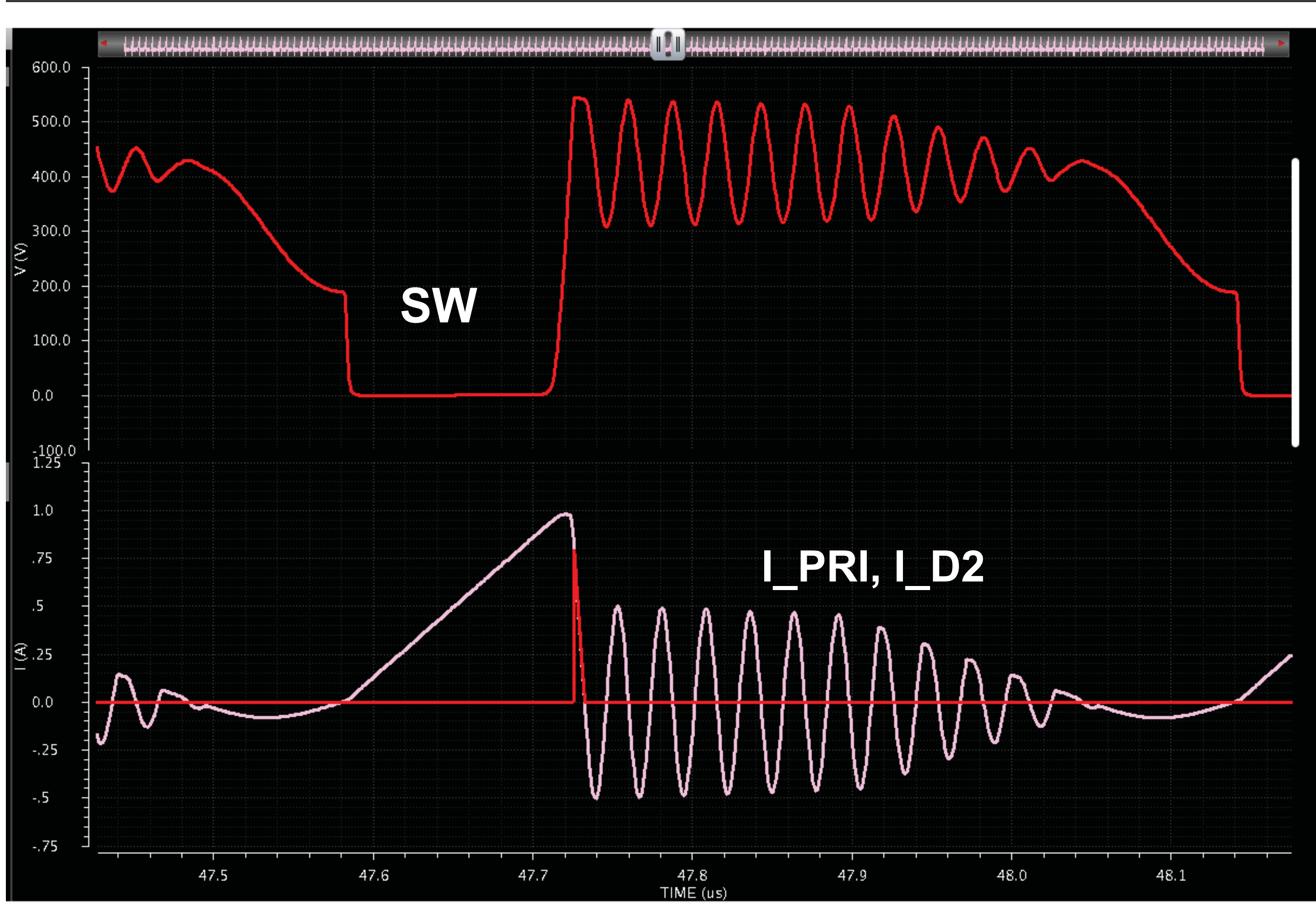


- High frequency, high efficiency topology
- Efficiency benefits in using GaN devices
- Needs 2 power FETs of >400V rating

Valley switch flyback operation



Valley switch flyback with leakage



1. With leakage inductance, the drain node is clamped by RCD snubber. Once the leakage energy is expended, the drain node rings down to VIN + N*VOUT

Design criteria

- Let the voltage of the clamp be

$$V_{CLAMP} = NV_{OUT} + V_C$$

- Maximum VDS on the switch

$$V_{DS,max} = V_{IN} + NV_{OUT} + V_C$$

- For VIN range from 90V – 360V and VOUT = 60V, N=2 is selected to keep duty cycle within reasonable range
- To keep maximum VDS to less than 600V, the clamp voltage is chosen as 240V, with VC set to 120V

Losses in a flyback converter

V_IN, L_lk, V_OUT_N, R_S, C_S, L_1, L_2, C_SEC, C_OUT, D_2, D_1, V_OUT_P, LS_ON, C_PRI

$$P_{cond,sw} = I_{rms,pri}{}^2 \times RDS_{ON}$$

$$P_{cond,diode} = I_{OUT} \times V_D + I_{rms,sec}{}^2 \times Rdiode$$

$$P_{L,copper} = I_{rms}{}^2 \times RIND_{DC} + I_{AC}{}^2 \times RIND_{AC}$$

$$P_{L,core} = a \times B_{pk}{}^b \times f_{sw}{}^c$$ (B_{pk} is proportional to $I_{L,\,pk\text{-}pk}$)

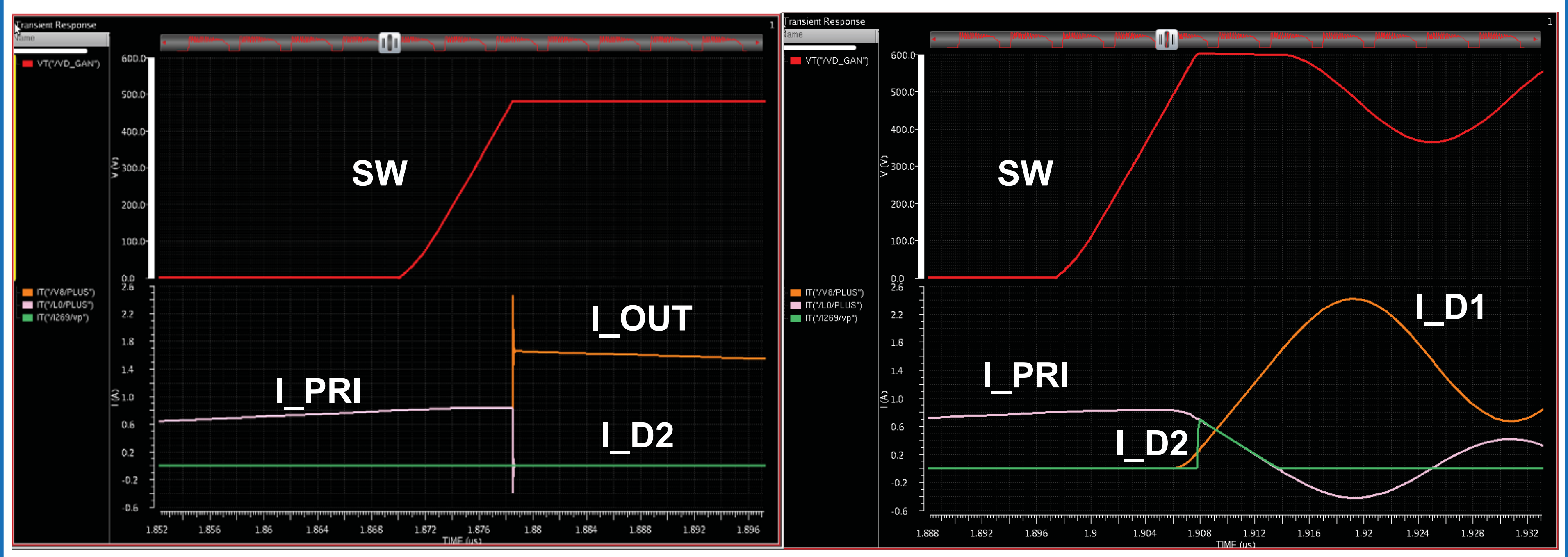
$$P_{sw} = \left[E_{OSS}@\,(VIN - N \times V_{OUT}) + \frac{1}{2} C_{pri}(VIN - N \times V_{OUT})^2\right] \times f_{sw}$$

$$P_{sw,diode} = \left[Q_{OSS}@\left(VOUT + \frac{V_{IN}}{N}\right) - Q_{OSS}@\,(2 \times VOUT) \times \left(VOUT + \frac{V_{IN}}{N}\right) f_{sw}\right]$$

$$P_{GD} = Q_G \times V_{GS} \times f_{sw}$$

$$P_{leak} = \frac{1}{2} L_K I_{peak}{}^2 \times \left(1 + \frac{NV_{OUT}}{V_C}\right)$$

Understanding leakage loss



- Time taken for leakage energy to be discharged into clamp

$$T_K = \frac{L_K I_{peak}}{V_C}$$

- Energy taken from output during this time

$$P_{leak,out} = \frac{1}{2} I_{peak} \times T_K \times NV_{OUT} = \frac{1}{2} L_K I_{peak}{}^2 \times \frac{NV_{OUT}}{V_C}$$

- Total leakage energy lost: $P_{leak} = \frac{1}{2} L_K I_{peak}{}^2 \times \left(1 + \frac{NV_{OUT}}{V_C}\right)$

V_{IN} L_{lk} NV_{OUT} + V_{CLAMP} L_{mag} NV_{OUT} D_2 C_{PRI}

Losses specific to the switch

$$P_{cond,sw} = I_{rms,pri}{}^2 \times RDS_{ON}$$

$$P_{cond,diode} = I_{OUT} \times V_D + I_{rms,sec}{}^2 \times Rdiode$$

$$P_{L,copper} = I_{rms}{}^2 \times RIND_{DC} + I_{AC}{}^2 \times RIND_{AC}$$

$$P_{L,core} = a \times B_{pk}{}^b \times f_{sw}{}^c$$

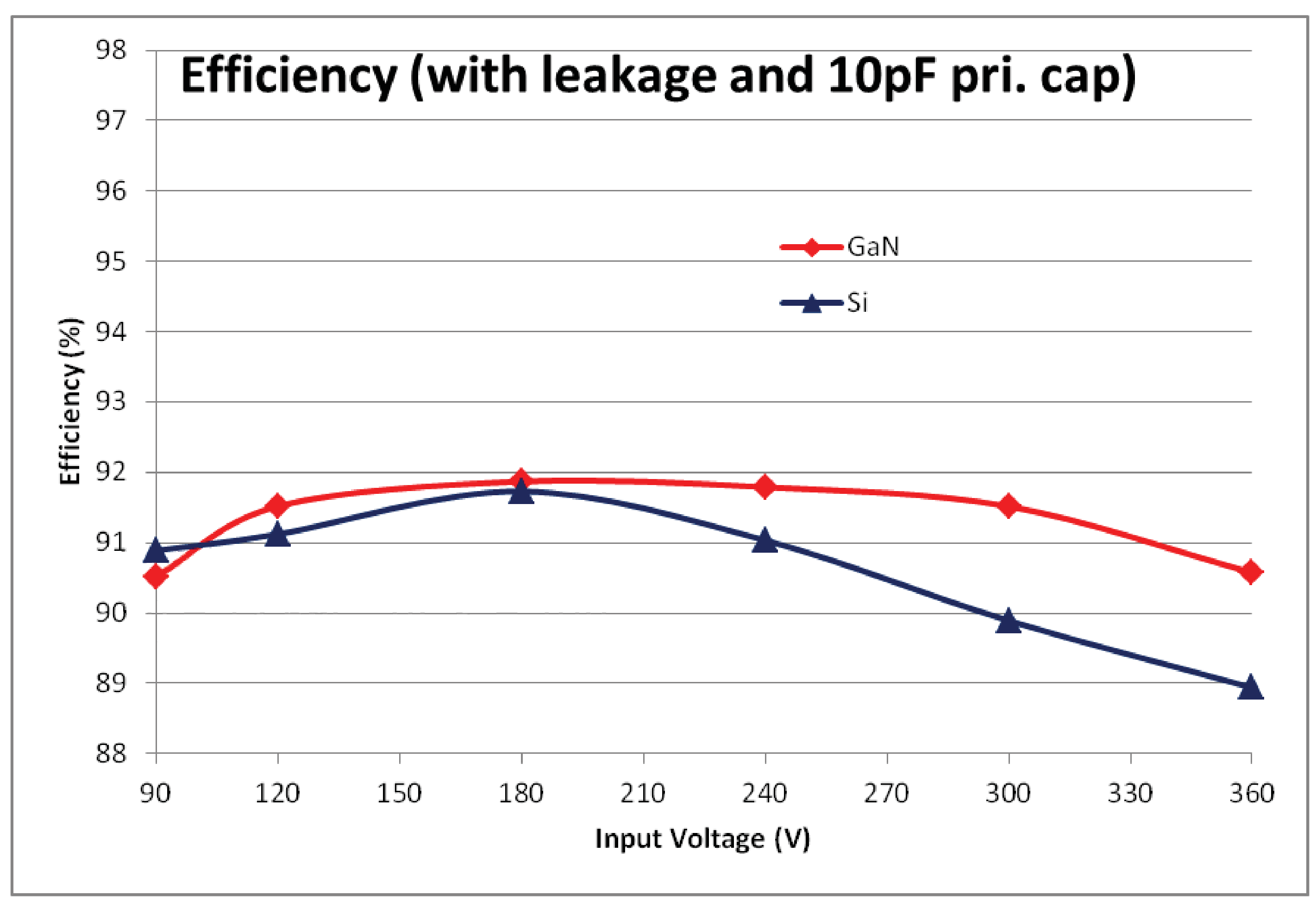
$$P_{sw} = \left[E_{OSS}@\,(VIN - N \times V_{OUT}) + \frac{1}{2} C_{pri}(VIN - N \times V_{OUT})^2\right] \times f_{sw}$$

$$P_{sw,diode} = \left[Q_{OSS}@\left(VOUT + \frac{V_{IN}}{N}\right) - Q_{OSS}@\,(2 \times VOUT) \times \left(VOUT + \frac{V_{IN}}{N}\right) f_{sw}\right]$$

$$P_{GD} = Q_G \times V_{GS} \times f_{sw}$$

$$P_{leak} = \frac{1}{2} L_K I_{peak}{}^2 \times \left(1 + \frac{NV_{OUT}}{V_C}\right)$$

Efficiency Comparison



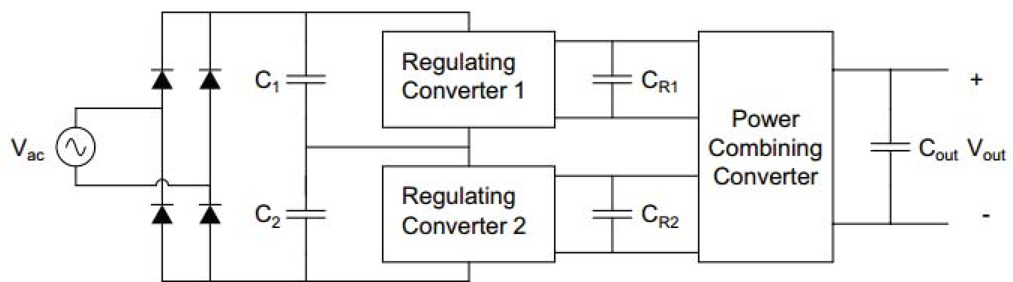
- Single low-side switch with isolation capability
- Severe voltage stress on the primary switch
- Switch losses are a small fraction of the overall losses and E_{OSS} dependent

Topology Selection

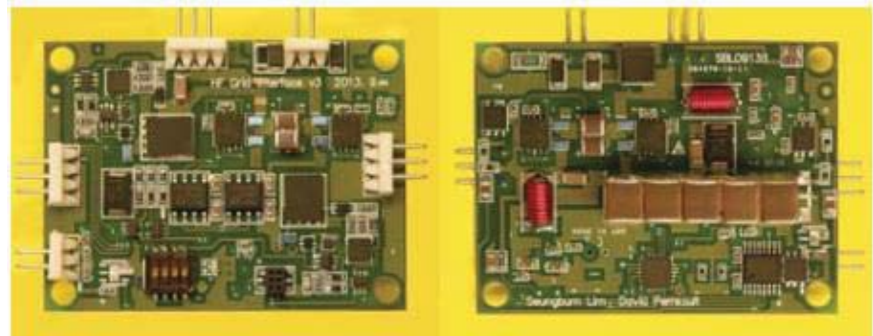
	0-100 W, Iout<10 A	0-100 W, Iout>10 A	100-400 W	400-1200 W	1200-3000 W
Single-switch flyback	✓	-	-	-	-
2-switch flyback	✓	-	-	-	-
Active clamp flyback	✓	-	-	-	-
Single-switch forward	✓	✓	-	-	-
2-switch forward	✓	✓	✓	-	-
Active clamp forward	✓	✓	✓	-	-
Half bridge	-	✓	✓	✓	-
LLC Half Brdige	-	✓	✓	✓	-
Full bridge	-	-	-	✓	-
Phase shifted ZVT full bridge	-	-	-	✓	✓

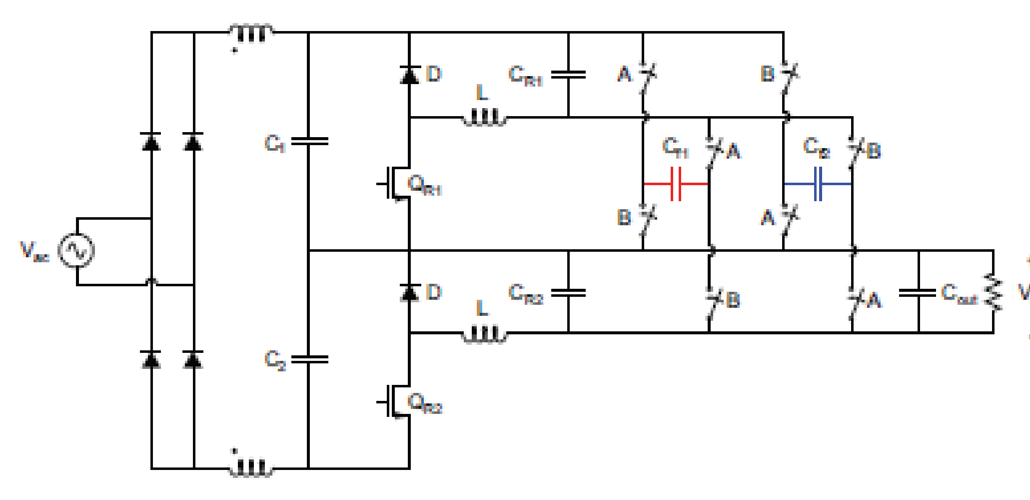
http://www.smps.us/topologies.html

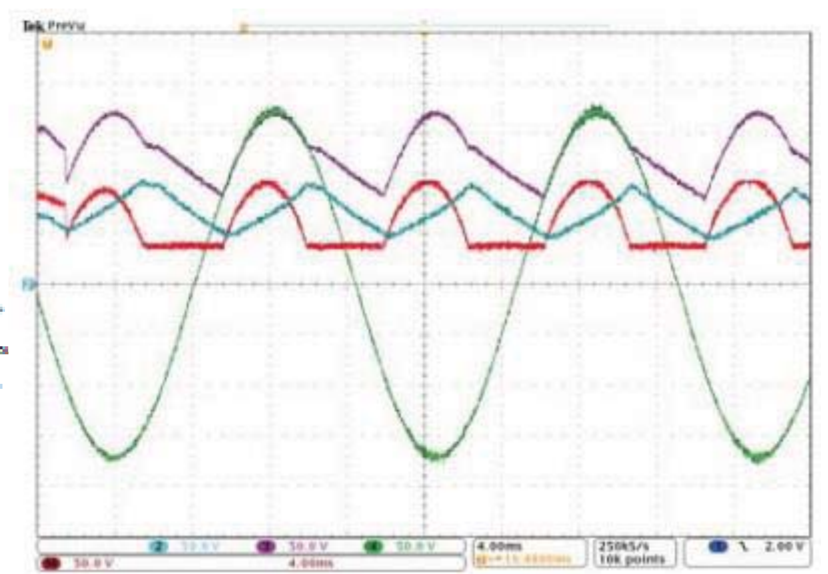
Stacked power converters



c. S. Lim, APEC 2014





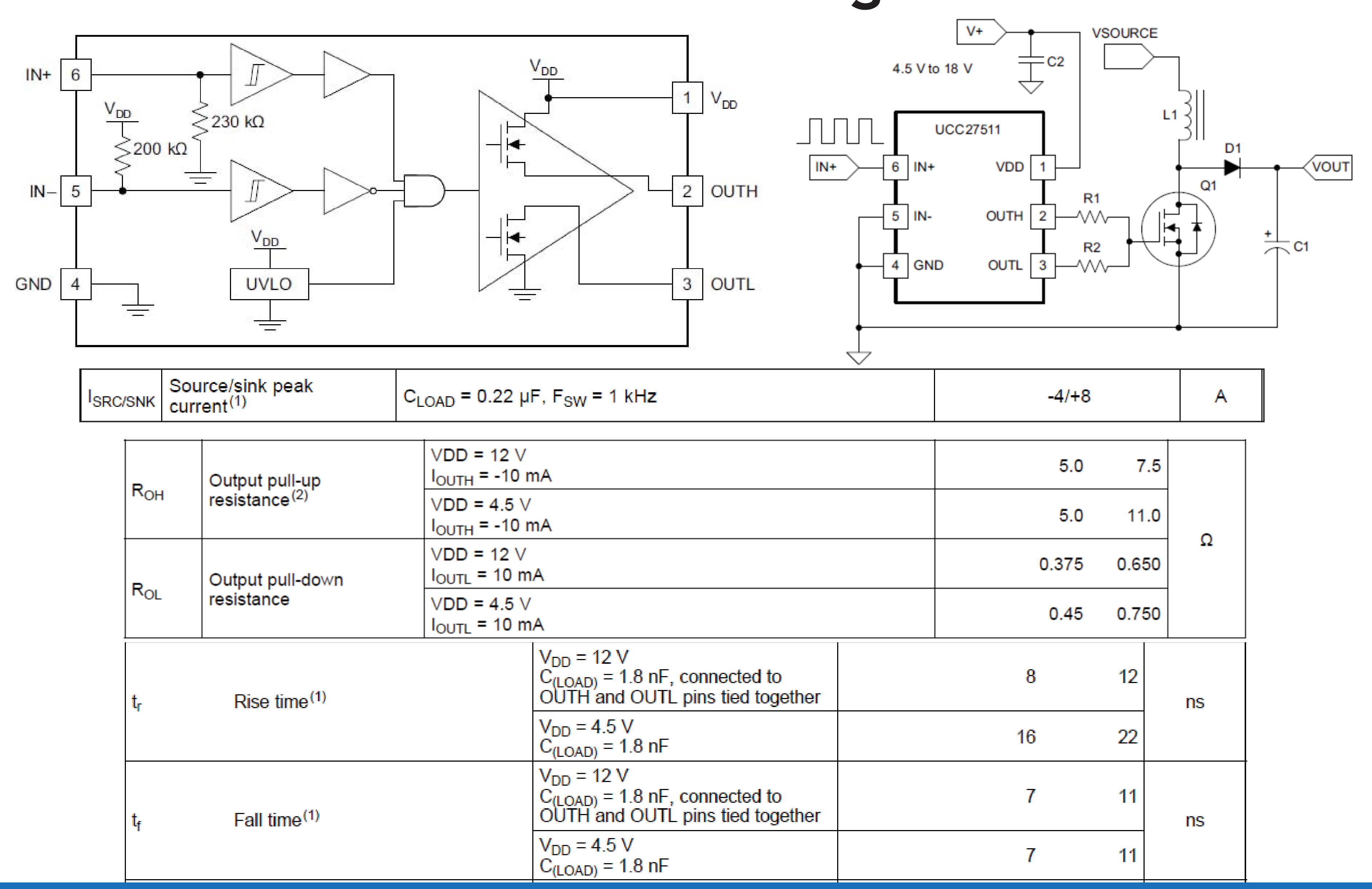


- Energy density of capacitors is higher
- Reduced voltage rating on switches
- More switches and associated drivers

Outline

- Power devices
  - MOS
  - GaN
  - SiC, IGBT
- Power system topologies
  - Hard-switched
  - Soft-switched
  - Buck, flyback
- Gate Drivers
  - Drive Requirements
  - Isolation
  - Protection Circuits
- Summary

UCC27511 - Low side gate driver

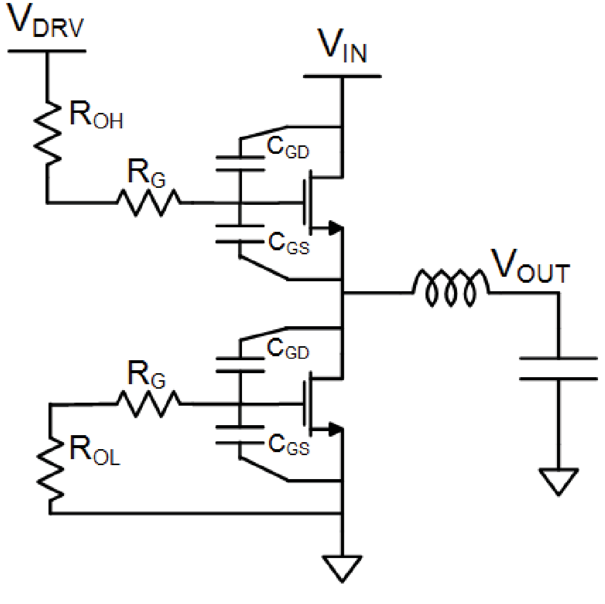


$I_{SRC/SNK}$	Source/sink peak current (1)	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz	-4/+8	A

R_{OH}	Output pull-up resistance (2)	VDD = 12 V, I_{OUTH} = -10 mA	5.0	7.5	Ω
		VDD = 4.5 V, I_{OUTH} = -10 mA	5.0	11.0	
R_{OL}	Output pull-down resistance	VDD = 12 V, I_{OUTL} = 10 mA	0.375	0.650	
		VDD = 4.5 V, I_{OUTL} = 10 mA	0.45	0.750	

t_r	Rise time (1)	V_{DD} = 12 V, $C_{(LOAD)}$ = 1.8 nF, connected to OUTH and OUTL pins tied together	8	12	ns
		V_{DD} = 4.5 V, $C_{(LOAD)}$ = 1.8 nF	16	22	
t_f	Fall time (1)	V_{DD} = 12 V, $C_{(LOAD)}$ = 1.8 nF, connected to OUTH and OUTL pins tied together	7	11	ns
		V_{DD} = 4.5 V, $C_{(LOAD)}$ = 1.8 nF	7	11	

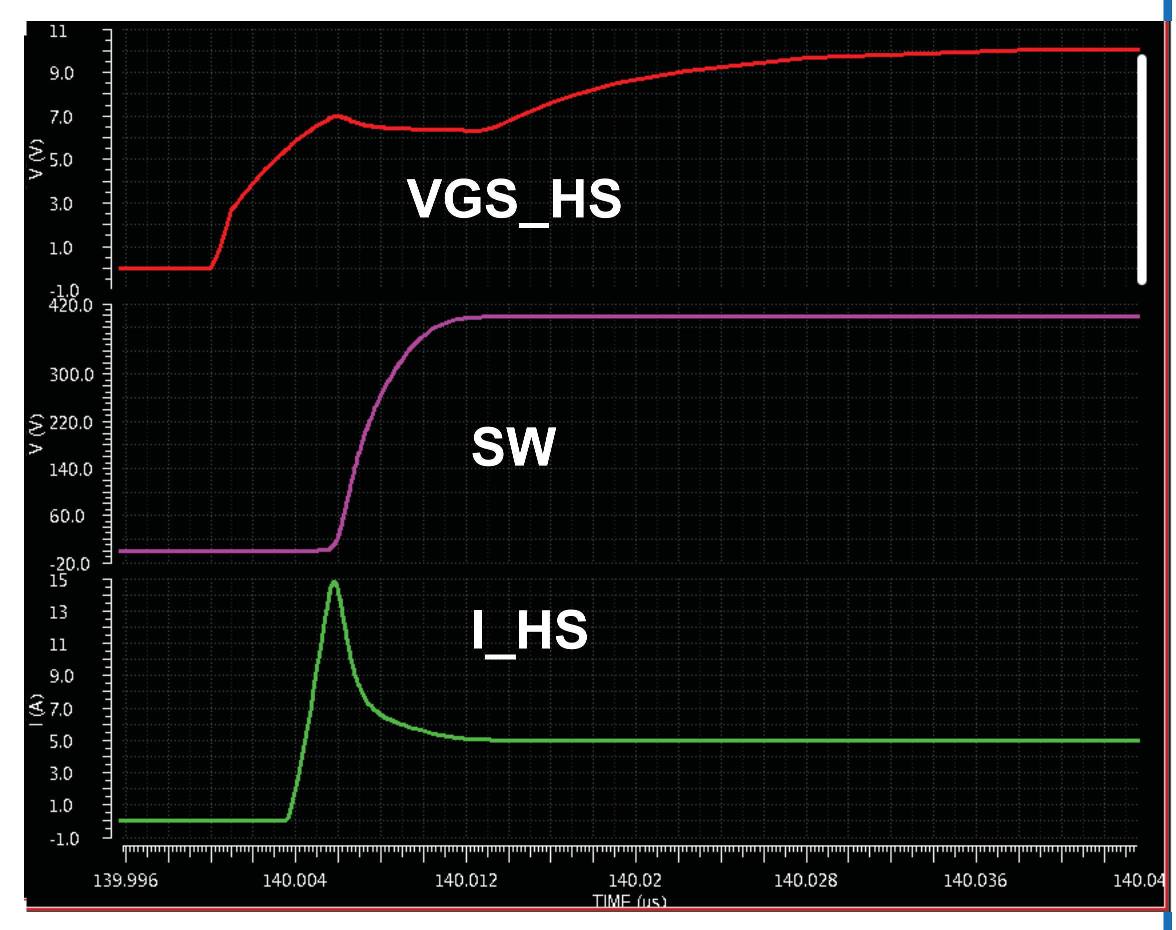
Turn-ON Slew-rate control



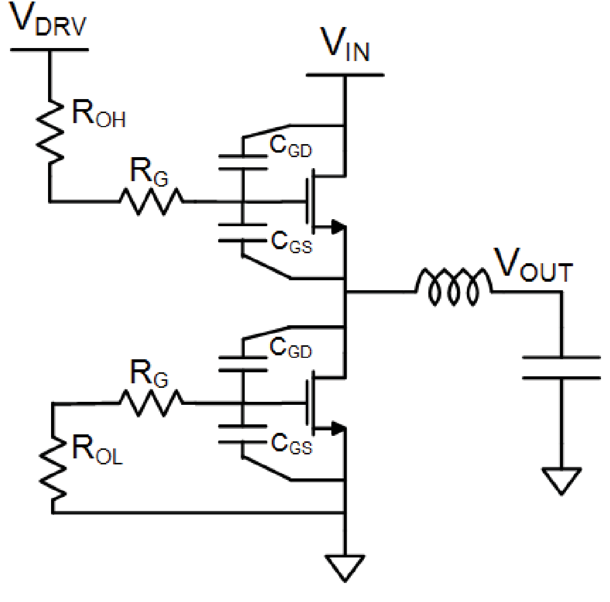
$$\frac{V_{DRV} - V_{GS}}{R_G} = C_{GD}\frac{dV}{dt}$$

$$C_{OSS}\frac{dV}{dt} = g_m V_{GS}$$

$$\frac{dV}{dt} = \frac{V_{DRV}}{\frac{C_{OSS}}{g_m} + R_G C_{GD}}$$



Turn-ON Slew-rate control



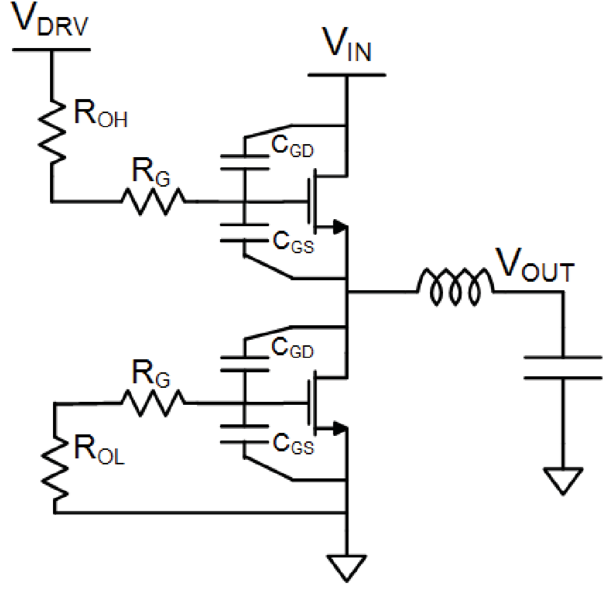
$$\frac{V_{DRV} - V_{GS}}{R_G} = C_{GD}\frac{dV}{dt}$$

$$C_{OSS}\frac{dV}{dt} = g_m V_{GS}$$

$$\frac{dV}{dt} = \frac{V_{DRV}}{\frac{C_{OSS}}{g_m} + R_G C_{GD}}$$

Adding 10nH loop inductance

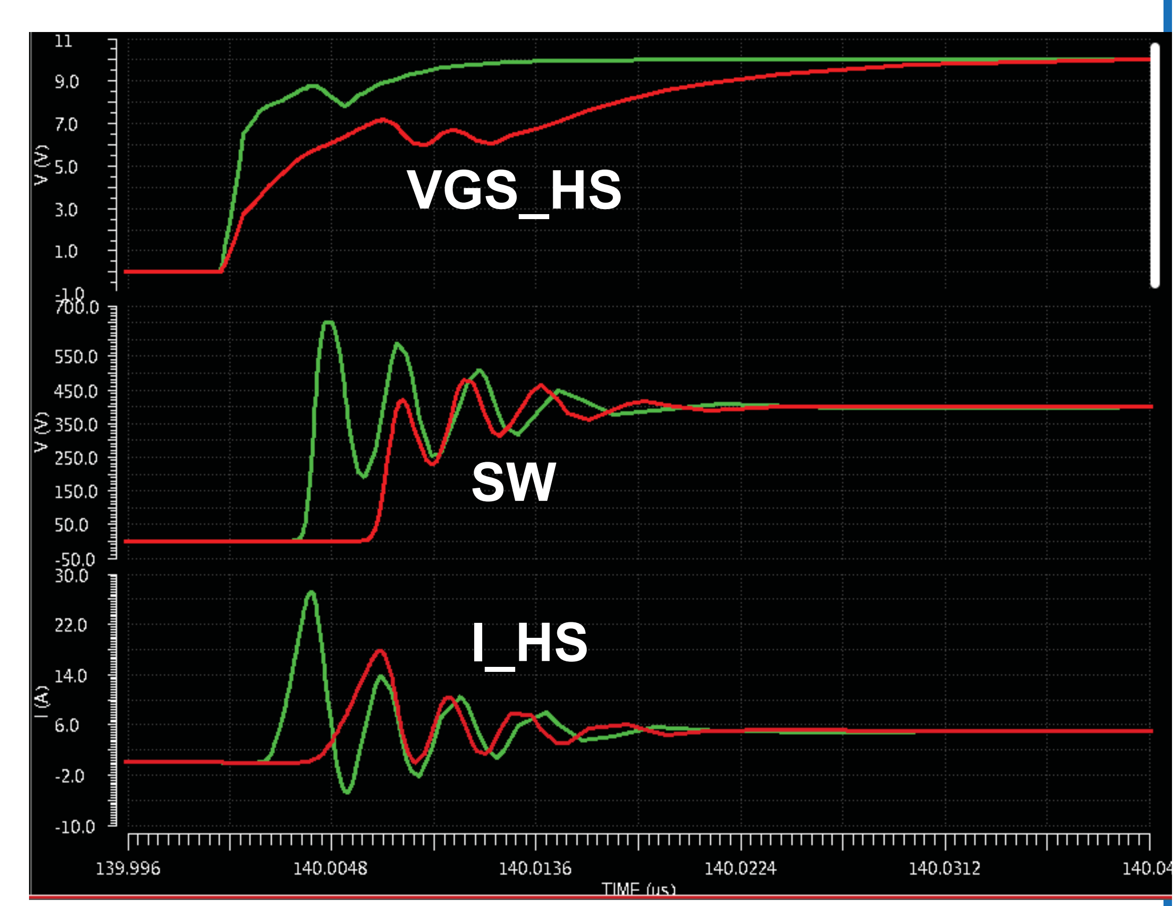
Turn-ON Slew-rate control



$$\frac{V_{DRV} - V_{GS}}{R_G} = C_{GD}\frac{dV}{dt}$$

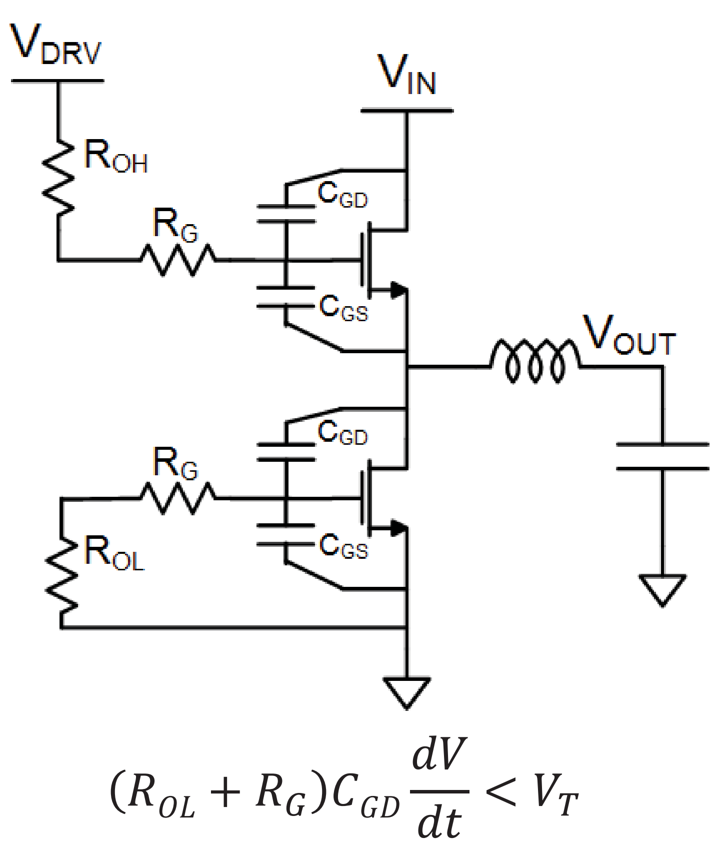
$$C_{OSS}\frac{dV}{dt} = g_m V_{GS}$$

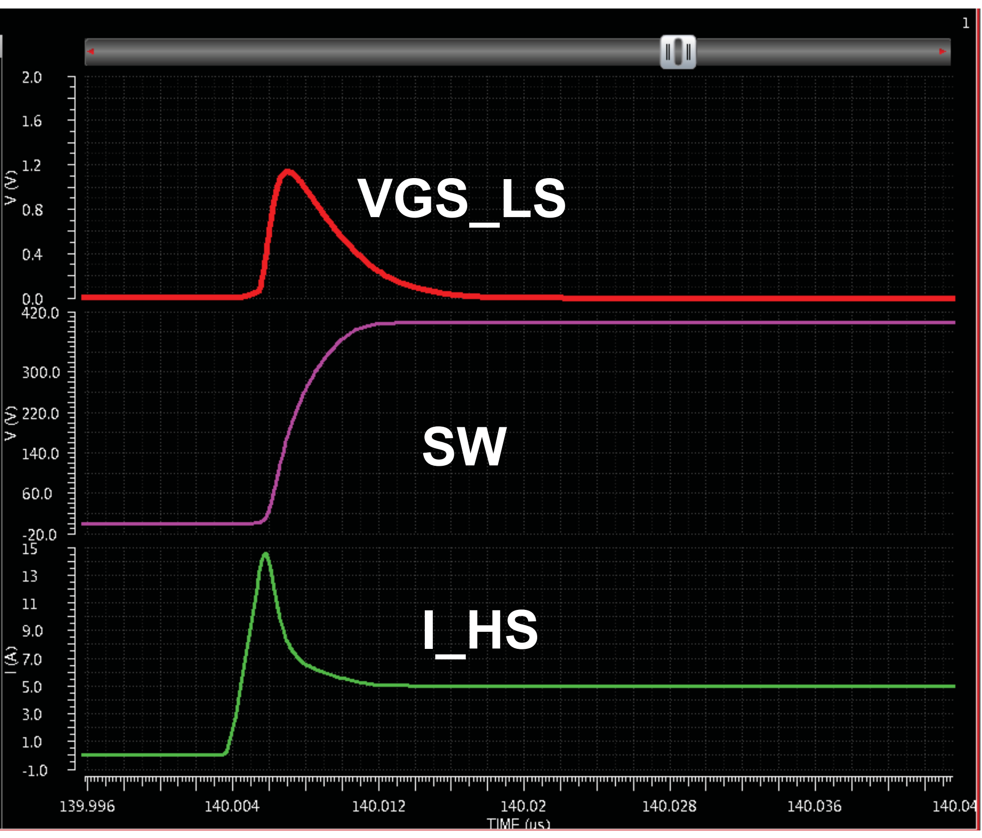
$$\frac{dV}{dt} = \frac{V_{DRV}}{\frac{C_{OSS}}{g_m} + R_G C_{GD}}$$



R_G : 1Ω → 5Ω

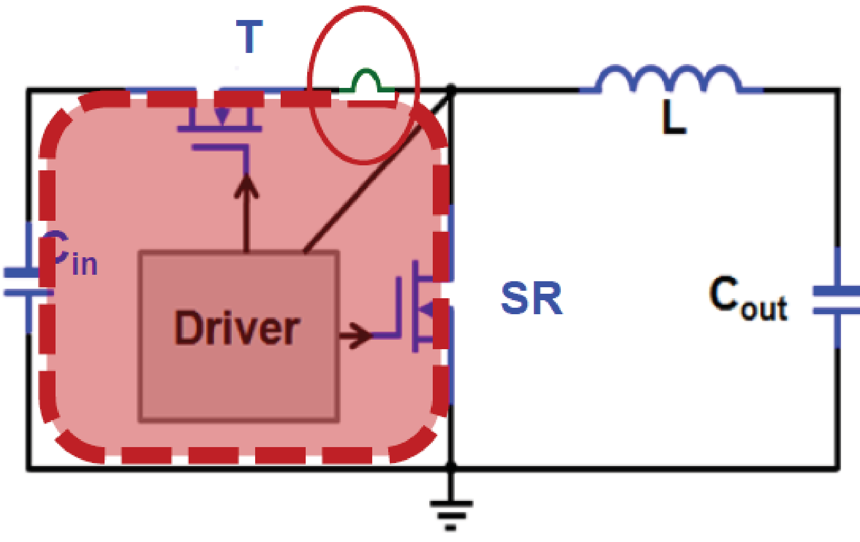
Pull-down constraints



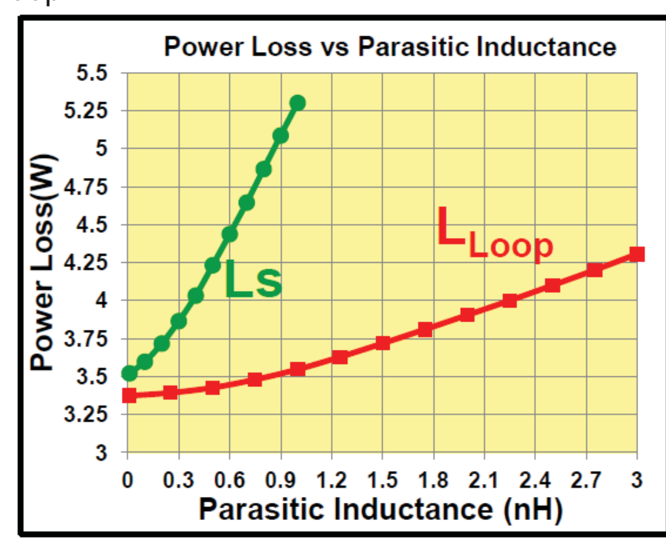


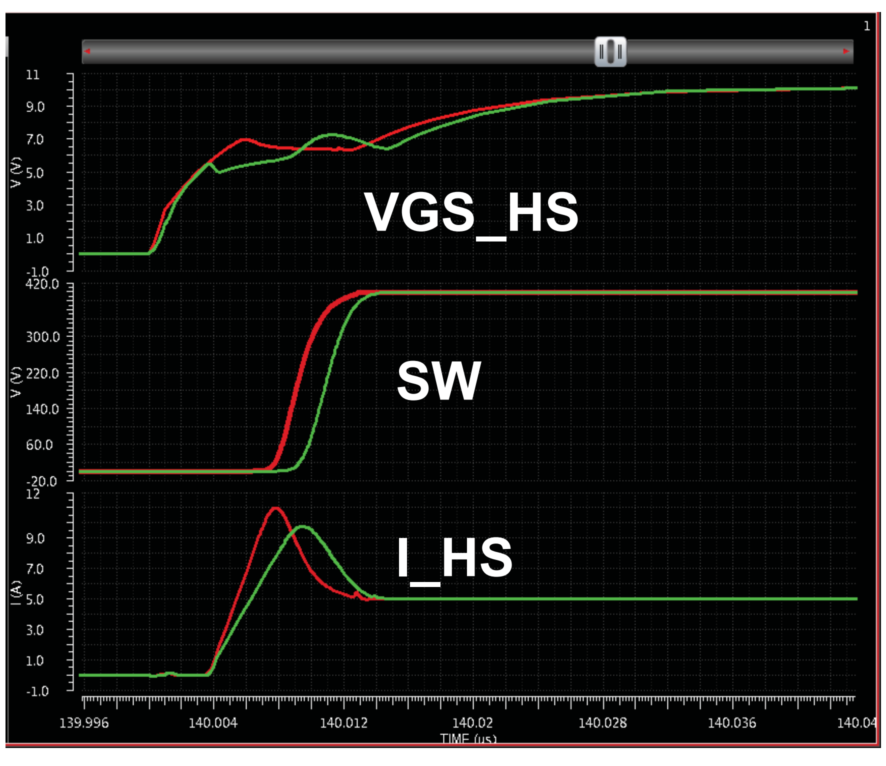
- Pull-down resistance needs to be small enough to prevent accidental turn-ON of power FET during hard-switching event

Loop Parasitics



L_s: Common Source Inductance
L_{loop}: Power Loop Inductance





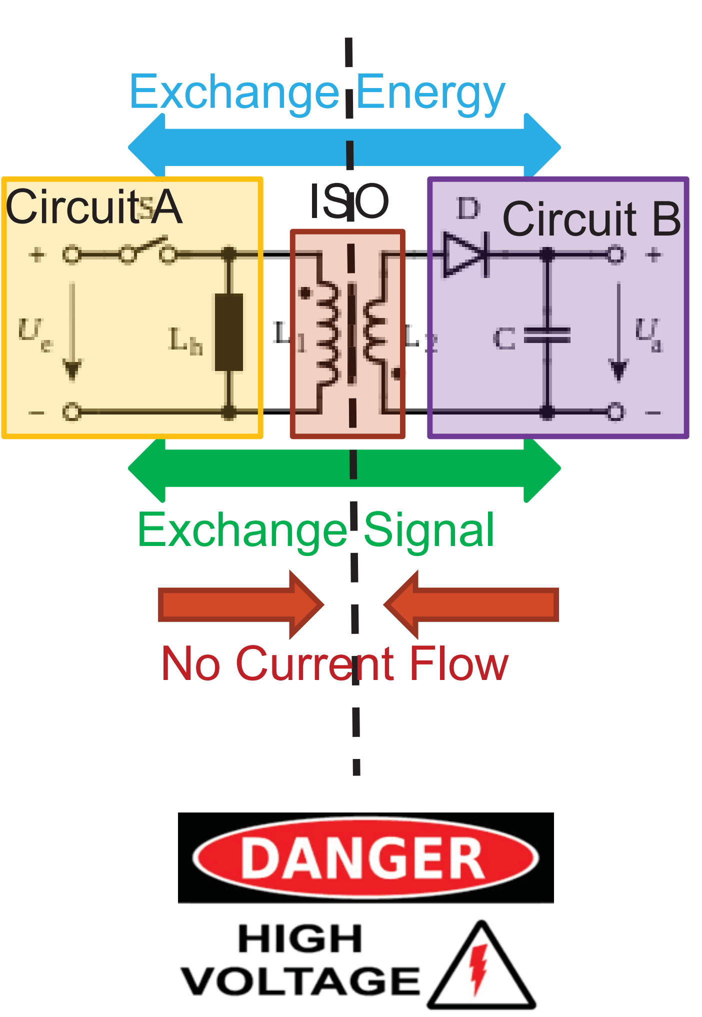
L_s : 0 → 2nH

- Common source inductance slows down turn-ON and increases overlap losses

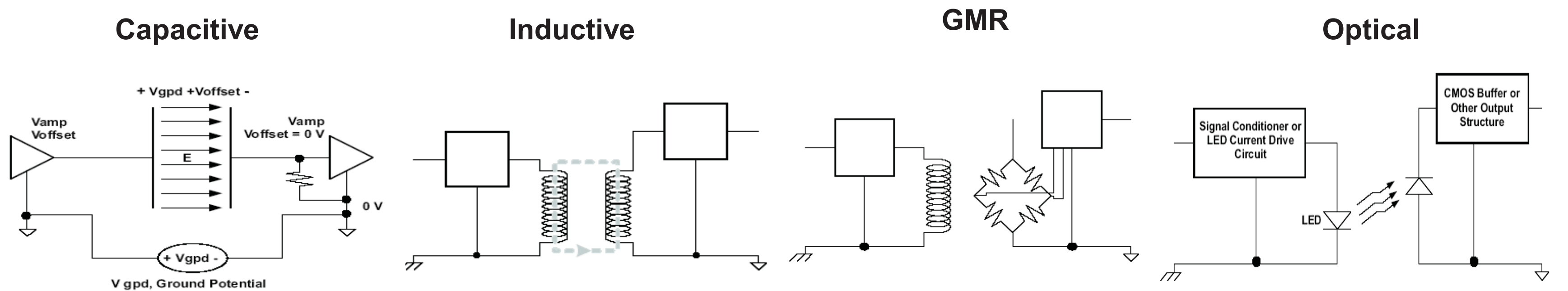
c. A. Lidow, DesignWest, 2013

Isolation

- What is Isolation?
  - It is a means for two or more electrical circuits to exchange signal or power without current flow
- Why Isolation is Used?
  - Safety, to protect from high voltage potential that would damage equipment or harm humans.
  - Break ground loop, to tolerate ground difference or eliminate ground/common-mode noise.
  - Communication, to send signal between unreferenced circuits or long distance
  - Level shifting



Signal Isolators

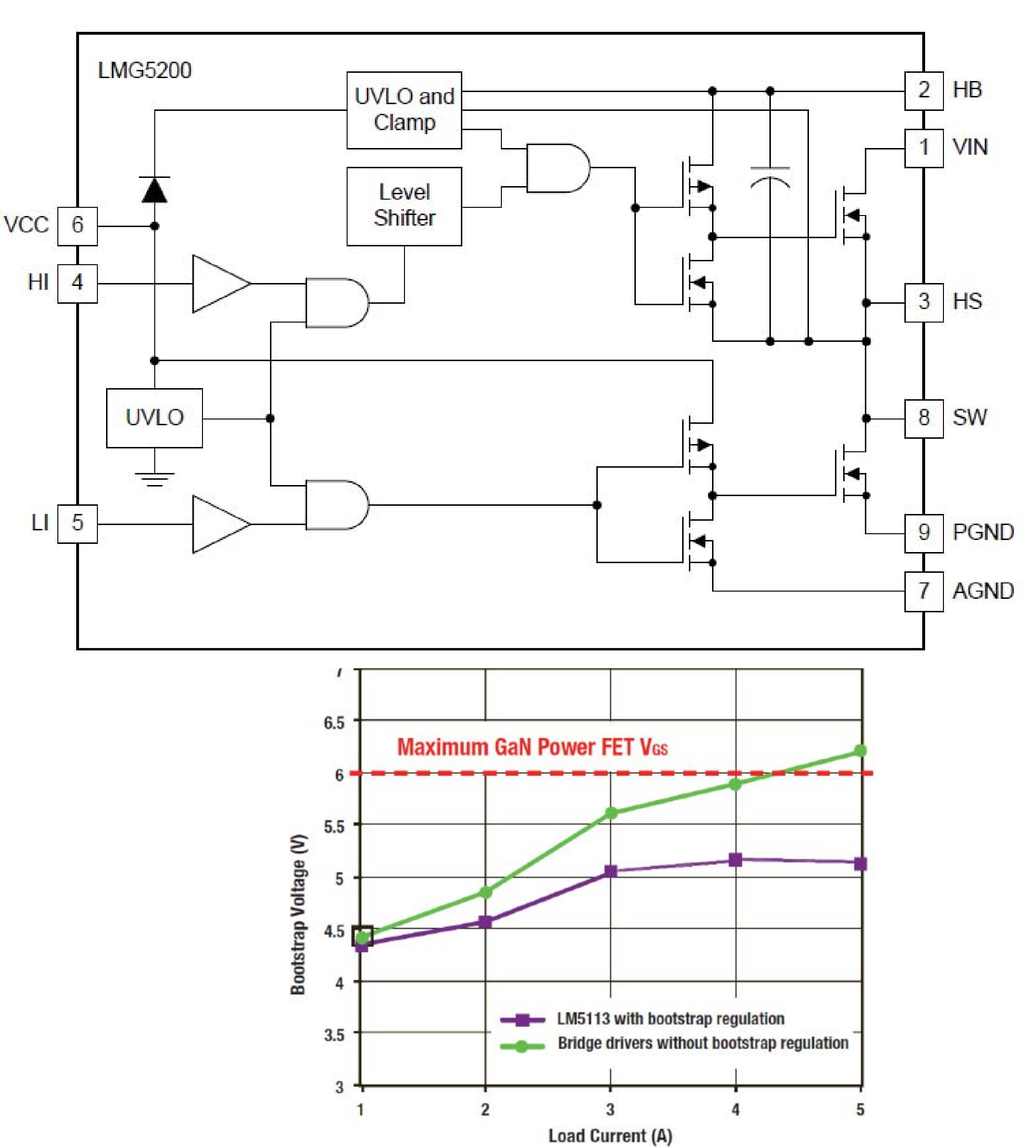


Part	Coupling Technology	V_{CC} (V)	Signaling Rate (Mbps)	UL1577 (VRMS)	Transient Immunity (kV/µs)	Power (mW)	Magnetic Field Immunity	Reliability (MTTF), 60% Confidence (Hr/Fail.)
ISO721	Capacitive	3.3 or 5	150	2500	25	60	+	1.25M
ADuM1100	Inductive	5	100	2500	25	4.3		
		3.3	50			1.2		
HCPL-0900	Inductive	5	100	2500	15	30		288k
		3.3				13.2		
HCPL-0721	Optical	5	25	3750	10	95	++	175k
HCPL-0723	Optical	5	50			137.5	++	

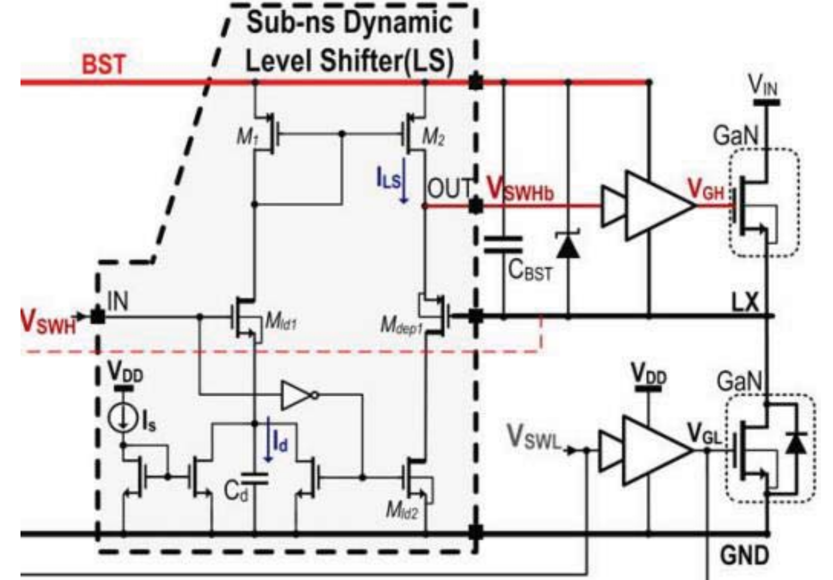
- Capacitive level shifter has high signal rates
- Transformer based level shifters excel in power consumption and immunity
- Optical isolators can handle large isolation voltages

LMG5200 - Half-bridge power stage

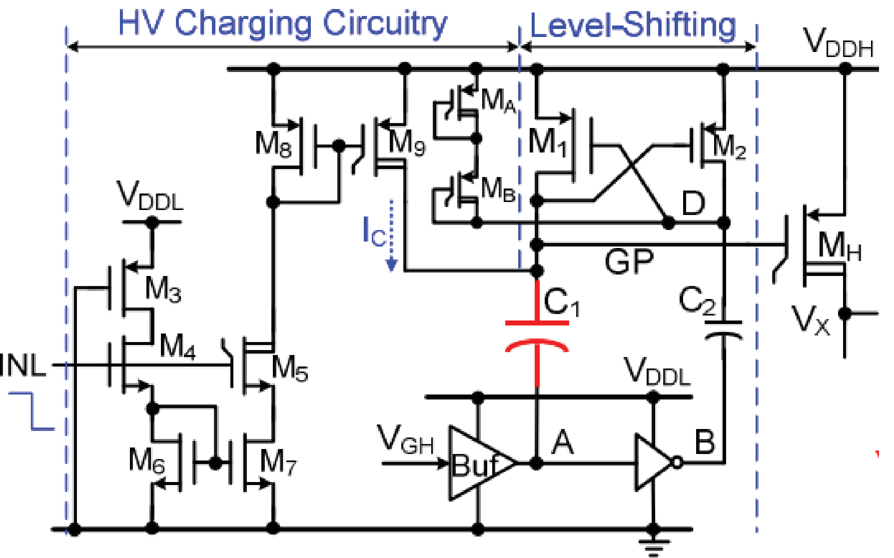
- Integrated 80V GaN FETs
  - Minimizes power and gate loops
- Drivers co-packaged with HS, LS FETs
- Fast propagation times
- Protection Functions
  - UVLO
  - Bootstrap clamp
  - Thermal Shutdown for GaN



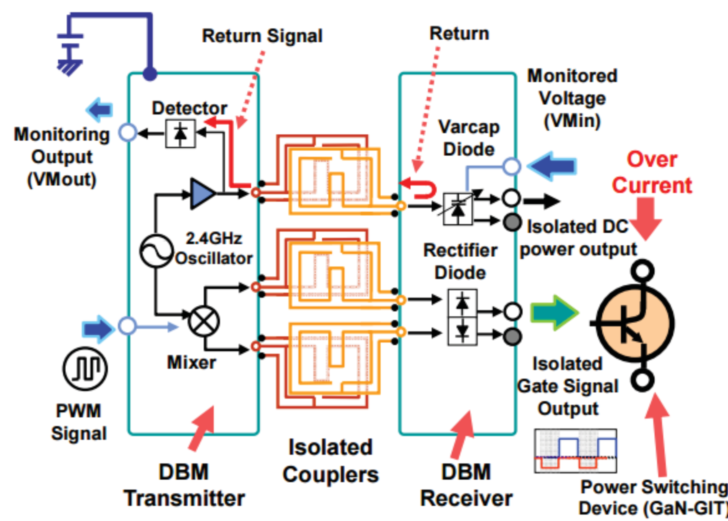
Level shifter options

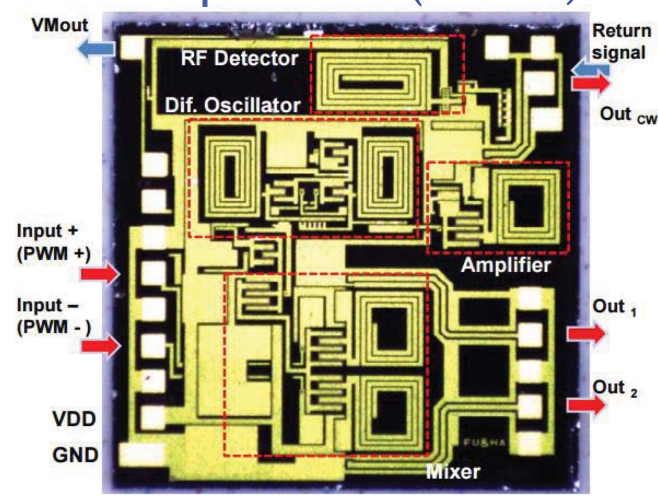


- Cascode (L. Chen, ISSCC 2015)



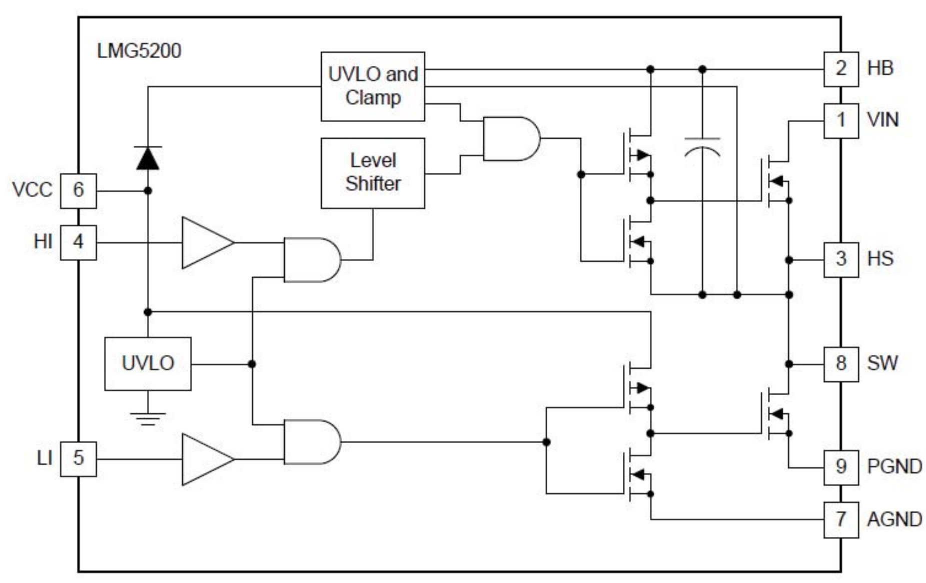
- Capacitive (Z. Liu, CICC 2015)





- Microwave (S. Nagai, ISSCC 2012)

LMG5200 - Half-bridge power stage



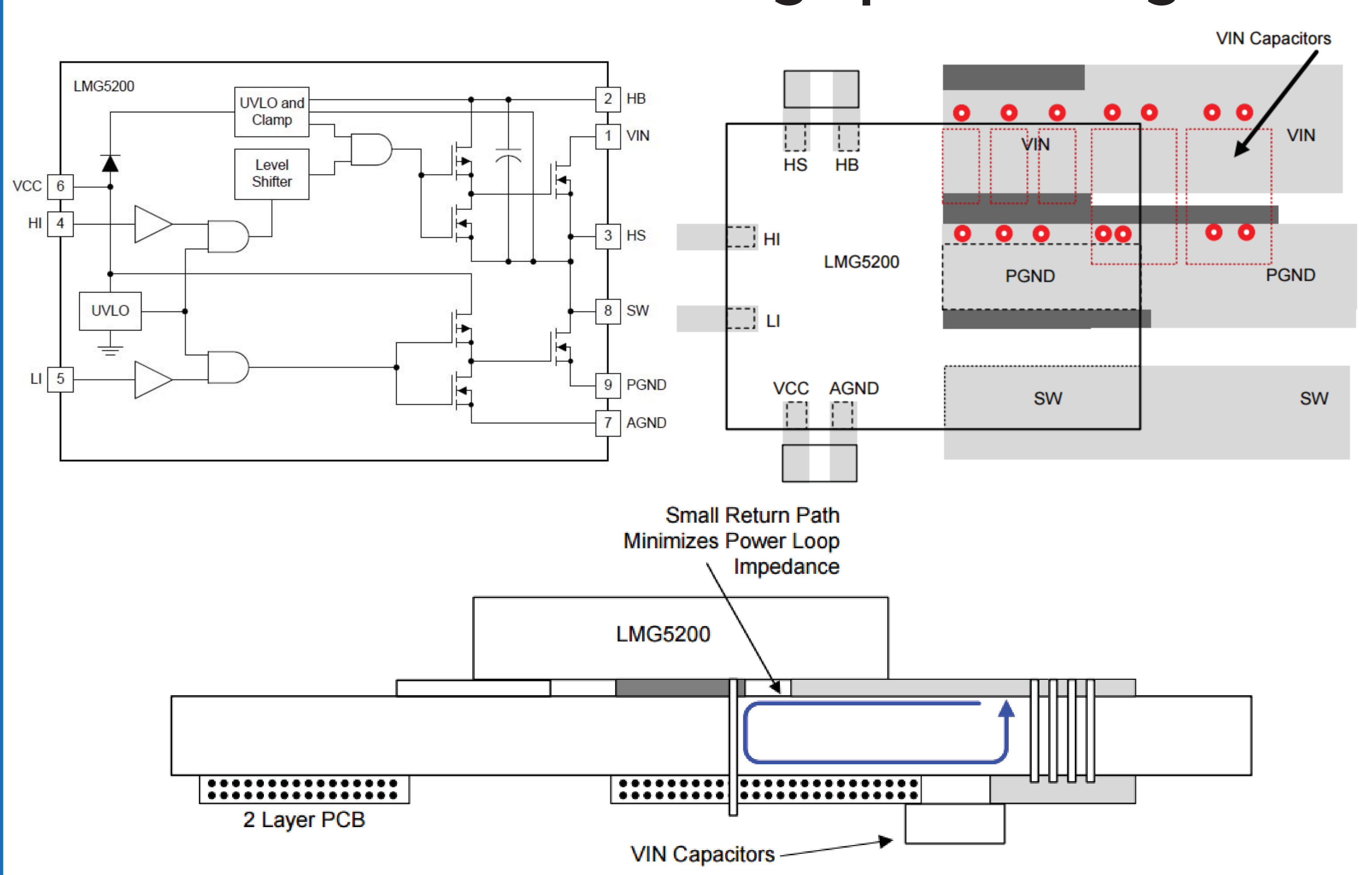
BOOTSTRAP DIODE

	HB-HS clamp	Regulation voltage	4.7	5	5.3	V
t_{BS}	Bootstrap diode reverse recovery time	I_F = 100 mA, I_R = 100 mA		40		ns
Q_{RR}	Bootstrap diode reverse recovery charge	V_{VIN} = 50 V		2		nC

Q_{OSS}	Output charge	V_{DS} = 50 V, I_D = 10 A		20		nC
Q_{RR}	Source to drain reverse recovery charge	Not including internal driver bootstrap diode		0		nC

t_{MON}	Delay matching: LI high and HI low (2)	V_{VIN} = 50 V, V_{VCC} = 5 V		2	8.0	ns
t_{MOFF}	Delay matching: LI low and HI high (2)	V_{VIN} = 50 V, V_{VCC} = 5 V		2	8.0	ns
t_{PW}	Minimum input pulse width that changes the output		10			ns

LMG5200 - Half-bridge power stage



Summary

- High voltage power devices play a significant role in our daily activities
- Energy efficiency of these devices impact a major part of energy consumption in the world
- Advent of faster, more efficient wide bandgap devices promises smaller, lighter power supplies
- Topology selection and application space determines the choice of suitable power device
- Smarter gate drive solutions and integrated modules are needed to maximize the benefits of faster switching devices and make robust power solutions