22.6 A 25Gb/s 4.4V-Swing AC-Coupled Si-Photonic Microring Transmitter with 2-Tap Asymmetric FFE and Dynamic Thermal Tuning in 65nm CMOS

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Silicon photonic microring modulators (MRMs) offer a promising approach for realizing energy-efficient wavelength-division multiplexing (WDM) optical interconnects. For data-rates greater than 10Gb/s, depletion-mode MRMs are generally preferred over their injection-mode counterparts due to their shorter carrier lifetimes and resulting higher bandwidths. Unfortunately, these depletion-mode MRMs typically exhibit low PN junction tunability, thereby requiring higher modulation voltages in order to provide >6dB extinction ratios (ER). Furthermore, negative DC-biasing of the MRMs is necessary to maintain reverse-biased depletion-mode operation. In this work, a 5×25Gb/s hybrid-integrated MRM WDM transmitter is demonstrated that incorporates the following key advances: 1) an AC-coupled differential output driver that applies a $4.4V_{pp\text{-}diff}$ output-swing on the MRM while providing a tunable on-chip negative DC-bias; 2) a 2-tap non-linear digital FFE that compensates for optical-dynamics-induced bandwidth limitations; 3) a dynamic thermal tuning loop that stabilizes the MRM by minimizing thermally-induced wavelength fluctuations.

As seen in Fig. 22.6.1, wire-bonding-based hybrid integration provides a low-cost approach for Si-photonic systems with a moderate number of pads. The Si-photonic WDM chip in this work consists of 8 common bus MRMs [1], with 5 of them wire-bonded to the CMOS transmitter IC. The measured DC ring spectrum data of the MRMs, which have a 7.5µm radius and ~5000 quality factor, shows that 4V swing is required to achieve >7dB extinction ratio. One potential approach to achieve this large swing amplitude involves the use of differential pulsed-cascode output stages using thin-oxide transistors [3,4], which can achieve 2×DVDD swing per-terminal, or an effective 4×DVDD differential swing on the modulator. However, DC-coupled differential drivers can provide only a 0V DC-bias, which conflicts with the negative-bias requirement for depletion-mode operation. While adding negative supply voltages can provide fixed DC-biases for the differential outputs [2], the number of power-supply domains will increase. In this work, an AC-coupled differential output stage is developed that enables 4×DVDD swing together with a tunable negative DC-bias. Figure 22.6.1 shows the on-chip DC-blocking capacitor C_C and DC-bias resistor R_B, implemented with the pulsed-cascode output stages to decouple the high-frequency modulation from the DC-bias voltages. The insertion loss of the driver passive network is designed to be <1dB between 0.1 and 20GHz, to minimize signal-integrity degradation and achieve $\sim 4.4V_{pp\text{-}diff}$ effective output swing from a 1.2V DVDD supply.

Figure 22.6.2 shows the block diagram of the 5-channel transmitter array. A half-rate global clock is distributed through an on-chip transmission line and locally recovered by per-channel CML-to-CMOS converters. 8-to-1 data serialization is achieved using three stages of CMOS MUXs. In conventional high-speed 2-to-1 MUX designs, retiming latches are used to introduce 1-UI delay between even and odd data. While CML latches could potentially be employed in the final 25Gb/s MUX stage, the low-swing CML output conflicts with the CMOS-level swings required in the output driver. Instead, this design utilizes quadrature phases in the 8-to-4 and 4-to-2 MUX stages to generate even and odd 12.5Gb/s data with 1UI delay to eliminate 25Gb/s retiming. A tri-state-inverter-based 2-to-1 MUX design is employed in the final two MUX stages that enable sub-15ps transition times, which is 50% faster than a conventional pass-gate MUX with identical clock-gate sizing and load capacitance. These fast edge rates result in minimal jitter accumulation of the TX, as demonstrated by the low jitter measurement of $582fs_{rms}$ when one of the transmitters is configured to output a 1010 clock pattern.

While depletion-mode MRMs exhibit superior modulation linearity relative to injection-mode devices, optical dynamics can still introduce unbalanced positive and negative transition times, significantly degrading the effective ER for data-rates higher than 20Gb/s [2]. To compensate for this non-linear ISI, an independently adjustable 2-tap FFE is required. This asymmetric FFE can be realized with the pulsed-cascode structure, where the auxiliary output stages are connected to the main stage output node [4]. However, if for example a ¼ weight auxiliary tap is activated, simulations indicate that the cascode PMOS and NMOS of the auxiliary stage will suffer from 1.7V V_{DS} overstress. This problem is addressed in our design by moving the current-shunting path to the source of the main output stage cascode transistors. FFE one and zero levels are controlled independently by binary coefficients EQ_P<0:3> and EQ_N<0:3>. Additionally, the main-tap pull-up and pull-down impedances are independently controlled by IMP_P<0:3> and IMP_N<0:3> to realize a tunable slew rate and output swing. Electrical-only testing is performed using one replica channel, implemented without on-chip AC-coupling capacitors and DC-bias resistors. Figure 22.6.3 shows the measured 25Gb/s electrical eye diagrams for different FFE settings. By optimizing the FFE coefficient, a wide eye opening is achieved for a 2^7-1 PRBS pattern, with a total jitter of 6.56 and $7.84ps_{pp}$ for one and five active channels, respectively. FFE tunability is also verified using a fixed output pattern.

The hybrid-integrated WDM transmitter shown in Fig. 22.6.1 is tested for its optical performance. Limited by the optical equipment setup (only a single tunable laser), each of the five MRMs is tested individually in succession. Figure 22.6.4 shows the measured 25Gb/s optical eye diagrams for two different MRMs. For MRM-1, a significant transition-time difference is observed when the FFE disabled, resulting in a limited 5.3dB ER. After enabling post-cursor taps of 2/15 one level and 8/15 zero-level, the ER increases to 6.8dB, and the clean and symmetrical eye shows that the nonlinear ISI is well compensated. The impact of applied voltage swing on the ER is demonstrated with the optical eye diagrams of MRM-2, where an ER of 7.2dB for a differential swing is degraded to 4.7dB when the driver is configured as single-ended.

An average-power-based dynamic thermal tuning loop is implemented in the transmitter IC to compensate for temperature-induced resonant wavelength fluctuations. As shown in Fig. 22.6.5, the MRM integrates a 1kΩ resistor heater that is connected to a 12b ΣΔ thermal DAC, providing a 2V dynamic range that covers ~0.8nm wavelength tuning range. On power up, a 100MHz FSM automatically locks the ring to the optimal thermal bias point by comparing the average optical MRM output power with an on-chip reference voltage. In order to verify operation of the dynamic thermal tuning loop, an adjacent MRM heater is modulated with a voltage ramp that introduces temperature fluctuations. When thermal tracking is disabled, the optical eye opening degrades severely due to the subsequent resonant wavelength drift. When thermal tracking is enabled, the thermal fluctuations are suppressed and a healthy optical eye opening is achieved.

Figure 22.6.6 shows the power breakdown and performance comparison with previously published MRM transmitters. The presented transmitter achieves the highest electrical output swing at 25Gb/s, robust optical modulation using non-linear equalization, and dynamic closed-loop thermal control. Figure 22.6.7 shows the die micrograph of the transmitter IC fabricated in a GP 65nm CMOS process. The transmitter occupies a per-channel area of $0.1mm^2$.

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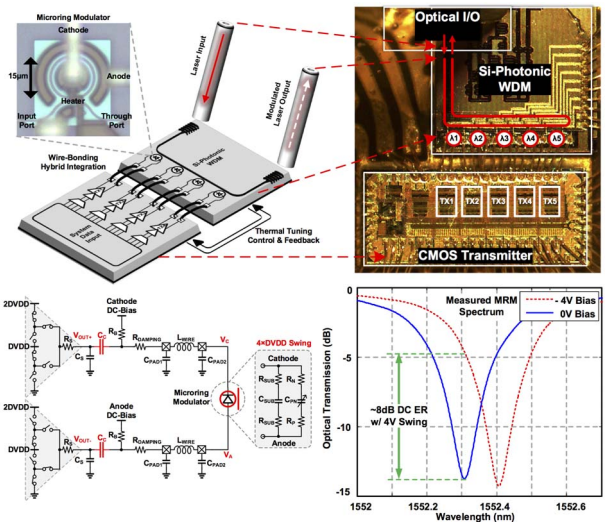

Figure 22.6.1: Hybrid integrated WDM transmitter concept and AC-coupled differential MRM modulation with 4×DVDD swing.

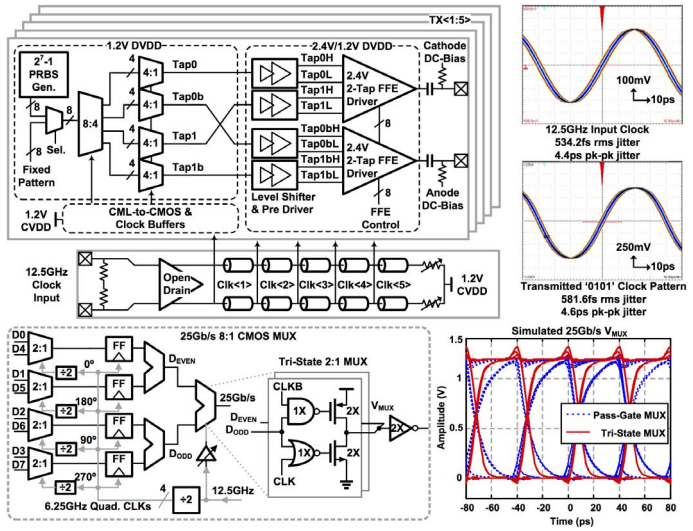

Figure 22.6.2: Transmitter block diagram and the CMOS-only 8-to-1 MUX design.

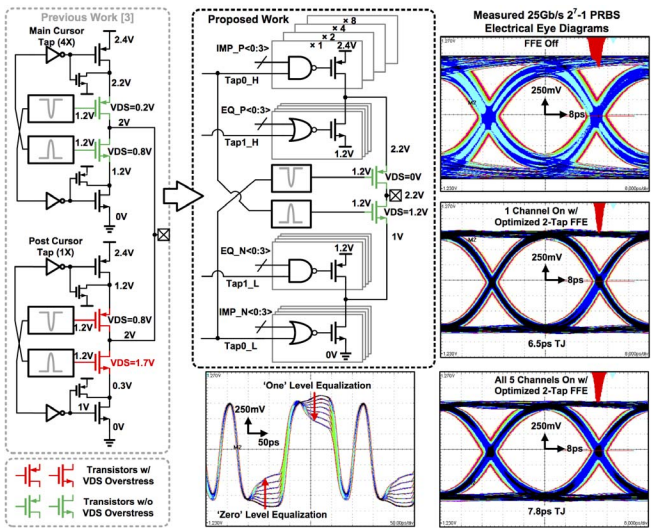

Figure 22.6.3: Architecture of the pulsed-cascode output stage with 2-tap asymmetric FFE and measured 25Gb/s electrical eye diagrams.

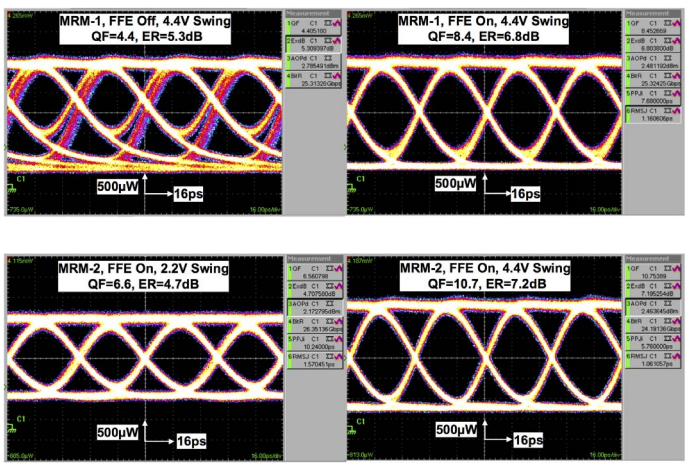

Figure 22.6.4: Measured 25Gb/s optical eye diagrams of the hybrid integrated WDM transmitter.

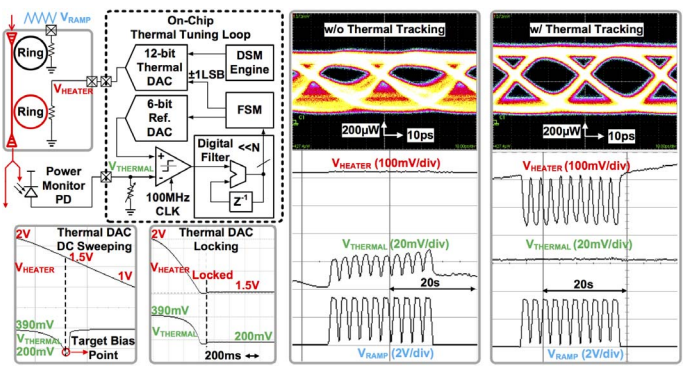

Figure 22.6.5: Block diagram of the dynamic thermal tuning loop, and the measured optical eye diagrams with the thermal stabilization loop disabled/enabled.

	Buckwalter [2] JSSC2012	Liu [3] JSSC2012	Li [4] ISSCC2013	Moss [5] ISSCC2013	This Work
Technology	130nm SOI	40nm CMOS	65nm CMOS	45nm SOI	**65nm CMOS**
Integration	Monolithic	Flip Chip	Wire Bonding	Monolithic	**Wire Bonding**
MRM Type	Depletion	Depletion	Injection	Injection	**Depletion**
MRM Q	~13000	~15000	~8000	~4000	**~5000**
Supply	+1.5V, -1.5V	1V, 2V	1V, 2V	1.1V, 1.5V	**1.2V, 2.4V**
WDM Channels	1	8	6	1	**5**
EQ	2-Tap FFE	N/A	2-Tap FFE	2-Tap FFE	**2-Tap FFE**
Swing	2.4$V_{pp\text{-}diff}$	2V_{pp}	4$V_{pp\text{-}diff}$	1.5V_{pp}	**4.4$V_{pp\text{-}diff}$**
Data Rate	25Gb/s	10Gb/s	5Gb/s	2.5Gb/s	**25Gb/s**
Transmitter Power/Channel	207mW	1.35mW	4.04mW	3.07mW	**113.5mW**
ER	6.5dB	7dB	12.7dB	3dB	**7dB**
MRM Stabilization	N/A	Static Thermal	Static Bias	N/A	**Dynamic Thermal**

Transmitter @ 25Gb/s	Power Breakdown	Thermal Tuning Loop	Power Breakdown
Local Clock Buffers & Amortized Global Distribution	20.5mW	Thermal DAC w/ 1kΩ Load	5mW
8-to-1 Serialization	31.2mW	FSM @ 100MHz	150μW
Output Stage & Pre-Driver	61.8mW	Comparator & Ref. DAC	23μW
Transmitter Total Power	**113.5mW**	Thermal Tuning Total Power	**5.17mW**

Figure 22.6.6: Performance comparison and transmitter power breakdown.

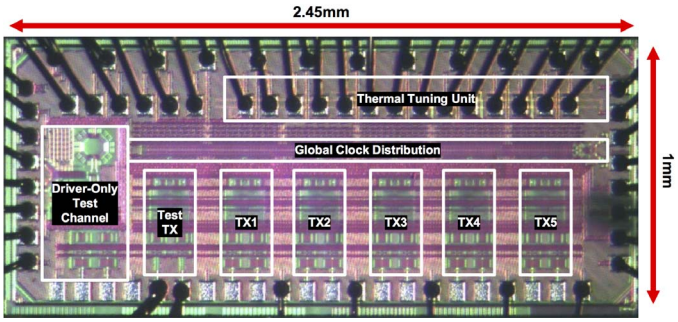

Figure 22.6.7: Die micrograph of the 5-channel transmitter IC with on-chip 2mm global clock distribution. Each transmitter channel occupies 0.1mm² area.

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