11.7 A 1.4 Gb/s DLL Using 2nd Order Charge-Pump Scheme with Low Phase/Duty Error for High-Speed DRAM Application

Kyu-hyoun Kim, Jung-Bae Lee, Woo-Jin Lee, Byung-Hoon Jeong, Geun-Hee Cho, Jong-Soo Lee, Gyung-Su Byun, Changhyun Kim, Young-Hyun Jun, Soo-In Cho

Samsung Electronics, Hwasung, Korea

Most timing circuits such as DLLs and PLLs adopt a charge pump both for the integration of phase information and the storage of locking information. In some circuits such as duty cycle correctors (DCC), it sometimes acts as a phase (or duty cycle) detector itself. Unfortunately, there are some nonideal characteristics in charge-pump circuits that result in considerable amount of phase errors [1]. These characteristics are 1) ripples, 2) mismatches between pull-up and pull-down currents, 3) output voltage dependent current mismatches and 4) charge injection/sharings due to parasitic capacitances. Those ripples could be minimized with a larger size of capacitor while slowing down the locking speed. Current mismatches between pull-up and pull-down currents can also be eliminated using differential structures. Differential type of charge pumps can also cancel out the charge injections only if the differential output voltage is zero. Therefore, it is the output voltage dependent mismatches that still remain unresolved. As the I/O speed goes higher and higher, a certain amount of phase error would gradually become the major factor of the speed limitation.

Another requirement for high-speed timing circuits is low power consumption. To reduce the power consumption, most of high-speed paths need to be shut down during power-down or stand-by mode, and restored from those modes instantly in order to sustain the system performance. Hence, all the locking information should be stored in a digital form. An ADC is normally required to convert the output voltage of the charge pump into digital bits. This needs large area and power to minimize the timing jitter produced by quantization. Although a successive iterative conversion can be used to avoid the problems related to ADCs, but the offset of the comparator directly leads to phase errors and handing over from a charge pump to an ADC would create other problems.

Figure 11.7.1 shows the basic principle of the 2nd order charge pump (SOCP) scheme. In the proposed scheme, an additional charge pump (CP2) is cascaded to the output of the original one (CP1), and the outputs of two charge pumps are added together to produce the final output. The transfer function of the macro of the SOCP is as follows:

$$\mathrm{OUT}(s) = \frac{A}{s}\cdot\left(1+\frac{B}{s}\right)\cdot \mathrm{IN}(s) = V_{CP1}(s)\cdot\frac{s+B}{s}$$

The equation implies that the final value ($s\rightarrow 0$) of V_{CP1} should be zero. Figure 11.7.1 shows the transient responses of three DLLs: a conventional one and two different kinds of SOCP. The DLL with the original SOCP is optimized to show critical damping behavior by adjusting the ratio between gains of two pumps to be A/B=2/K. Note that V_{CP1} always converges to zero regardless of the input phase or frequency, which means that the circuit is free from output voltage dependent mismatch error of the charge pump (CP1). Though the output of the second charge pump (CP2) is not zero, it does not affect the phase error between the input and the output because it is the original pump that detects the phase difference. The hybrid type SOCP scheme can be derived with replacing the second charge pump in the original scheme with a comparator and a counter. The counter increases or decreases depending upon the output value of the comparator so that the output of the charge pump would converge to zero. In this manner, the locking information can be seamlessly transferred from the analog form into the digital one.

Figure 11.7.2 shows a block diagram of the DCC using the hybrid SOCP scheme. The differential outputs of the charge pump would become the same level. Note that they need to be equalized so as to conserve the voltage across the capacitor during the standby mode as shown in the figure. The coefficients (A, B) of the SOCP should be chosen to compromise among locking times, bang-bang jitters, maximum duty/frequency ranges and storage ranges. Figure 11.7.3 shows the input stage of the duty amplifier where the analog and the digital information are weighted and summed. Transient responses corresponding to two different ratios are shown. The higher portion of digital information enables faster locking but suffers from ripples in both transition and steady states. In our design, the ratio of digital to analog is much smaller than unity, which is achieved mainly by using enough clock dividers for the counter and the DAC (updates once per 48 clocks).

Figure 11.7.4 shows the block diagram of the designed DLL adopting the SOCP scheme. The main configuration remains the same as the previous designs [2,3] where the coarse structure is a tapped delay line and the fine delay is controlled by phase interpolation between two phases out of the tapped delay line. The SOCP scheme is located at the end of DLL to correct the duty cycle of double data rate DQ and DQS (DQ Strobe). Two DLLs are designed for a 512Mb DDR2 SDRAM (800Mb/s) and a 256Mb GDDR2/3 SDRAM (1400Mb/s), respectively. Because of different frequency targets, detail circuits of those DLLs are slightly different, but they adopt the same DCC using the proposed hybrid SOCP scheme. The DLLs are fabricated using a 0.10μm DRAM process.

The SHMOO data in Fig. 11.7.5 shows the output data window of the fabricated DLL at the data-rate of 1Gb/s. The DLL operates at the data-rate up to 1.4Gb/s (700MHz). Figure 11.7.5 also shows the measured DQS waveform at 1Gb/s. The waveform includes some ISI effect mainly caused by the tester channel environment. A free running test mode is used to eliminate the ISI effect for the actual duty cycle measurement.

Figure 11.7.6 shows the comparison of DCC performances between the new and the previous designs. The measurement frequency of 250MHz (500Mb/s) is chosen to compare performances for the wider input duty cycle. The new design exhibits almost ideal characteristics for the input duty error less than ±500ps (±12.5% for 500Mb/s) as predicted in the simulation. For much larger input duty error, the new design also suffers from the finite correction range.

Figure 11.7.7 shows the die micrographs of DLLs fabricated as a 512Mb DDR2 SDRAM (upper) and a 256Mb GDDR2/3 SDRAM (lower), respectively. The DLL in DDR2 consumes 26mW at 450MHz and 0.9mW during standby mode with the standby exit time of only 2 cycles. The DLL in GDDR2/3 consumes 76mW at 700MHz and 1.1mW during power-down mode.

References :

[1] B. Razavi, "Design of Analog CMOS Integrated Circuits," *McGraw-Hill Book Company*, pp. 564-566, 2001.

[2] J.-B. Lee et al., "Digitally Controlled DLL and I/O Circuits for 500Mb/s/pin x16 DDR SDRAM," *ISSCC Dig. Tech. Papers,* pp. 68-69, Feb. 2001.

[3] K-H. Kim et al., "Built-in Duty Cycle Corrector Using Coded Phase Blending Scheme for DDR/DDR2 Synchronous DRAM Application," *Dig. Symp. VLSI Circuits*, pp. 287-288, Jun. 2003.

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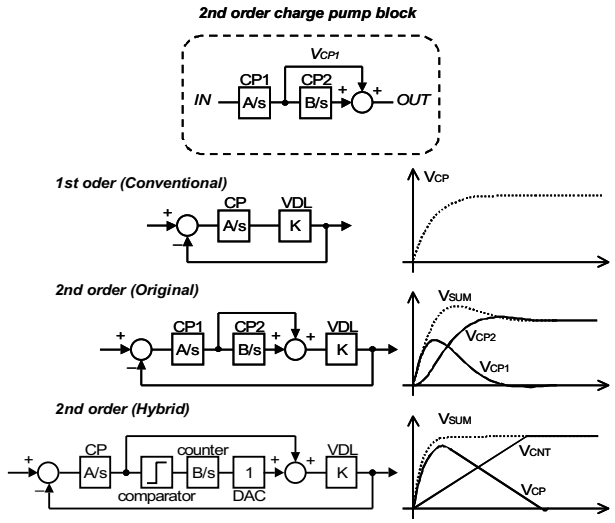

Figure 11.7.1: Basic principle of the SOCP scheme.

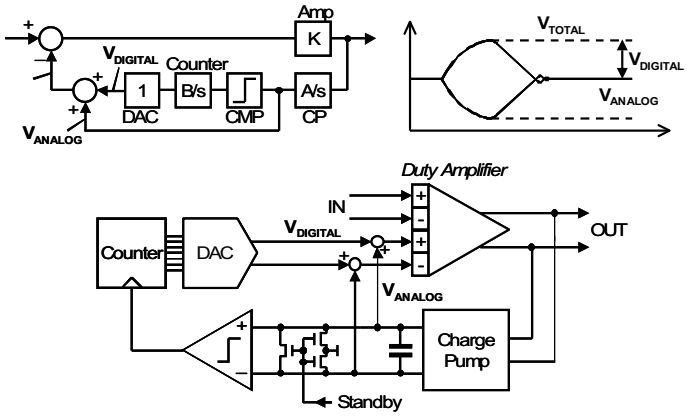

Figure 11.7.2: Block diagram of DCC using the hybrid SOCP scheme.

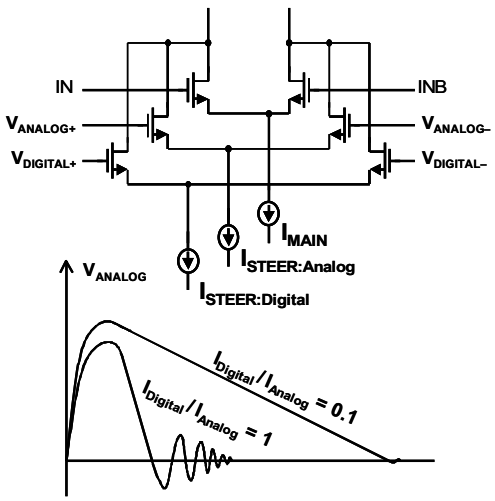

Figure 11.7.3: Input stage of duty amplifier and transient responses for various parameters.

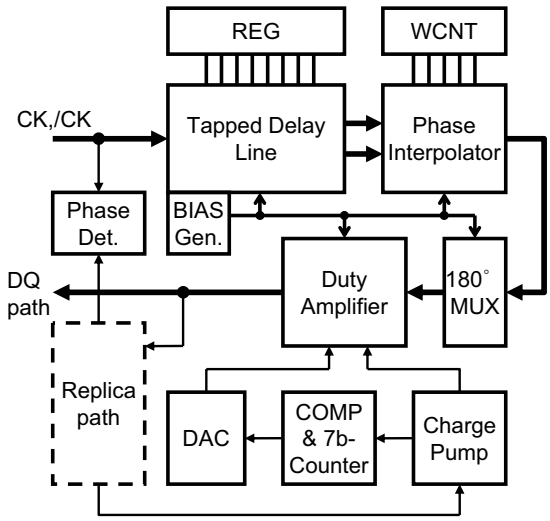

Figure 11.7.4: Block diagram of DLL.

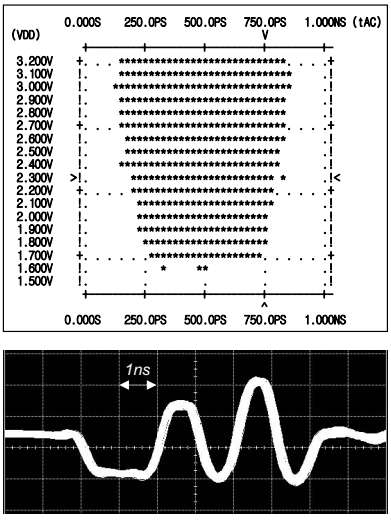

Figure 11.7.5: Valid data window and waveform measured at 1Gb/s.

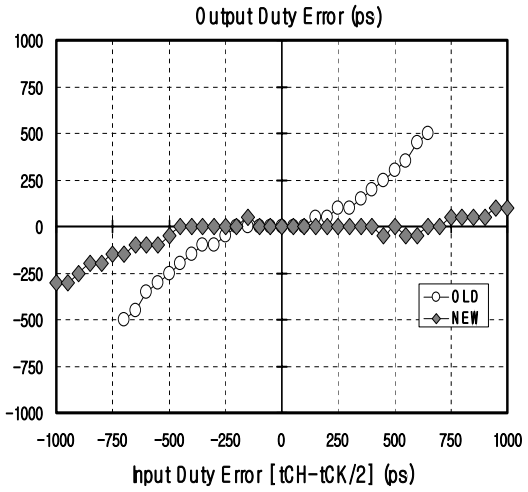

Figure 11.7.6: Measured DCC performances.

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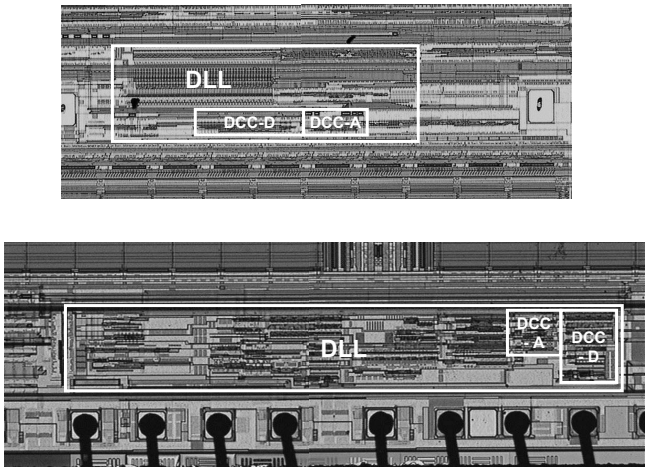

Figure 11.7.7: Die micrographs.

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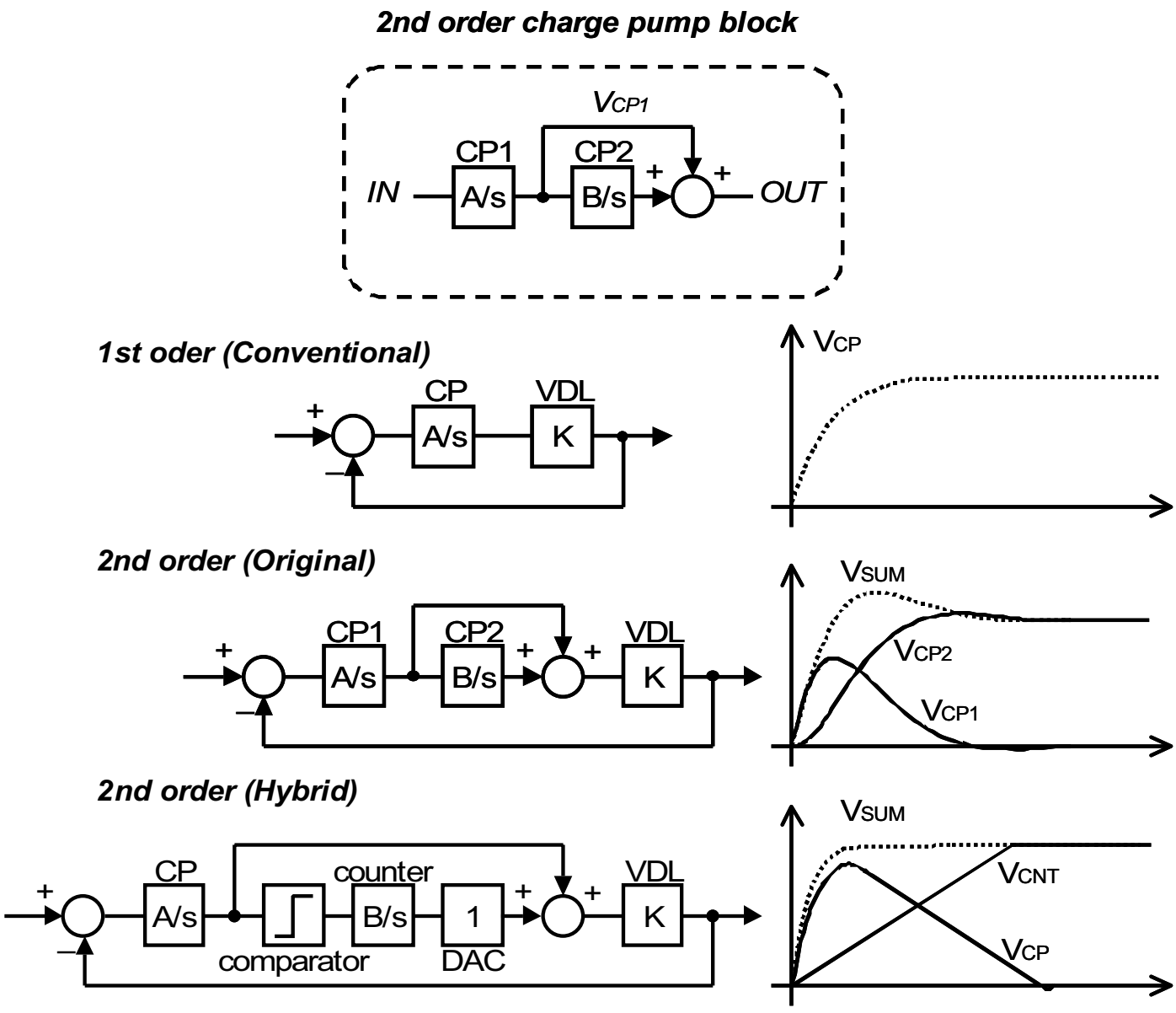

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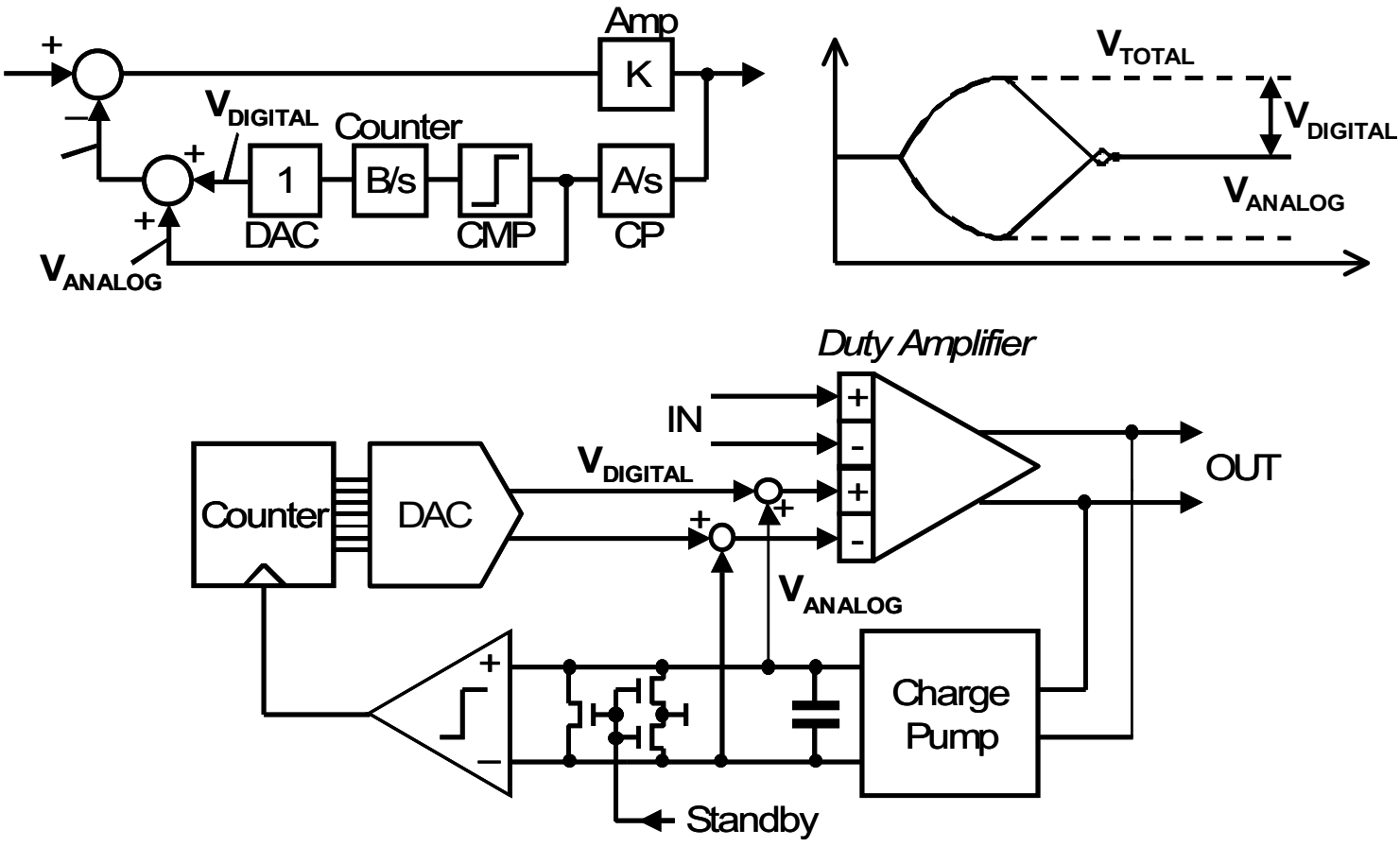
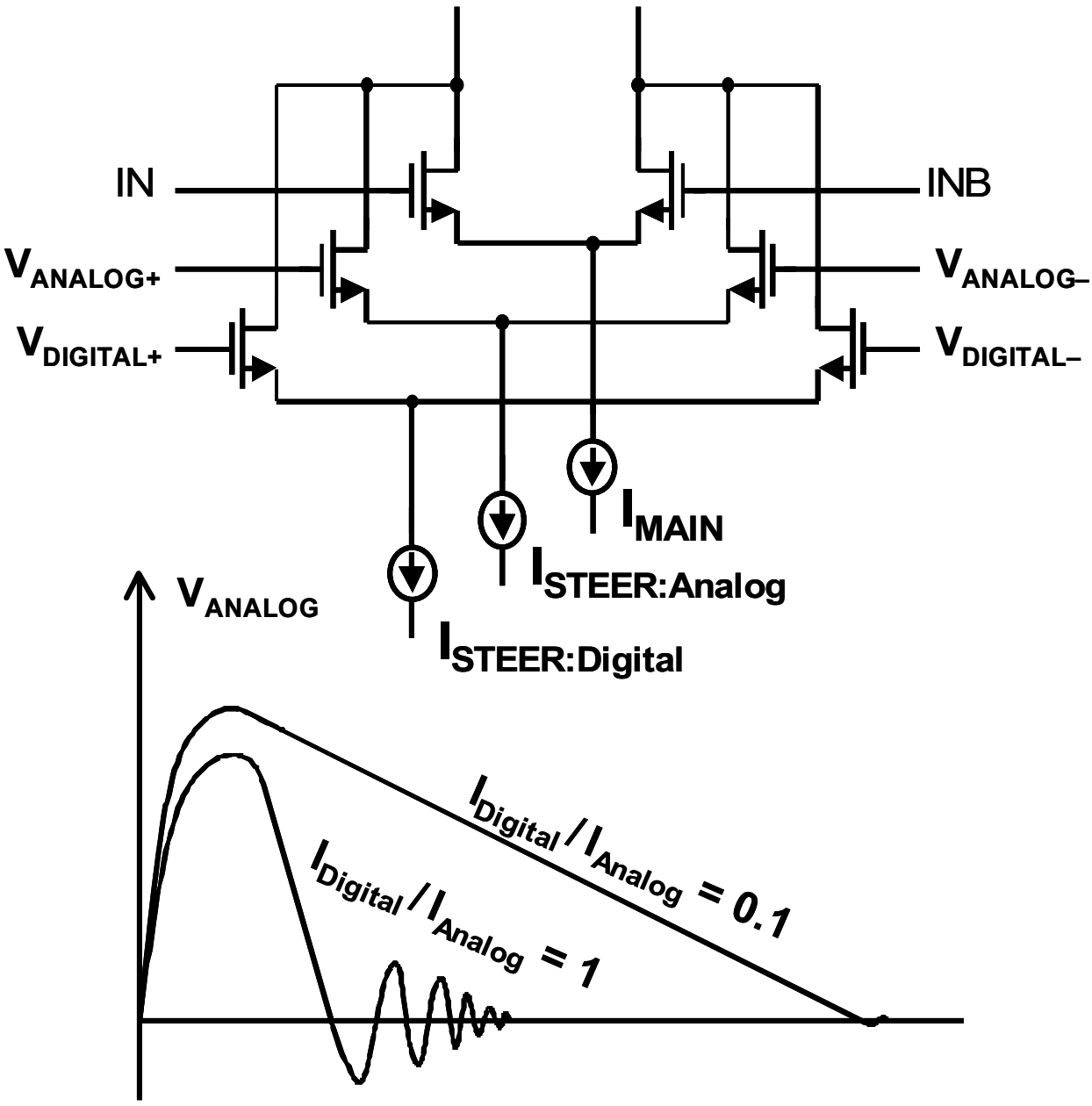


Figure 11.7.2: Block diagram of DCC using the hybrid SOCP scheme.



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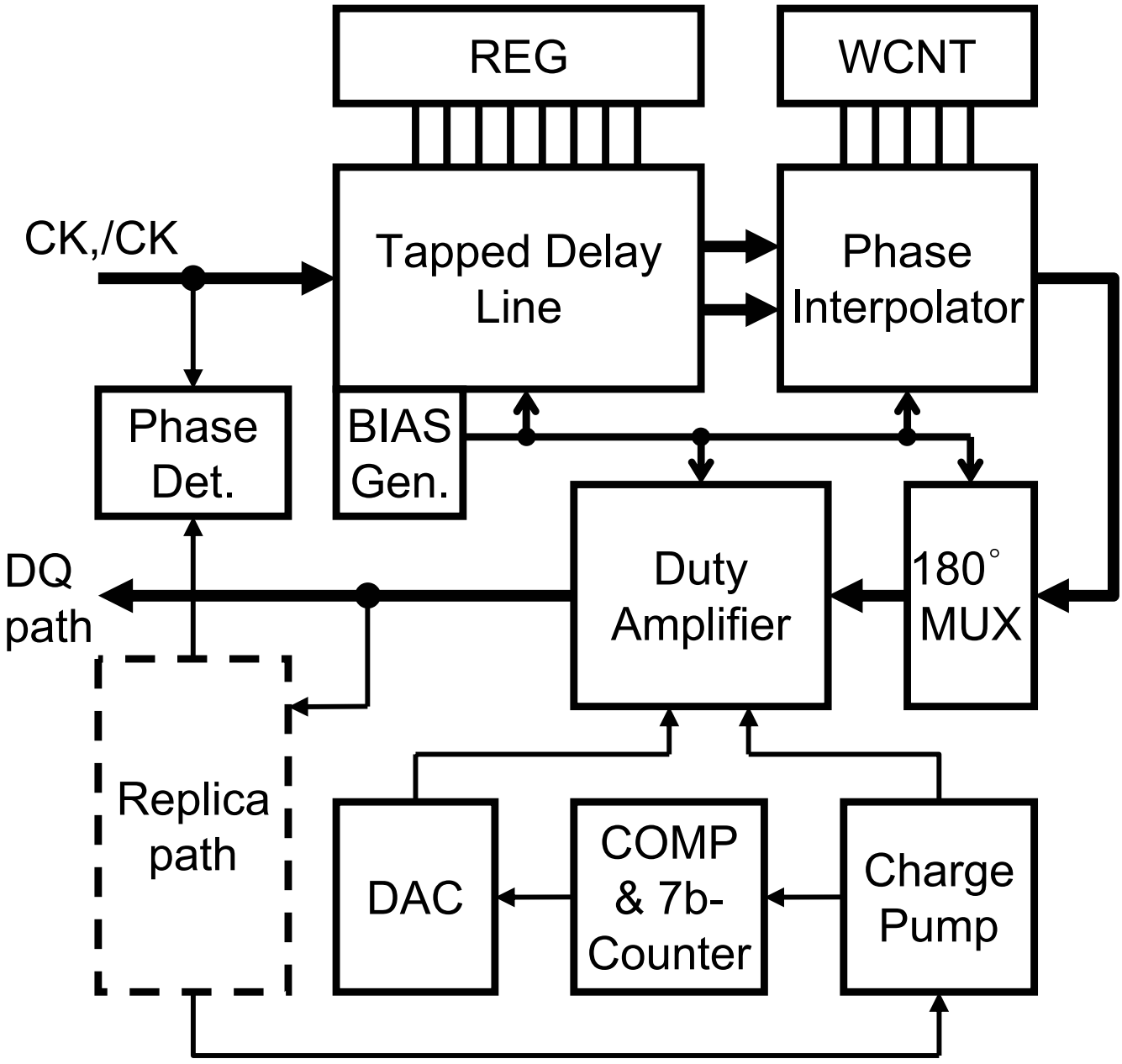

Figure 11.7.4: Block diagram of DLL.

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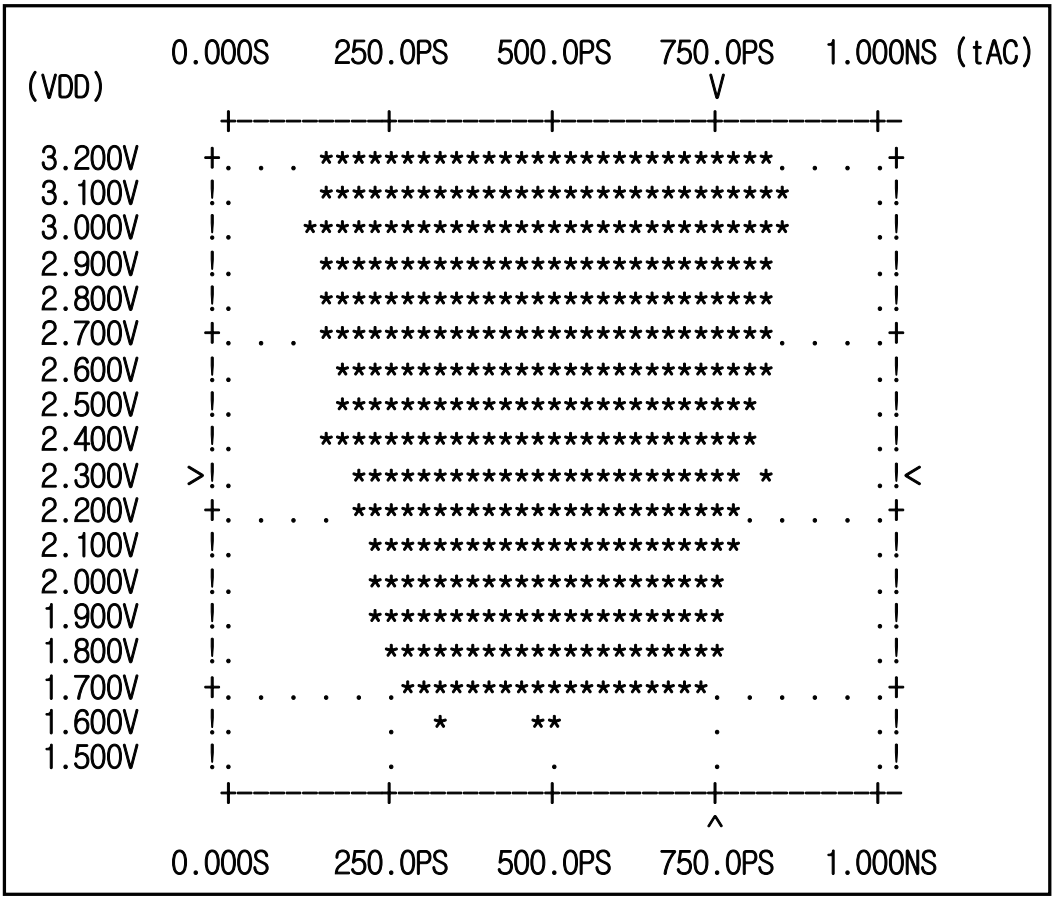

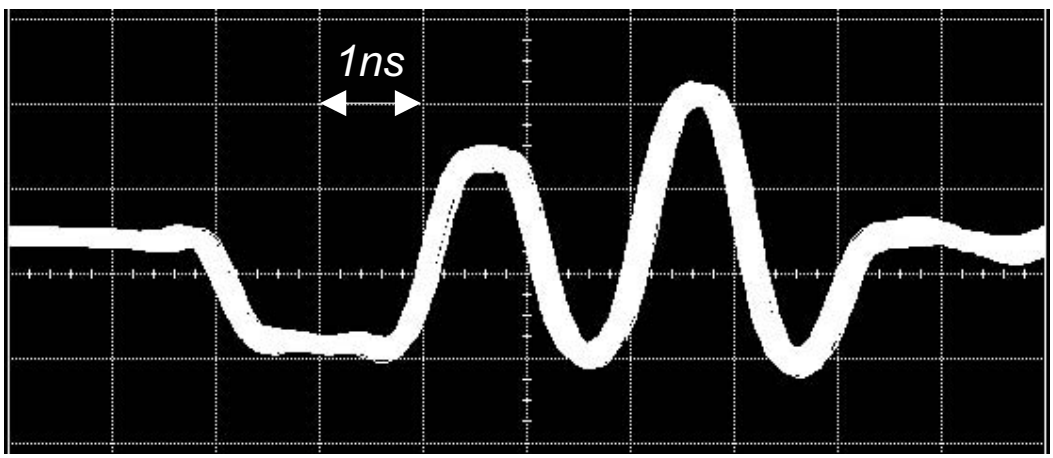

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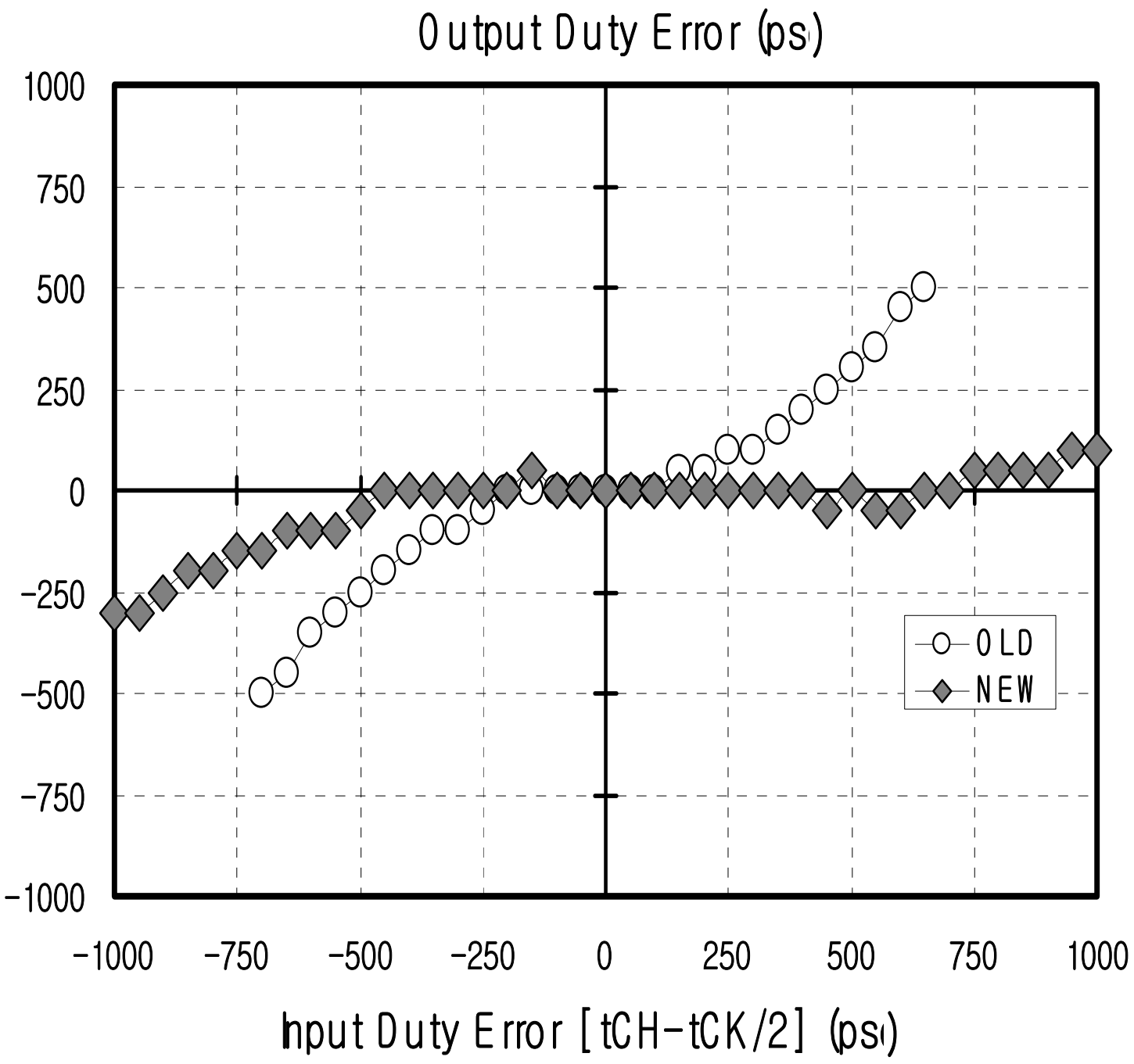

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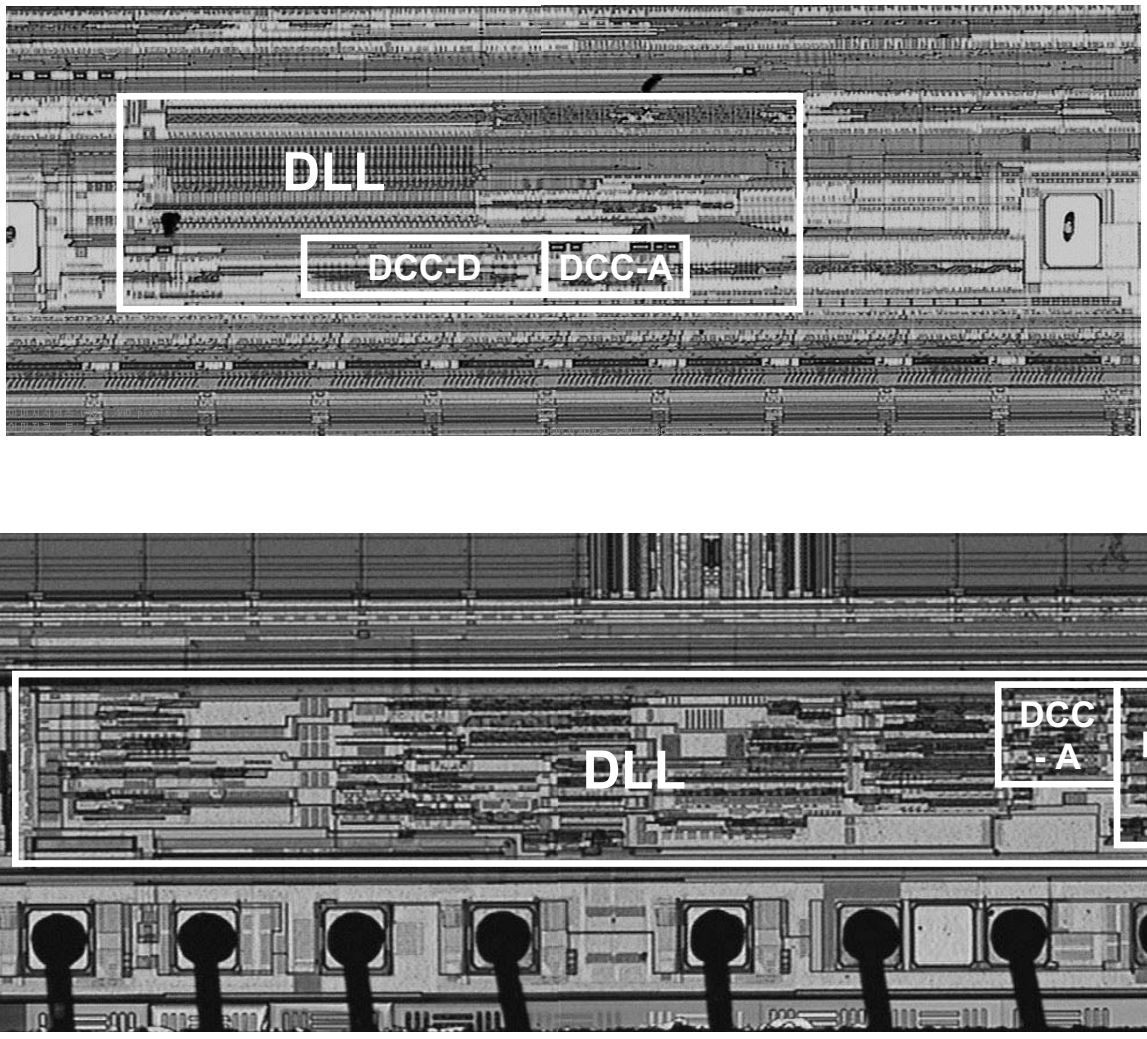

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