Effects of Basal Plane Dislocations on SiC Power Device Reliability

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Abstract—As silicon carbide power devices enter the commercial power electronics market there is a strong interest in all aspects of their reliability. This work discusses the degradation of MOSFETs due to basal plane dislocations (BPDs). During the forward bias of the MOSFET body diode, electron-hole recombination causes BPDs to fault and the resulting stacking faults in the drift layer degrade the MOSFET. As the stacking faults grow, the on-state conductivity of the MOSFET drift layer decreases, the off-state leakage of the drift layer increases, and the forward voltage of the body diode increases. Commercial 1200 V MOSFETs were stressed with a body current of 5 A or 10 A. The first generation of commercial MOSFETs showed significant degradation within minutes of stress time, whereas more recent MOSFETs did not show degradation for over 5 hours of stress time.

I. Introduction

The potential advantages of using silicon carbide to fabricate power electronics switches were recognized several decades ago. SiC devices that are now commercially available include MOSFETs and JBS diodes, and due to their superior capabilities, they have established a small and growing fraction of the power electronics market. Compared to silicon, SiC has a 3X larger bandgap, which results a 10X larger electric breakdown field and a lower intrinsic carrier density. The higher breakdown field decreases the required thickness of the device drift region and makes higher switching frequencies possible. The thermal conductivity of SiC is 3X higher than silicon's value so it more effectively conducts heat away from the devices active area. The development of SiC power devices also have the advantage that a majority of the processing steps developed for Si can be used with SiC. The oxidation of SiC forms a SiC/SiO_2 interface and similar implantation processes can be used to dope SiC either n-type of p-type. These characteristics make it possible to use similar equipment and techniques to fabricate familiar power devices such as MOSFETs, IGBTs, JBS diodes and PiN diodes with performance characteristics that are superior to their Si-based counterparts.

II. BPDs and Reliability

The effects of BPDs are more complicated than other materials extended defects in SiC. Other extended defects such as the various types of in-grown stacking faults can introduce a leakage path through the drift layer, but the leakage does not change due to device operation [1]. The adverse effects of BPDs were first reported by researchers working with ABB to develop 4.5 kV SiC PiN diodes [2]. ABB found that the forward voltage drop of SiC PiNs increased during forward voltage operation and identified the faulting of BPDs in the epitaxial drift layer as the source of the degradation, and they concluded that the stacking faults decreased the carrier lifetime. During the on state, the BPDs divide into two partial dislocations and form a stacking fault between them. These stacking faults are quantum wells trapping electrons and serve as a recombination site for electrons and holes that degrade the local lifetime, which reduces the carrier flow [3]. Later work showed that the stacking faults from BPDs are also potential barriers that impede current flow in majority carrier devices such as MOSFETs [4], [5]. The stacking faults originating from the BPDs also affect the leakage of SiC devices including MOSFETs by increasing the leakage in the off-state [5], [6].

The essence of the distinction between the effects of BPDs and other extended defects is that before faulting, the BPDs have a negligible effect on device performance. The degradation to both bipolar and unipolar devices is due to the stacking faults that develop from the BPDs. Degradation from other extended defects is primarily a yield challenge. Their effects are much more quickly and easily observed by screening of the dies on a wafer. In contrast, BPDs pose more of a reliability challenge. The development of stacking faults in a MOSFET or other device depends on the details of the switching cycle being used so the BPD degradation requires reliability testing.

With the maturing of SiC bulk (substrate) and epitaxial growth techniques, the concentrations of BPDs originating in the substrate and entering the epitaxial drift layer has been decreased several orders of magnitude from the original observations by ABB. BPD density in substrates has dropped two orders of magnitude over the last decade and is now typically 300 BPD/cm2 [7]. Another improvement was the change from 8° to 4° of the offcut angle of wafers to increase the number of substrates that could be cut from a boule [8].

On 8° substrates about 10% of the BPDs in the substrate propagate into the epitaxial layer and continue through the whole thickness of epitaxial layer. In contrast, on 4° substrates, a similar fraction enter the epitaxial layer but they convert into benign threading edge dislocations (TEDs) within the first few microns of epitaxial growth. However, a BPD

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causes degradation, even if only a short part of it is in the epitaxial drift layer, because it forms a stacking fault that expands to the top of the drift layer. Epitaxial growths for power devices normally start with a buffer doped nearly as high as the substrate to keep the BPD out of the drift layer and to keep e-h recombination away from the BPD. By optimizing the epitaxial growth, it is possible to reduce the BPD concentration in the drift layer to 0.1 BPD/cm^2 [9]. . The geometry of a BPD entering the epitaxial layer is shown in Figs. 1 and 2. Figure 1 is an ultraviolet photo luminescence (UVPL) plan-view image of several BPDs. Figure 2 is a 3D schematic showing the path of BPDs within the epitaxial layer. The two schematics compare a BPD that fully traverses the epitaxial layer with a BPD that converts into a TED during the epitaxial growth.

Contrary to earlier assumptions, it has been shown that stacking faults entering the drift layer can originate at BPDs in the substrate or epitaxial buffer layer. Using UV illumination corresponding to ~1000 A/cm^2, BPDs from a nitrogen-doped buffer layer, 3x10^{18}/cm^3, were observed to slowly fault until they reached the drift layer, doped 1x10^{15}/cm^3, and then rapidly expanded to the surface of the drift layer [10]. The buffer layer had a minority carrier lifetime of 100 ns. Recent work has also shown that a BPD that converts into TED at the substrate/epi interface can create stacking faults in the epitaxial layer [11], [12]. One difference is that many of the stacking faults originating from BPDs in at the substrate/epi interface expand to cover a larger area of a device so each BPD leads to more device degradation.

The control of BPDs is complicated by the fact that BPDs can be created and introduced into the device drift layer in multiple ways. Inclusions resulting from downfalls during epitaxial growth are a combination of misoriented 4H and 3C polytypes [13]. They introduce a local stress field that produces a cluster of BPDs surrounding the inclusion. An example is shown in Fig. 3.

Another important source of BPDs that has recently been observed is BPDs introduced during wafer processing [14]. These BPDs are formed by the combination of Al implantation and the activation anneal used to form p+ contacts in MOSFETs or other devices. The BPDs originate from the implanted region and glide through the epitaxial layer during the annealing as shown in Fig. 4. Their formation is enhanced at corners formed by RIE etching through the implanted area, but oxidation removes surface damage at the corners and suppresses BPD creation [15]. Figures 4 and 5 illustrate the formation of BPDs during the implantation/anneal processes. They show BPDs introduced into areas originally free of BPDs. If the Al implantation is sufficiently high, such as for p+ contacts, BPDs can be introduced. The BPDs are thought to be created around small defect areas in the implanted layer and expand by gliding through the epitaxial layer during the annealing.

Examples of BPD degradation on early commercial 1200 V MOSFETs (gen 1) and the improvement in more recent 1200 V MOSFETs (gen 2) are shown in Figs.6-11. Three characteristics of the MOSFETs are shown: body diode I_{DS}-V_{DS} curves, MOSFET on-state I_{DS}-V_{DS} curves, and MOSFET off-state leakage. The MOSFETs were stressed by turning on the body diode as shown in the figures to cause BPDs to fault and degrade the MOSFETs. The case temperature during stressing was kept below 100°C. Gen 1 MOSFETs have significant degradation, while no degradation is observed in gen 2 MOSFETs.

III. Conclusion

While SiC power devices have significant advantages over their Si based counterparts, the issue of extended defects, especially BPDs, must be carefully managed to produce reliable SiC devices. Examination of the characteristics of BPDs has resulted in improved understanding of their development and their effects on device performance. The insights gained through the study of the properties and behavior of BPDs have enabled decreasing the concentrations of BPDs, preventing the faulting of BPDs within the device drift layer and thereby limiting degradation to SiC device reliability.

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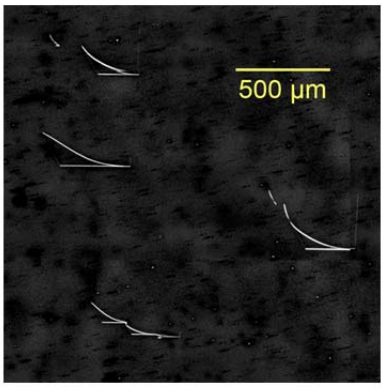

Fig. 1. UVPL image of five individual BPDs originating from the substrate. Shorter BPDs convert to TEDs during epi growth.

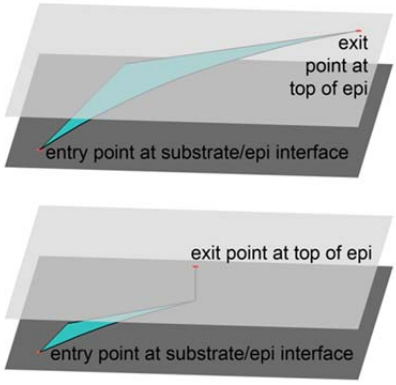

Fig. 2. Schematics of BPDs originating from the substrate: top BPD spans total epi layer, bottom BPD converting to a TED during epi growth.

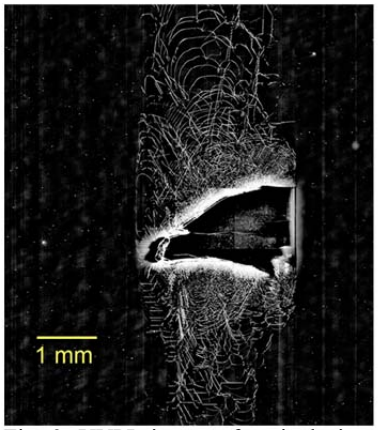

Fig. 3. UVPL image of an inclusion formed during epi growth and the cluster of BPDs the inclusion induces around it due to local stress.

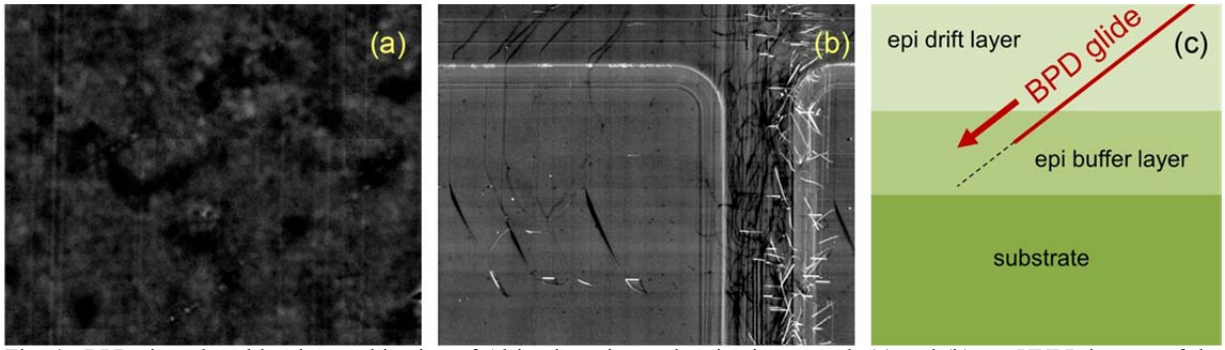

Fig. 4. BPDs introduced by the combination of Al implantation and activation anneal: (a) and (b) are UVPL images of the same area of a wafer before and after processing. The bright and dark lines in (b) are BPDs introduced by the processing. None of these BPDs are present in (a). Frame (c) illustrates the observation that the BPDs originate in or near the implanted layer and glide towards the substrate during the anneal.

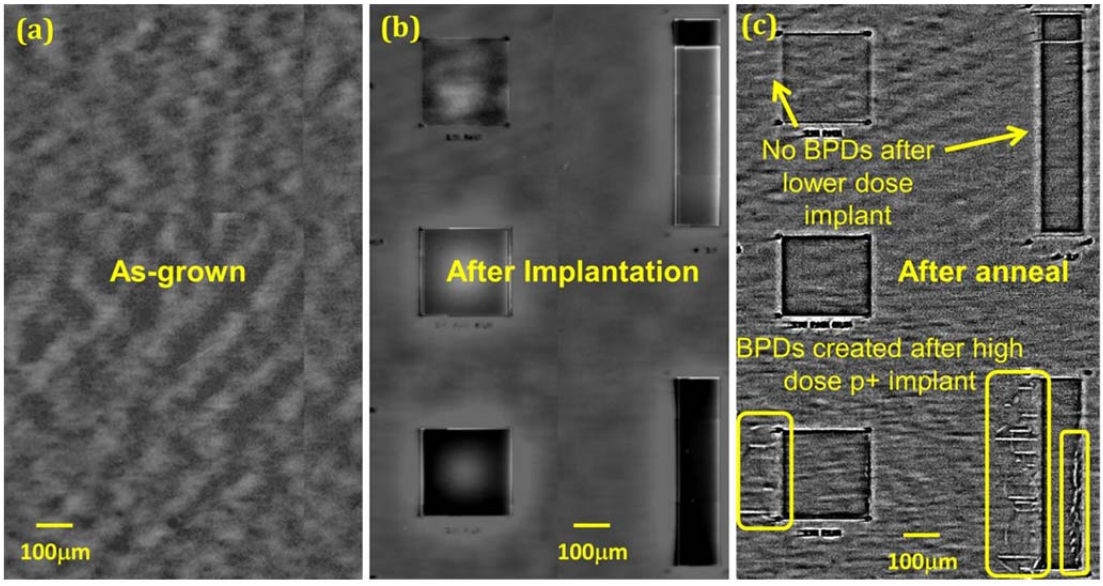

Fig. 5. UVPL from the same wafer area showing the introduction of BPDs during processing. There are no BPDs in (a) as-grown and (b) after-implantation. In (c) BPDs appear after annealing (see boxes). Note that BPDs are only introduced at the higher Al p^+ dose and not during the lower p dose.

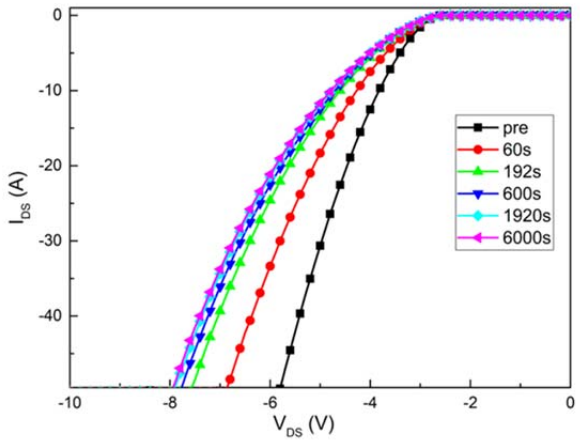

Fig. 6. Increases to the MOSFET (gen 1) body diode I-V curve due to BPD faulting caused by current stressing of 5 A for the accumulated times shown. V_{gs} = -5V to eliminate current through the channel.

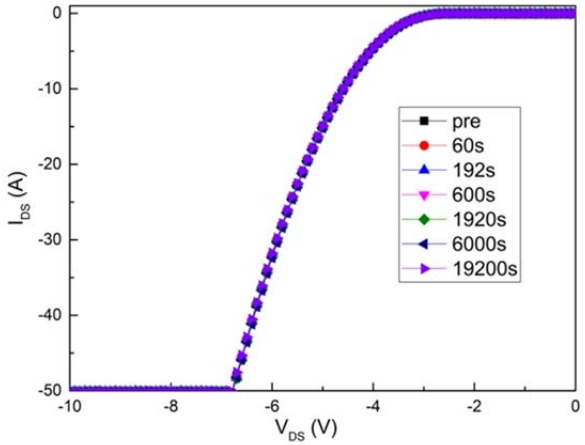

Fig. 7. No changes in the MOSFET (gen 2) body diode I-V curve during stressing of 10 A for the accumulated times shown. V_{gs} = -5V to eliminate current through the channel.

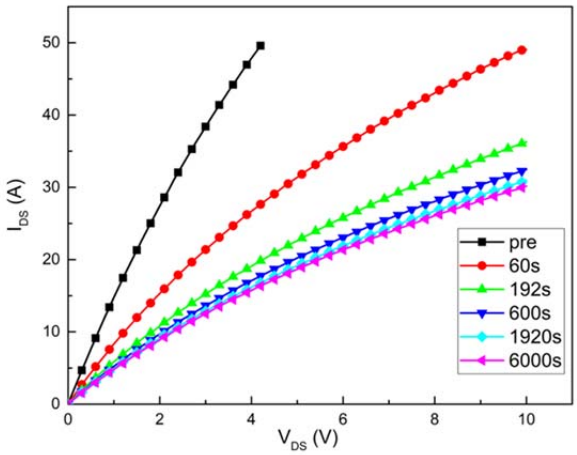

Fig. 8. Decreases to the MOSFET (gen 1) I-V conduction curve at V_{gs} = 20 V due to BPD faulting caused by current stressing of 5 A for the accumulated times shown.

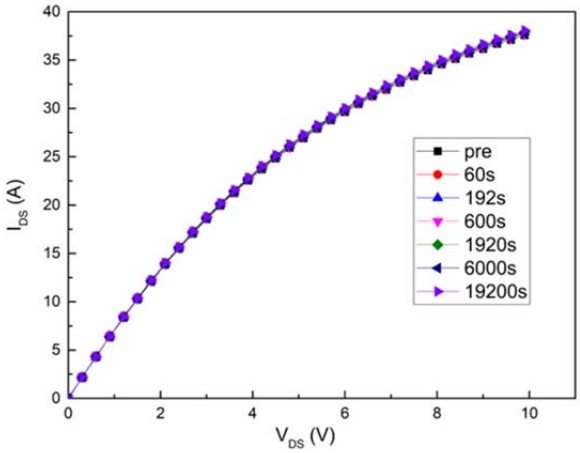

Fig. 9. No changes in the MOSFET (gen 2) I-V conduction curve at V_{gs} = 20 V during stressing of 10 A for the accumulated times shown.

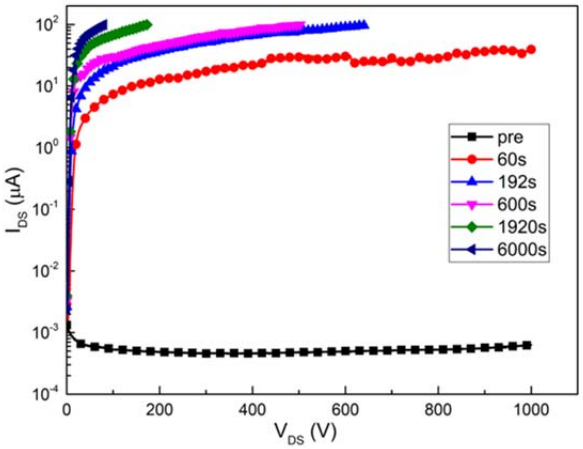

Fig. 10. Strongly increasing leakage in gen 1 MOSFET due to BPD faulting caused by current stressing of 5 A for the accumulated times shown.

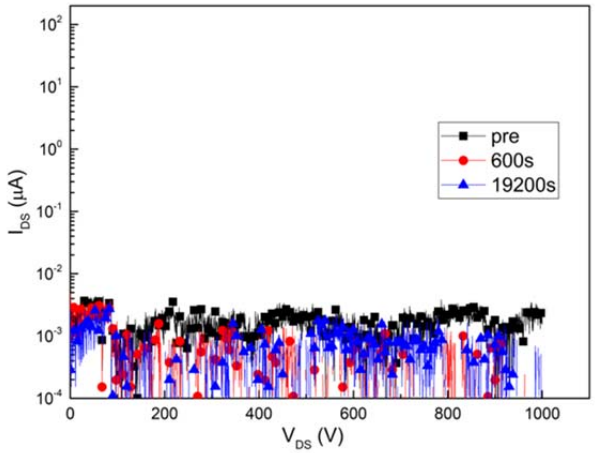

Fig. 11. No leakage increase in gen 2 MOSFET induced by current stressing of 5 A for the accumulated times shown.