A Process and Temperature Insensitive CMOS Linear TIA for 100 Gbps/λ PAM-4 Optical Links

Kadaba Lakshmikumar, Alexander Kurylak, Manohar Nagaraju, Richard Booth, Joe Pampanin
Transceiver Module Group,
Cisco Systems,
Allentown, PA, USA

***Abstract*— A linear TIA for a 53 GBd PAM-4 optical link to support 100 Gbps data rate on a single wavelength is reported. Designed in a 16 nm FinFET CMOS process, the chip consumes 61 mW with < 2 % THD at 600 mVpp differential output swing, 27 GHz bandwidth, and an input referred noise density of 18.3 pA/ √ Hz. Transimpedance can be programmed from 63 to 80 dBΩ in 0.5 dBΩ steps. Dynamic voltage scaling tightly controls the bandwidth and in-band peaking across PVT variations to improve the parametric yield.**

Keywords— TIA, optical links, PAM-4, dynamic voltage scaling

I. Introduction

The interconnection of compute, storage, and switching nodes in modern large-scale data centers demands high bandwidth optical interfaces. The IEEE Standards Association is working to define the transport of 100 Gbps of data on a single wavelength (λ) of light [1]. At such rates, the bandwidth requirement of the popular bi-level (PAM-2) non-return-to-zero (NRZ) signaling scheme is too large and expensive for the electrical-to-optical and optical-to-electrical interfaces. Advanced modulation techniques such as pulse-amplitude-modulation with four levels (PAM-4) are needed to reduce the required bandwidth. Fig. 1 shows a transceiver system-in-package (SiP) consisting of an electrical IC (EIC) with a monolithically integrated transimpedance amplifier (TIA), flip-chipped on a photonics IC (PIC). The photodiode in the PIC converts the received PAM-4 optical signal to a current, which is then transformed into a voltage and amplified by the TIA in the EIC. The TIA needs to be linear (< 5 % THD) to produce four equally spaced levels. Here, we present a test chip designed to characterize such a linear TIA for a 100 Gbps/λ link with < 2 % THD in a CMOS process. The rest of the paper is organized as follows: Section II describes the basic amplifier topologies for a TIA application, Section III describes the circuit details of the full signal chain and Section IV reports the measured results.

II. Topological Considerations

A. Basic building block

High bandwidth linear TIAs are often realized in InP or SiGe BiCMOS technologies, where the bipolar transistors offer high speed, low noise, and sustain high voltages [2, 3]. However, the signal processing and logic requirement of a monolithic transceiver IC are best realized in CMOS. Thus the

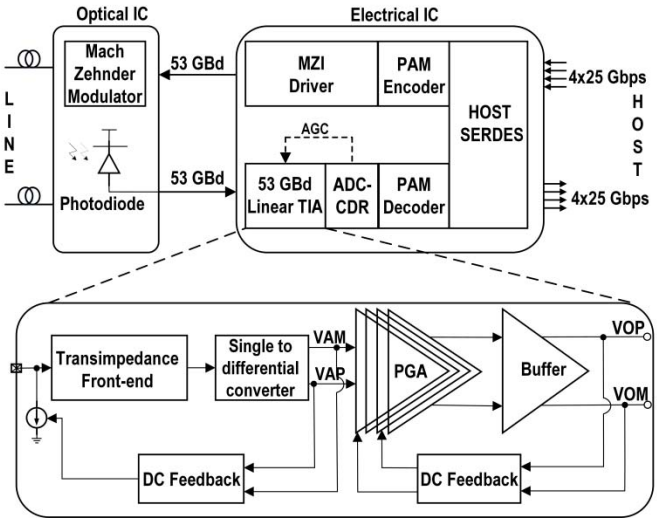

Fig. 1: Block diagram of a 100 Gbps/λ transceiver

linear TIA is designed in a fine-line CMOS process with the major technological challenge of signal compression due to limited supply voltage. A CMOS inverter, biased in the linear region, is chosen as the basic building block since it offers the highest swing for a given supply voltage and level of distortion. Compared to a non-push-pull driver such as a common-source transistor driving a resistive load, a push-pull driver offers a more linear transconductance. Hence, we use a CMOS inverter as the amplifier in all stages. Referring to Fig. 2 (a), the large-signal voltage-current relationship in a CMOS inverter may be written as:

$$i_o = i_n - i_p \approx \left(k_n V_{GTn} + k_p V_{GTp}\right) v_i + \left(\frac{k_n}{2} - \frac{k_p}{2}\right) v_i^2 \qquad (1)$$

where $V_{GT} = V_{GS} - V_T$ *and* $k = \mu C_{ox}(W/L)$.

The non-linearity arising from the square-law behavior is completely cancelled when the k's of the p- and n-channel transistors are perfectly matched. Even when there is a mismatch, the second order non-linearity is proportional to difference in the k values. Mobility degradation due to transverse electric field, and channel length modulation, which are severe in low-supply voltage environments, produce odd-order non-linearities. Inclusion of these effects into the MOS transistor model, however, makes Eq. (1) intractable. Hence, we use a circuit simulator to evaluate different topological options.

978-1-5386-2483-8/18/$31.00 ©2018 IEEE

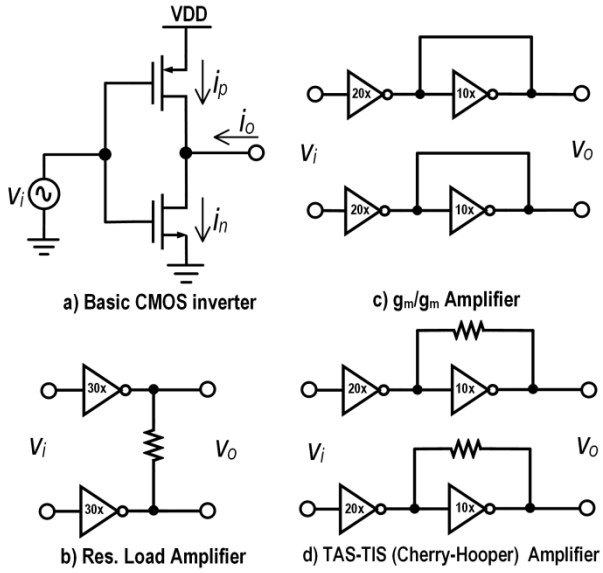

Fig. 2: Comparison of different amplifier topologies

B. Voltage-gain topology

Three voltage-gain topologies were investigated as shown in Fig. 2. A CMOS inverter can be loaded with a resistor as shown in Fig. 2(b). In Fig. 2(c), the load resistor is replaced by a shorted inverter to investigate the possibility of cancellation of the non-linearity of the driver with that of the load. Finally, a trans-admittance trans-impedance (TAS-TIS) circuit (Cherry-Hooper), which is a very popular high-bandwidth structure, is shown in Fig. 2(d). The size of the inverters is adjusted to have the same power dissipation for all three variations. Note that all these structures are pseudo-differential, and have a low-frequency gain of approximately 2 (6 dB) and produce 600 mV differential peak-to-peak swing. Table I summarizes the simulated linearity. The inverter load structure (Fig. 2(c)) has the best linearity, suggesting significant cancellation of the driver and load non-linearities. The TAS-TIS has the worst linearity. Other disadvantages of Fig. 2(b) and Fig. 2(d) are that the resistance may have to be tuned in addition to the transconductance of the inverters to achieve a tight gain, bandwidth and output impedance. Further, resistors occupy much larger area than an equivalent resistive load realized with an inverter. Based on this investigation, we have used the topology in Fig. 2(c) for all the gain functions as described in the next section.

Table I: Comparison of simulated linearity of 3 amplifiers

	(b)	(c)	(d)
2nd harmonic (dBc)	-182.2	-185.1	-185.2
3rd harmonic (dBc)	-40.12	-53.76	-27.38
4th harmonic (dBc)	-185.4	-192.6	-185.4
5th harmonic (dBc)	-77.44	-71.63	-62.07
THD (%)	0.98	0.2	4.13

III. Circuit Details

A. Signal path

The TIA consists of a transimpedance front-end, single-ended-to-differential converter, programmable gain amplifiers (PGA) and an output buffer. Fig. 3 depicts the entire signal path consisting of dc-coupled inverters. The front-end of the TIA is a shunt-feedback inverter, which converts the current output of a photo-detector to a voltage. The feedback resistor is realized using MOS devices operating in triode region to reduce parasitics and achieve a higher bandwidth as compared to a programmable resistor. Any variation in the resistance value over PVT is minimized by dynamic voltage scaling (DVS) as discussed later. An inverter driving a shorted inverter as a load generates a complementary signal. The amplitude of the complementary signal is determined by the ratio of the sizes of the driving (INV1) and load (INV2) inverters, and hence is very tightly controlled. The additional phase shift of the complementary path is very small as the pole frequency is near the transit frequency (f_t) of the devices. This single-ended to differential arrangement is more precise than a TAS-TIS circuit [4] because the amplitude and phase of the signals do not have any resistor dependency.

The complementary signals then pass through a cascade of 3 coarse (0 or 5 dB) programmable gain stages (PGA-C) and a fine gain stage with 0.5 dB steps (PGA-F). The load in PGA-C

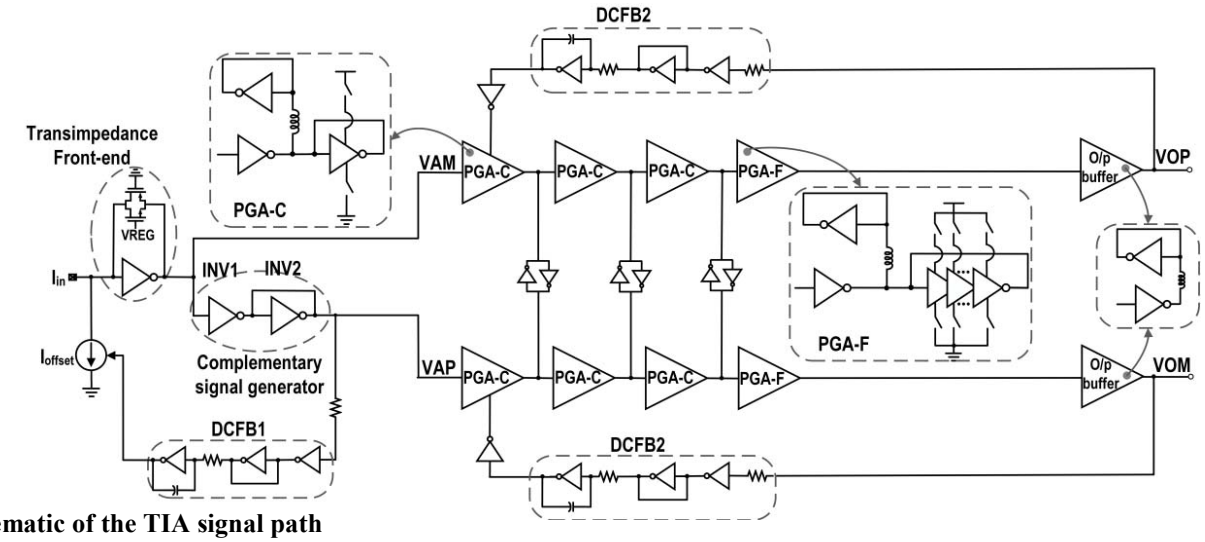

Fig. 3: Schematic of the TIA signal path

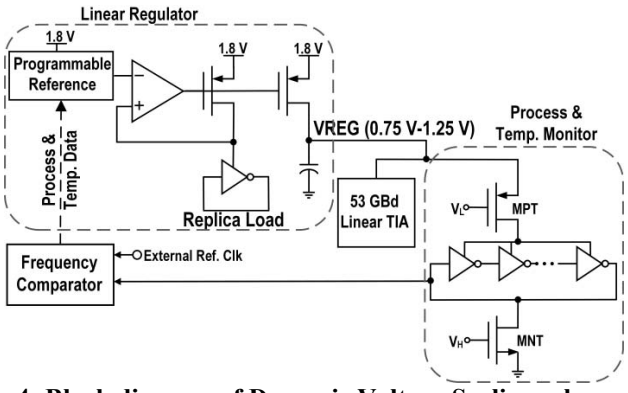

Fig. 4: Block diagram of Dynamic Voltage Scaling scheme

is a fixed shorted inverter in parallel with a switchable-shorted inverter. For PGA-F, a number of smaller switchable-shorted inverters are used. The last stage is an output buffer, again with a shorted inverter load to offer 50 Ω output impedance. In all these stages, the transconductance non-linearity of the load partially cancels the non-linearity arising from the driver to improve the overall linearity. Shunt peaking inductors present in all the stages extend their bandwidth at higher gain settings. At lower gain, where the bandwidth is inherently more, the Q of the load decreases thus preventing any undesirable peaking. Cross-coupled inverters between the complementary signal paths minimize any amplitude and phase mismatch. Using multiples of unit-sized inverters eliminates systematic offset. The average value of the photo current is subtracted at the input with a dc feedback loop (DCFB1). A second dc feedback loop (DCFB2) minimizes the random mismatch effects, and prevents saturation of the gain stages. The dc loops also use unit-sized inverters and provide a high-pass corner of less than 100 kHz for the signal. Automatic gain control (AGC) is implemented via firmware by monitoring the A/D converter (ADC) output in the clock and data recovery (CDR) block.

B. Dynamic voltage scaling (DVS) scheme

Traditional designs employing differential pairs have good common-mode and power-supply noise suppression. Here, the dc-coupled inverters have no such immunity. Therefore, an on-chip programmable linear regulator (Fig. 4), that provides isolation from supply and substrate noise, powers the entire signal path. The self-biased inverter, which is the basic building block of the TIA, is very sensitive to PVT variations. Therefore, the regulated voltage is made to adapt to PVT variations. The transconductance of an MOS transistor biased in saturation is given by:

$$g_m \approx k(V_{GS} - V_T)$$

As the transistors in an inverter are biased at $V_{GS} \approx VDD/2$, by appropriately controlling VDD, process and temperature variations can be tuned out. Similarly, for the feedback transistors in the front end, which are biased in the triode region, the drain-source conductance is given by:

$$g_{ds} \approx k(V_{GS} - V_T)$$

where $V_{GS} \approx VDD/2$. Thus, the gain and bandwidth of the TIA can be tightly controlled. The range of the regulated output voltage is from 0.75 to 1.25 V across PVT. However,

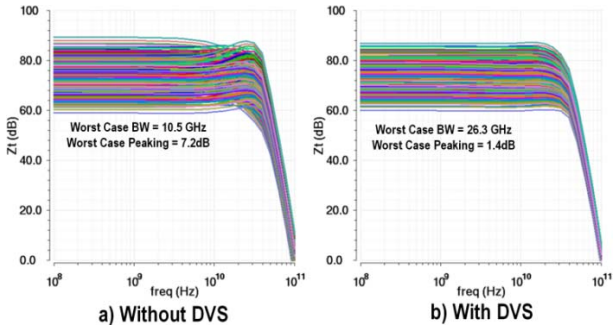

Fig. 5: Simulated TIA |Zt| across PVT (a) without DVS, and (b) with DVS

the voltage across any two terminals of a transistor does not exceed 0.9 V. A ring oscillator (RO) made of the same unit-sized inverter serves as a PVT sensor. Although voltage swing in the TIA is well below rail-to-rail, a ring oscillator swings from rail-to-rail. Thus, MOS devices in triode region, MPT and MNT, are added to prevent over-voltage. The frequency of the RO is compared with a reference clock. The digital output of the frequency comparator represents the process-corner and temperature of the TIA. The linear regulator is programmed via a firmware feedback loop to get a targeted RO frequency.

Fig. 5 compares the simulated transimpedance of the complete TIA without DVS (Fig. 5(a)) and with DVS (Fig. 5(b)) across process and temperature corners, and PGA gain settings (432 combinations). With DVS, the worst-case bandwidth improves from 10.5 GHz to 26.3 GHz and the worst-case peaking decreases from 7.2 dB to 1.4 dB.

IV. Measured Results

The 16nm FinFET test chip measures 1.24mm x 1.16 mm (Fig. 6). It is mounted on a silicon electrical interposer with 50 Ω traces and probe-pads for input and outputs. Fig. 7 illustrates measured small-signal parameters for a gain setting of 78 dBΩ. With the 50 Ω environment of the test setup, s-parameters are measured and converted into transimpedance by $Z_t \approx Z_o \cdot s_{21}/(1 - s_{11})$. With a bandwidth of 27 GHz, a group delay variation of < 20 ps is observed. The bandwidth of the TIA is plotted as a function of normalized RO frequency for 5 samples from typical, slow, and fast lots. Excellent correlation between RO frequency and TIA bandwidth is observed, thus validating the DVS scheme. The

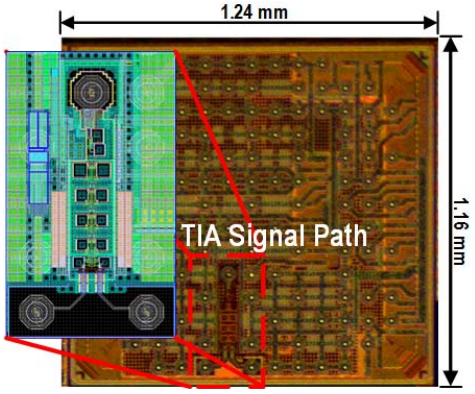

Fig. 6: Chip micrograph of the proposed TIA

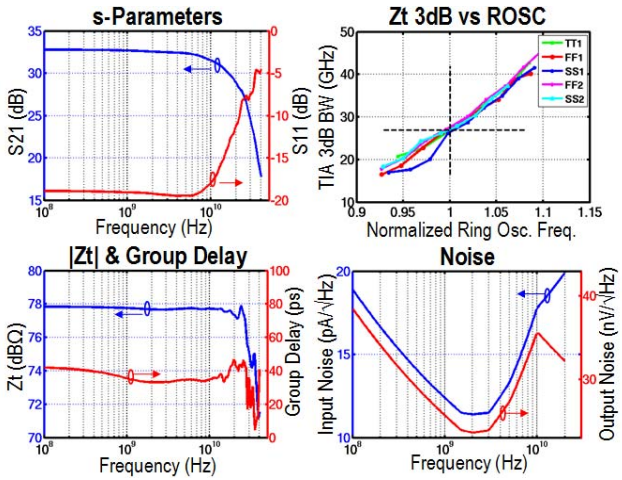

Fig. 7: Measured small signal parameters of the TIA

output and input referred noise spectral densities are also shown. The average input current noise density is 18.3 pA/√Hz. Linearity and gain results are shown in Fig. 8. The spectrum analyzer capture shows the fundamental and harmonics of a 400 MHz sinusoid measured differentially with the help of a balun for an equivalent differential swing of 600 mVpp. In contrast to low-speed circuits where linearity can improve due to negative feedback, all gain stages here are open-loop. Hence, linearity is not a function of frequency and the THD value would be valid at higher frequencies as well. Low-level even harmonics indicate well-matched pseudo differential branches. THD vs. signal swing is also presented for devices from different process corners. As the DVS mechanism sets a lower supply voltage for fast processes, the THD is slightly higher, but still below 2% for a 600 mVpp swing. The TIA has a gain range of 63 to 80 dBΩ in 0.5 dBΩ steps in order to fill the full-scale range of the ADC. Fig. 9 depicts the optical to electrical conversion performance of the TIA, when mounted on a PIC, at a data rate of 53.125 GBd with a PRBS13Q pattern. With a 0.954 Ratio Level Mismatch (RLM) optical input and 4.5 dB extinction ratio, an equivalent output 600 mVpp with a RLM of 0.95 was observed.

Table II provides a performance comparison of this work with other state-of-the-art TIAs. The figure-of-merit (FoM), as defined in [5], is the highest for a linear TIA published to date, even with the power overhead needed for DVS, and compares very favorably with PAM-2 parts as well.

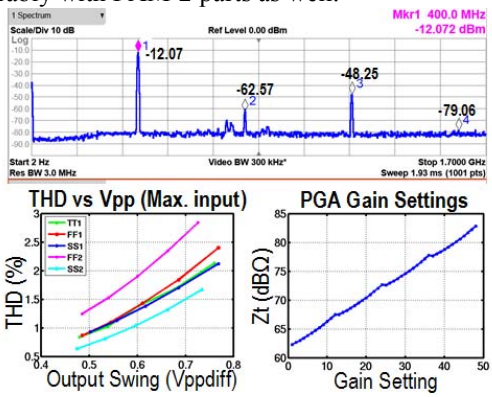

Fig. 8: Measured large signal parameters of the TIA

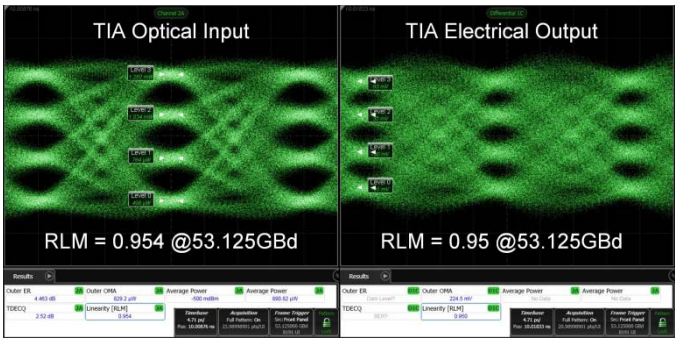

Fig. 9: Eye diagram of TIA input & output @ 53.125 GBd

Table II: Performance comparison with state-of- art TIAs

	[2]	[3]	[4]	[5]	This work
Technology	1µm InP	130nm SiGe	14nm FinFET	130nm SiGe	16nm FinFET
Supply Voltage (V)	5	3.3	1	3.3	1.8
Serial data rate (Gb/s)	100	64	64	25	100
Modulation	QPSK	QPSK	PAM-2	PAM-2	PAM-4
Bandwidth (GHz)	45	53	14.2	23	27
Transimpedance (dBΩ)	70	80	77	76.5	78
Input ref. noise (pA/√Hz)	N/A	24.86	N/A	15.82[1]	18.3
Power dissipation (mW)	1300	277	25.1	67.5	60.8[2]
Swing (mVpp diff.)	500	900	N/A	160	600[3]
THD (%)	3.16	4.13	N/A	N/A	1.8
FOM (GHz. Ω.mW)	109	1913	4005	2283	3527[4]

1 calculated from integrated noise & BW
2 for TT parts, 49.3 mW for FF & 85.9 mW for SS parts
3 equivalent swing of embedded part, 300 mV with 50 Ω termination
4 for TT parts, 4350 for FF and 2496 for SS parts

ACKNOWLEDGMENT

The authors would like to thank Vito Boccuzzi and Dr. Romesh Nandwana for assistance with painstaking measurements. We also appreciate the support of Sanjay Sunder, Matt Traverso, Cristiana Muzio and Dr. Kaushik Patel for support & helpful discussions.

REFERENCES

[1] http://www.ieee802.org/3/cd/public/July16/lewis_3cd_01a_0716.pdf

[2] D. Ferenci, et al., "A highly linear transimpedance amplifier in InP technology for applications in 100 Gbits/s fiber optical data communication," European Microwave Integrated Circuits Conference (EuMIC), pp.45-48, 2013.

[3] A. Awny, et al., "A dual 64Gbaud 10kΩ 5% THD linear differential transimpedance amplifier with automatic gain control in 0.13µm BiCMOS technology for optical fiber coherent receivers," ISSCC 2016, Digest of Technical Papers. IEEE International, pp.406-407, Feb. 2016.

[4] A. Cevrero, et al., " A 64Gb/s 1.4pJ/b NRZ Optical_Receiver Data_Path in 14nm CMOS FinFET," ISSCC 2017, Digest of Technical Papers. IEEE International, pp.482-483, Feb. 2017.

[5] G. Kalogerakis, et al.," A Quad 25Gb/s 270mW TIA in 130nm BiCMOS with <0.15dB crosstalk penalty," ISSCC 2013, Digest of Technical Papers. IEEE International, pp.116-117, Feb. 2013.