21.4 A Microfluidic-CMOS Platform with 3D Capacitive Sensor and Fully Integrated Transceiver IC for Palmtop Dielectric Spectroscopy

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Quantitative measurement of the complex relative dielectric permittivity (ε_r) of a material *vs.* frequency (i.e., dielectric spectroscopy, or DS) is a powerful monitoring technique that extracts key information on molecular characteristics of the material-under-test (MUT) via its interactions with electromagnetic waves in a broad frequency range. Despite its potential as a label-free, nondestructive, real-time and fully electrical monitoring modality for myriad applications, including structural biology, fermentation monitoring for alcoholic beverages, food safety control and clinical diagnostics, DS is still underutilized as an analytic tool in scientific research or clinical settings. This is due to the dearth of an autonomous, small-sized, low-power and portable instrument to conduct MHz-to-GHz DS measurements without requiring a microwave probe station, benchtop vector network analyzer (VNA) equipment, or large (100's of mL) sample volume.

This paper reports a self-sustained miniaturized DS platform that incorporates a microfabricated parallel-plate capacitive sensor with a 3D-gap, floating electrode and microfluidic channel for sample delivery, as well as a fully integrated transceiver IC, as conceptually shown in Fig. 21.4.1. The transceiver applies a sinusoidal RF excitation signal with MHz-to-GHz tuning capability to the sensor loaded with the MUT, and measures the amplitude/phase of this excitation signal after transmission through the sensor.

Figure 21.4.1 also shows a cross-sectional view of the DS sensor and transceiver IC architecture. Two planar sensing electrodes (0.6×0.6mm^2) are separated from a gold floating electrode (1.2×2.8mm^2) through a microfluidic channel (height of 250µm, sample volume of 9µL) to form a 3D, series-connected, parallel-plate, capacitive sensing area [1]. As the MUT passes through this area, the impedance (and hence voltage-transmission characteristics) of the sensor changes based on ε_r of the MUT. A surface coating (1.5µm Parylene-N) prevents direct contact between the MUT and metal electrodes.

The IC architecture incorporates a RX, which utilizes broadband frequency response analysis to process the sensor response signal by first down-converting it from the RF excitation frequency to an IF of 1MHz using an LNA and active mixer, followed by down-converting the IF signal to dc using a coherent detector employing a passive HPF, two IF VGAs, a passive mixer driven by phase-calibrated I/Q signals (1MHz) and an active-RC LPF [2]. The ε_r of the MUT is then extracted from the IC measurements of the sensor using a 6-point sensor calibration algorithm that runs either offline on a computer or online on low-cost embedded platforms such as the Raspberry Pi. To enable a self-sustained operation for platform portability, the IC architecture also incorporates a TX to generate the RF excitation signal for the sensor, as well as the LO signals for the RX in a frequency range of 9.75MHz to 2.432GHz.

The TX core is an integer-N frequency synthesizer operating from 1.248-to-2.432GHz, which integrates a PFD, current-programmable charge pump, loop filter, dual G_M-mode QVCO and buffer, high-frequency divide-by-2 block and programmable frequency divider with a ratio (N) from 39 to 76. The synthesizer is designed with a constant loop gain K ($\propto K_{VCO} \times I_{cp}/N$) by keeping a nearly constant VCO gain factor (K_{VCO}) and varying the charge pump current (I_{CP}) in proportion to the programmable N. This ensures stability and consistency in settling time and phase noise of the synthesizer over the entire operation frequency range.

Figure 21.4.2 shows the circuit architecture of the wideband VCO and an illustration of the TX frequency planning. The VCO employs a pseudo-exponential capacitor bank [3] with both coarse and fine tuning to feature a nearly constant K_{VCO} of ~35MHz/V and enable low phase noise and constant loop BW of ~500kHz in the PLL. Further, the VCO features a dual G_m-mode structure for switching in cross-coupled transistors, M_{m2}, to overcome a tradeoff between VCO minimum frequency limited by the startup gain of its active core and VCO maximum frequency impacted by parasitic capacitances of the active core. The 3b-programmable tail current of the VCO is also increased with the capacitor bank code to further overcome the degradation of the LC-tank Q factor at lower frequencies.

Seven band-select frequency divide-by-2 blocks are used in the TX architecture to generate lower LO frequencies (9.75MHz to 1.248GHz), in conjunction with a wideband MUX to route the differential LO signal (I/Q) to both the RX circuitry and a programmable clock buffer. The RF excitation signal for the sensor is generated by mixing the differential LO signal (after clock buffer) with an 8-phase 1MHz signal (generated by an all-digital frequency divide-by-16 block from 16MHz external reference clock) using a harmonic-rejection SSB (HR-SSB) mixer. The mixer rejects the image sideband as well as 3rd- and 5th-harmonic mixing terms by >35dBc, resulting in a nearly single-tone RF excitation signal for the DS sensor. The clock buffer corrects any amplitude/phase mismatch between I/Q LO signals, enhancing HR-SSB mixer performance. Further, the current-programmable clock buffer and HR-SSB mixer allow for tunability in RF excitation amplitude ($\pm V_{RF}$) to ensure that the sensor response signal lie within the input DR of the RX, given a target range for ε_r of the MUT and the desired RF excitation frequency.

Figure 21.4.3 shows the circuit architecture of the HR-SSB mixer, band-select MUX, clock buffer and frequency divide-by-16 block. The wideband MUX selects one of the 8 LO signal bands using common-gate switching stages for enhanced signal isolation and suppression of harmonic mixing in HR-SSB mixer. The clock buffer uses two identical stages driven by selected I/Q LO signals to generate two I/Q LO outputs with phases of 45° and 135°. Any phase error between the I/Q LO outputs in the range of ±45° is compensated via $V_{Phase\ Adj}$ by steering the tail current and altering weighting factors of the two inputs. Any amplitude error is also corrected by adjusting the 4b-programmable current of the two stages. The HR-SSB mixer incorporates three SSB sub-mixers with a common resistive load to sum the output current signal in sub-mixer #2 with that from sub-mixers #1 and #3 with relative phase shifts of ±45° and scaling of 0.707. Each SSB sub-mixer has resistive source-degeneration at both input ports to further enhance linearity.

Figure 21.4.4 shows the measured dc system output in I/Q modes at RF excitation frequencies of ~ 50MHz, 500MHz, 1.5GHz and 2.4GHz, with the sensor loaded with DI water, phosphate-buffered saline (PBS), Miller Lite beer and Guinness beer as four primarily-water-based MUTs. Since dielectric relaxation characteristics of water molecules would dominate the response at sufficiently high excitation frequencies, the MUT responses were much closer to each other at 2.4GHz (compared to 50MHz), as evident by the much smaller DR of X-Y axis. Nonetheless, the miniaturized DS platform was fully capable of differentiating among the four MUTs at all frequencies. Note also how the response from Miller Lite beer, as compared to darker Guinness beer, was always closer to that of DI water at elevated excitation frequencies.

Figure 21.4.5 depicts the frequency-dependent real and imaginary parts of ε_r for PBS at six RF excitation frequencies from 50MHz to ~2.4GHz. These data were extracted from voltage measurements of the sensor by the IC using a 6-point sensor calibration algorithm. Compared to bulk-solution reference measurements with a benchtop *Agilent* probe and VNA, dielectric readings of the platform showed an overall rms error of 1.7% (real) and 7.2% (imaginary), with the errors reducing to 0.7% and 1.5%, respectively, between 500MHz and 2.4GHz, demonstrating feasibility of conducting MHz-to-GHz DS measurements with a self-sustained fully miniaturized platform using µL-sample volumes.

Figure 21.4.6 shows the platform performance comparison *vs.* other recent work [4]-[6]. Figure 21.4.7 shows a photograph of the palmtop DS platform and a close-up view of its sensor prototype along with a die micrograph of the 3.3×3.3mm^2 IC fabricated in 0.35µm 2P/4M RF CMOS.

References:

[1] M.A. Suster, *et al.,* "An RF/Microwave Microfluidic Sensor Based on a 3D Capacitive Structure with a Floating Electrode for Miniaturized Dielectric Spectroscopy," *Proc. IEEE Sensors Conf.*, pp. 1784-1787, Nov. 2014.

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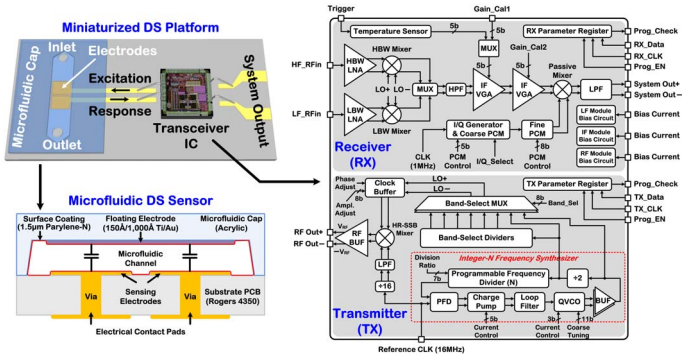

Figure 21.4.1: Conceptual illustration of a miniaturized measurement platform for dielectric spectroscopy.

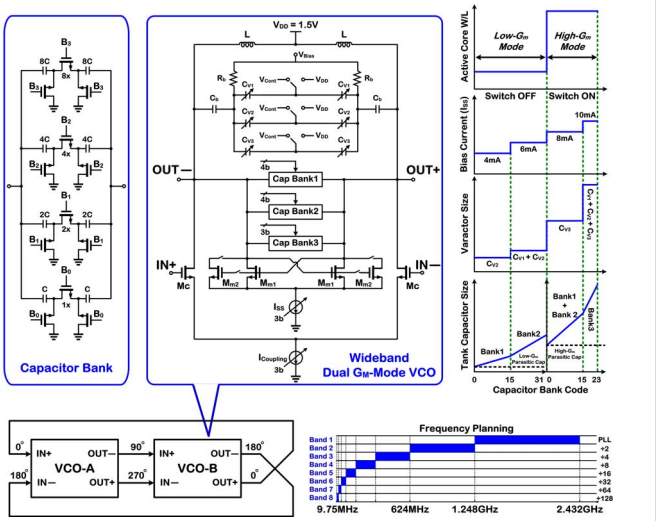

Figure 21.4.2: Circuit architecture of wideband dual G_m-mode VCO and an illustration of TX frequency planning.

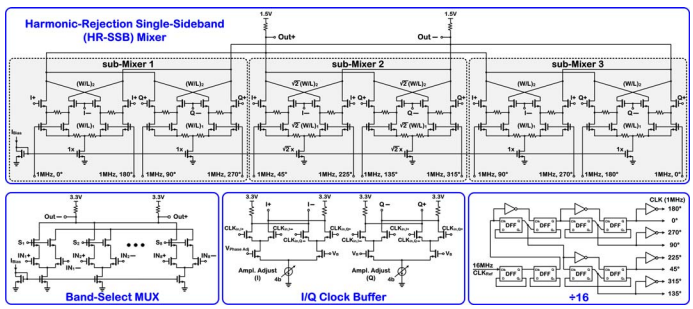

Figure 21.4.3: Circuit architecture of HR-SSB mixer, band-select multiplexer, programmable I/Q clock buffer and all-digital frequency divide-by-16 block.

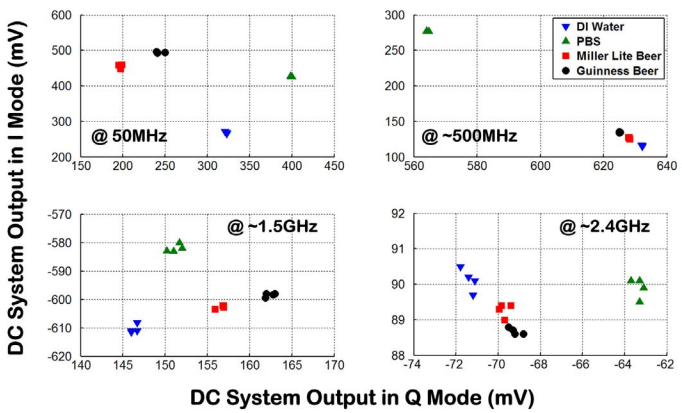

Figure 21.4.4: Measured dc system output in I/Q modes at ~50MHz, 500MHz, 1.5GHz and 2.4GHz with the sensor loaded with DI water, PBS, Miller Lite beer and Guinness beer as MUTs.

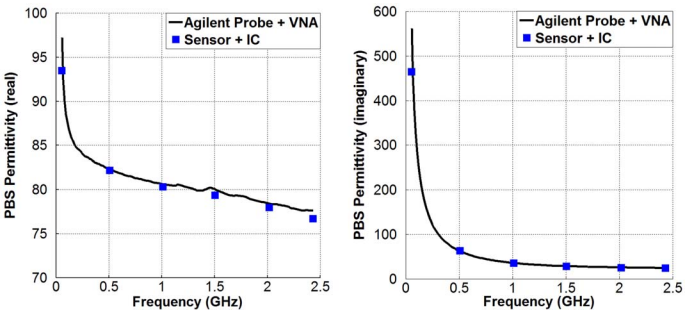

Figure 21.4.5: Measured real and imaginary parts of complex relative dielectric permittivity *vs.* frequency for PBS after excitation at 6 different frequency points from 50MHz to ~2.4GHz.

	This Work	[2] – *JSSC'14*	[4] – *IMS'14*	[5] – *JSSC'12*	[6] – *VLSI'14*
Functionality	Measurement of dielectric permittivity				Capacitive sensing for flow cytometry
Methodology	Amplitude/phase	Amplitude/phase	Amplitude/phase	Oscillation frequency shift	Oscillation frequency shift
Self-Sustainability	Yes	No (RX only)	No (external excitation)	Yes	Yes
Sensor Type	μfabricated 3D capacitor	μfabricated center-gapped μstrip line	On-chip interdigitated capacitor	On-chip interdigitated capacitor	On-chip coplanar electrodes
Operation Freq.	9MHz – 2.4GHz	10MHz – 3GHz	620MHz – 10GHz	7 – 9GHz	6.5/11/17.5/30GHz
Permittivity Type	$\varepsilon_r' \cdot \varepsilon_r''$	ε_r'	$\varepsilon_r' \cdot \varepsilon_r''$	ε_r'	ε_r'
Permittivity Range	1 – 94 (ε_r') 0 – 465 (ε_r'')	1 – 48	1 – 48 (ε_r') 0 – 20 (ε_r'')	1 – 30	1 – 60
RMS Permittivity Error	< 0.7% (ε_r') < 1.5% (ε_r'') (0.5 – 2.4GHz)	< 6.4% (0.5 – 2.5GHz)	< 1%* (0.62 – 10GHz)	< 3.5%** (7 – 9GHz)	-
Total Power Consumption	61 – 94mW	4 – 9mW (RX only)	65 – 72mW (w/o freq. synthesizer)	16.5mW	65 – 75mW (4 channels)
Die Size	3.3 × 3.3mm²	3 × 3mm²	3 × 3mm²	2.5 × 2.5mm²	-
Technology	0.35μm RF CMOS	0.35μm RF CMOS	0.18μm CMOS	90nm CMOS	65nm CMOS

*non-uniform frequency measurement points **maximum error

Figure 21.4.6: Summary of measured performance of the platform and comparison with that in prior work.

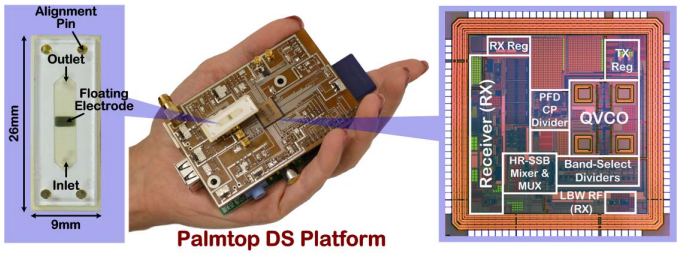

Figure 21.4.7: Photograph of the palmtop dielectric spectroscopy platform, with a Raspberry Pi module on the bottom, along with its microfabricated microfluidic sensor prototype and die micrograph of the transceiver IC fabricated in AMS 0.35µm 2P/4M RF CMOS.

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