## SESSION VII: Memory II/Memory Circuits and Systems

### THAM 7.3: A Fully-Decoded 2048-Bit Electrically-Programmable MOS-ROM

D. Frohmann-Bentchkowsky

Intel Corp.

Mountain View, Cal.

ELECTRICALLY PROGRAMMABLE semiconductor read-only memories have received considerable attention in recent years. The search for nonvolatile semiconductor storage devices stems from the inadequacy of mask programmable ROMs in meeting the demands of periodic program changes in computer microprogramming applications and in the design phase of general purpose computers. Another aspect of this search is the need for a semiconductor memory element that can provide a substitute for the nonvolatile storage capability (retention of stored information without an external power source) of magnetic memories.

The different proposed electrically programmable memories can be divided into two main categories. *(1)*—Fuzable link ROMs in which a permanent (irreversible) change in the memory interconnection pattern is affected by an electrical pulse or by mechanical scratching. *(2)*—Alterable ROMs in which a reversible change in active device characteristics is induced electrically. The fuzable type ROMs (which cannot be reprogrammed) are mainly bipolar memories with capacities up to 512 memory bits.

Most proposed alterable ROMs rely on charge storage in a dielectric which forms part of the gate of a field effect transistor. Feasibility has been demonstrated for an MNOS (metal-nitride-oxide-silicon) memory[1,2], an MAS (metal-aluminum oxide-silicon) memory[3], and a dual gate MNOS memory[4]. Due to difficulties in controlling of the storage dielectrics and lack of on-the-chip decoding, the realization of these approaches so far has been limited to *undecoded* memory arrays of up to 256 bits. Recently, the feasibility of the ovonic amorphous semiconductor memory device has been demonstrated by fabrication of an *undecoded* 256-bit memory array[5].

This paper will describe a *fully decoded* 2048-bit electrically-programmable ROM implemented with a novel MOS charge storage transistor as the basic nonvolatile memory element. The memory is organized as 256 words of 8 bits, is fully TTL compatible and can be operated in both the static or dynamic decoding and sensing mode. The memory array was fabricated successfully with silicon-gate MOS technology yielding functional devices with access times below 800 ns in the static mode and less than 500 ns in the dynamic mode of operation. The memory chip is assembled in a 24-lead dual inline package.

The novel charge storage element is a floating-gate avalanche-injection metal oxide semiconductor (FAMOS) device. A cross-section of the FAMOS structure is shown in Figure 1 with its suggested electrical symbol. It is a P-channel silicon gate MOS field effect transistor in which no electrical contact is made to the silicon gate. The gate is formed by deposition of a polysilicon[6] layer over thermal oxide (~1000Å). The floating silicon gate is isolated from the top surface by 1.0 micron of vapor deposited oxide.

The concept of an insulated-gate field-effect transistor with a floating gate as a nonvolatile memory element was first advanced by Khang and Sze[7]. Their proposed structure operates by a different physical mechanism then the present device. It involved a dual-layer metal structure with the floating gate deposited over a very thin (~50Å) layer of dielectric, to allow charge transport by tunneling from the substrate. The same concept evolved to the MNOS structure in which the floating metal gate was replaced by a layer of traps in the silicon nitride.

The operation of the FAMOS memory structure depends on charge transport to the floating gate by avalanche injection of electrons. Charge can be transferred to the floating silicon gate if an avalanche injection condition is reached in either the source or drain junction. Nicollian, et al.,[8] have shown that relatively high-current densities can be achieved in MOS capacitors by avalanche injection of electrons from a P-type silicon substrate. Dill, et al.,[4] described the use of avalanche electron injection to achieve a memory function in an N-channel dual-gate MNOS field-effect transistor. In a P-channel FAMOS transistor with a 1000Å thick oxide, an applied junction voltage of -30 V is required for the onset of avalanche injection. The gate charging current is of the order of $10^{-7}$ A/cm$^2$. Since the silicon gate is floating, the avalanche injected current results in the accumulation of a negative electron charge on the gate. For P-channel FAMOS transistor this negative charge will induce a conductive inversion layer connecting SOURCE and drain. The amount of charge transferred to the floating gate is a function of the amplitude and duration of the applied junction voltage. Once the applied junction voltage is removed, no discharge path is available for the accumulated electrons since the gate is surrounded by silicon oxide which is a very low conductivity dielectric. A plot of charge decay at 300°C and 125°C is shown in Figure 2. The activation energy was measured to be 1.0 eV. An extrapolation of the charge decay results indicates that 70%

*(See p. 200 for Figure 4)*

---

1 Wegener, H.A., "MNOS Memories", *Digest of the Intermag Conference;* April, 1970.

2 Frohman-Bentchkowsky, D., "An Integrated Metal-Nitride-Oxide-Silicon (MNOS) Memory", *Proc. IEEE (Letters),* p. 1190-1192; June, 1969.

3 Nakanuma, S. Tsujide, T., Igarachi, R., Onoda, K., Wada, T., and Makagiri, M., "A Read-Only Memory Using MAS Transistors", *ISSCC Digest of Technical Papers,* p. 68-69; Feb., 1970.

4 Dill H.G., and Toombs, T.N., "A New MNOS Charge Storage Effect", *Solid State Electronics,* Vol. 12, p. 981-987; 1969.

5 Neale, R.G., Nelson, D.L., and Moore, G.E., "Amorphous Semiconductors (Part I)", *Electronics;* Sept., 1970.

6 Vadasz, L.L., Grove, A.S., Rowe, T.A., and Moore, G.E., *IEEE Spectrum,* (6), p. 28; 1969.

7 Khang D., and Sze, S.M., BSTJ, *(46),* p. 1288; 1969.

8 Nicollian, E.H., Goetzberger, A., and Berglund, C.N., *Applied Physics Letters, (15),* p. 174; 1969.

of the initial induced charge is retained in excess of 10 years at 125°C.

Since the gate electrode is not electrically accessible, the charge cannot be removed by an electrical pulse. However, the initial equilibrium condition (no electronic charge on the gate) can be restored by illuminating the unpackaged device with ultraviolet light or by exposure of the packaged device to X-ray radiation.

The electrically-alterable ROM chip consists of an array of 2048 FAMOS transistors organized as 256 words of 8 bits. A circuit schematic of the memory cell and the decoding transistor is shown in Figure 3. Programming of a memory bit is accomplished by coincidence selection of the $X$ and $Y$ lines which connect the selected FAMOS transistor to the voltage pulse on the $Y$ line, resulting in charge transfer to the floating gate. All other memory bits are not programmed due to either the lack of a pulse on the $Y$-select line or the lack of a transfer pulse on the $X$-select line.

In the WRITE mode, initially all 2048 bits are in the "1" state. Information is introduced by selectively writing "0's" in the proper bit locations. The WRITE signal applied to the $W$ terminal (Figure 4) is a 50-V, 1.0-ms pulse. Address selection in the WRITE mode is done by the same decoding circuitry used in the READ mode ($A_1$ - $A_8$). Writing of information into a fully decoded 256 x 8 memory required the use of the output terminals ($OUT_{1\text{-}8}$) as additional decoding inputs during the WRITE mode only. In addition, the chip was designed to allow 50-V signal lines in the WRITE mode without any critical parasitic paths due to field inversion.

The amount of charge stored in a memory cell in response to a WRITE pulse is typically 3.0 x $10^{-7}$ C/cm$^2$ which is equivalent to 10 V on the gate of a conventional MOS transistor. The long term decay rate in a memory cell at 125°C is logarithmic with a slope of 1.0 V per four decades of storage time. This compares with a faster decay rate of 1.0 V per decade for both the MNOS and MAS memories.

Over 5000 hours of storage retention data at 125°C has been accumulated. Extrapolation of charge decay measurements at 300°C and 125°C indicates storage retention times greater than 10 years at 125°C.

Memory operation in the *read-only* mode is the same as in conventional mask programmable ROMs. A selected memory cell with a charged FAMOS transistor will be reflected by a low ("0") TTL level at the output, while a memory cell which is not charged will result in a high ("1") TTL level. Both the static and dynamic modes of decoding and sensing are available in a single package through the use of parallel load transistors on the chip. Mode selection is done by activating the load transistors connected to the clock lines $\phi_1$ and $\phi_2$ (Figure 4) in the dynamic mode and those connected to $V_{GG}$ in the static mode. The static mode of operation eliminates the need for clocks at the expense of increased power dissipation and reduced speed, while the dynamic mode offers advantages in both performance categories.

As can be seen from the foregoing, electrical programming of the memory is conceptually the same as operation in the read mode with the exception of the voltage levels. Hence, the memory can easily be programmed from punched paper tape or other data input devices through an electrical programming terminal. Once programmed the memory array can be erased (restored to the all "1" state) by ultraviolet light (before packaging) or by exposure to X-ray radiation. This allows the memory chip to be completely tested and erased prior to shipment.

In summary, the combination of a novel charge storage device and circuit techniques which allow its implementation with existing processing techniques has led to the realization of the first fully-decoded 2048-bit electrically-programmable ROM. A photomicrograph of the chip with a designation of the different circuit blocks is shown in Figure 4.

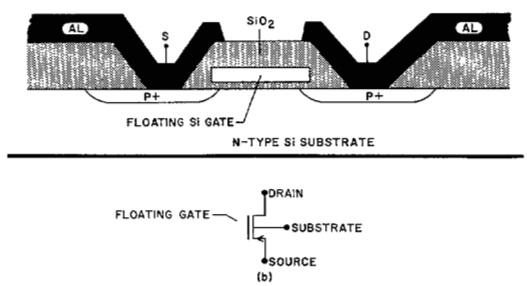


**FIGURE 1—*(a)*—Cross section of a FAMOS structure. *(b)*—Suggested electrical symbol.**

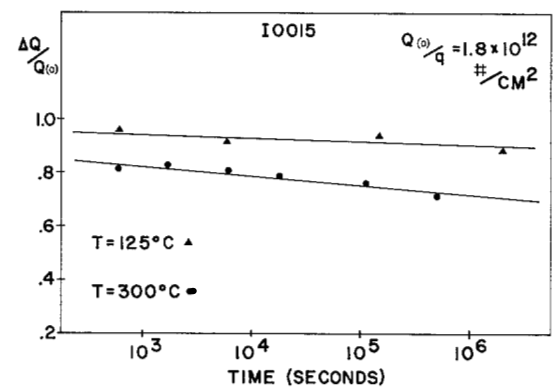


**FIGURE 2—Charge decay of a FAMOS device at 300°C and 125°C.**

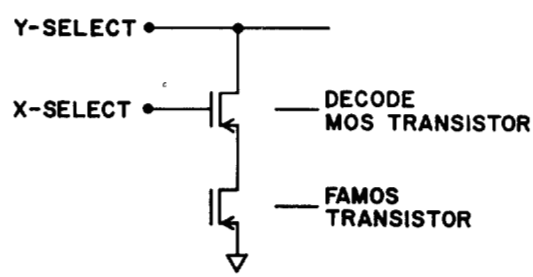


**FIGURE 3—Circuit schematic of the memory cell and decode transistor.**

## Monolithic Main Memory

(Continued from Page 76)

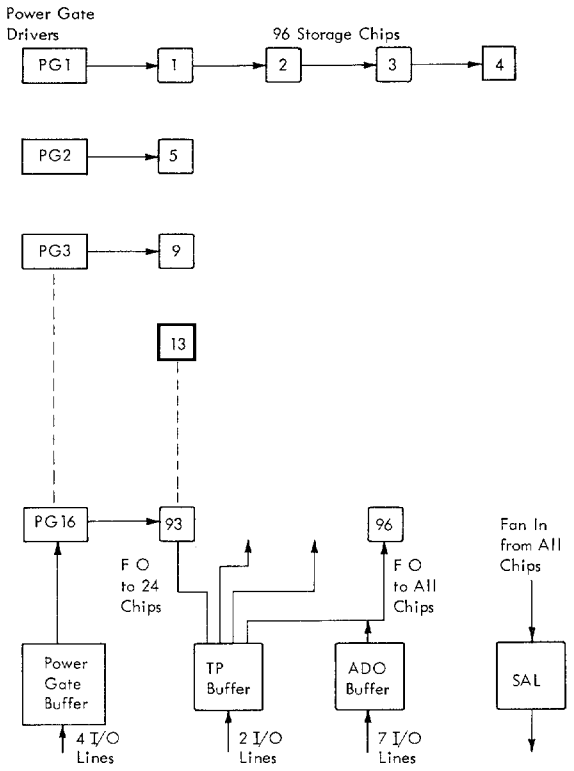


FIGURE 3-12K by 1-bit card organization.

## A Fully-Decoded 2048-Bit Electrically-Programmable MOS ROM

(Continued from Page 80)

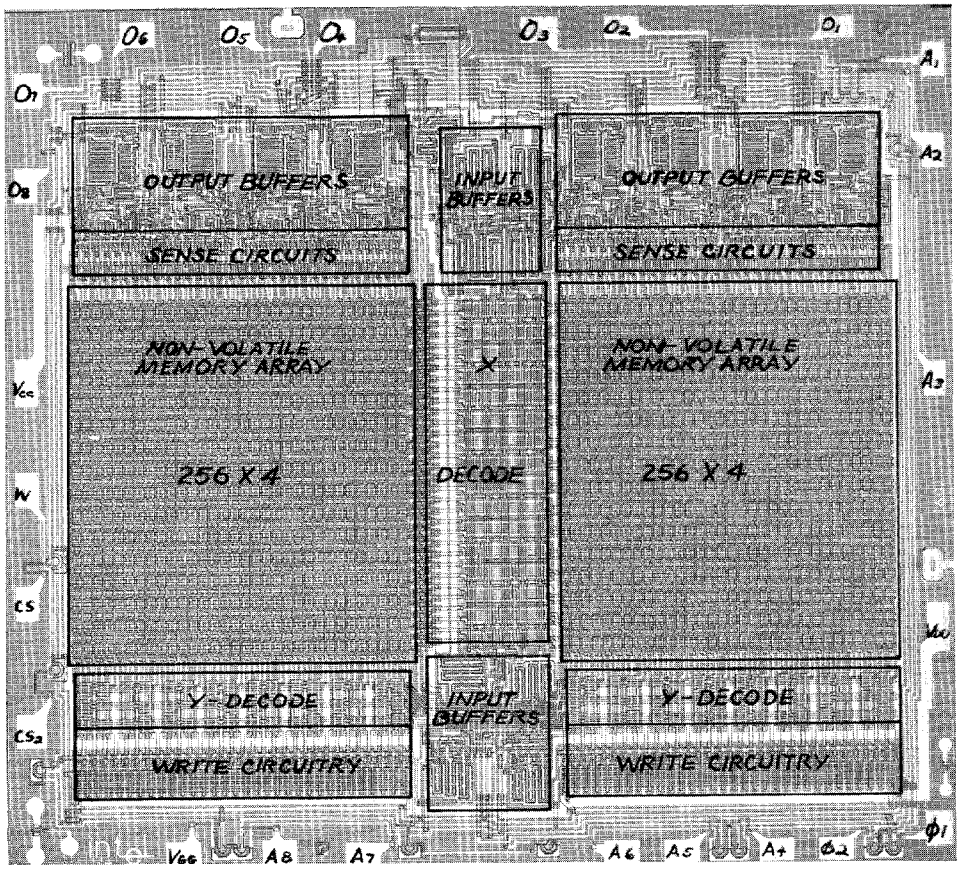


FIGURE 4—Photomicrograph of the 2048-bit memory chip.