A 26 dBm 39 GHz Power Amplifier with 26.6% PAE for 5G Applications in 28nm bulk CMOS

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***Abstract*— Continued demand for 5G cellular connectivity in mobile handheld devices, where antenna real-estate is at a premium, necessitates high output power from individual transmitter elements. While more expensive heterogeneous and SOI CMOS process based power amplifiers (PAs) provide high P_{out} at good efficiencies, deep sub-μm bulk CMOS still remains the technology of choice for cost and integration benefits. This paper presents a 5G mm-Wave PA at 39 GHz that generates a saturated P_{out} of 26 dBm with a peak power-added efficiency (PAE) of 26.6% and a saturated power gain of 28.6 dB. The output stage utilizes compact layout & triple-well transistors to enable efficient yet reliable device stacking and a compact, 4-way, low-loss, series-parallel power combiner further enhances P_{out}. High average power measurements have been demonstrated during single-carrier as well as 5G NR OFDM modulations at competitive efficiencies. Long term reliability measurements using aging acceleration techniques demonstrate the robustness of the implemented PA. This PA achieves one of the highest ITRS figure-of-merit among reported 5G mm-Wave works in CMOS and also the highest output power among deep sub-μm (<90nm) 5G bulk CMOS PAs.**

***Keywords*— 5G, CMOS power amplifier, millimeter-wave.**

I. Introduction

The widespread demand for gigabit per second cellular connectivity for content-rich handheld applications has driven the development and recent standardization of the 5G New Radio (NR) specifications in the mm-Wave bands world-wide from 24 to 43 GHz [1]. As a result, there has been a surge of interest in 5G chipsets for base-station applications where the form factor allows for multi-element, large-aperture phased arrays to be realistically implemented. The peak output power (P_{max}) requirement of the individual transmitter (TX) elements for such applications is moderate (i.e. $5-15$ dBm [2]) and the desired link range is achieved through array gain.

However, in a hand-held form-factor with limited usable dimensions, only a small number of elements can be physically integrated [2], thus dramatically increasing the requirement on P_{max}. For an illustrative $\sim$100 m link (for better coverage than the 30 m estimate in [2]) with moderate multipath shadowing, even an asymmetric uplink-based phased-array (e.g. $4-8$ element TX, $64-128$ element RX) transmitting a high-order constellation (e.g. 64 QAM – 256 QAM) over $\sim$ 500 MHz bandwidth would require per-element TX P_{max} of >23 dBm at 39 GHz. Generating such high P_{max} at mm-Wave frequencies in handheld devices necessitates high efficiency power amplifiers (PAs).

Recent works in SOI CMOS and III-V processes have demonstrated high P_{max} at reasonable efficiency [3], [4]. However, the high-cost and low-yield of some of these technologies make low-cost bulk CMOS a desirable process technology choice for the mobile 5G market. Additionally, integrating the TX in the same CMOS process node as the 5G modem/transceiver can present integration benefits in volume manufacturing and costs. However, bulk CMOS integration of high-power PAs brings about a set of challenges mainly due to swing limitations and long-term reliability issues affecting P_{max}.

This paper addresses these challenges through the use of (a) triple-well device stacking in bulk CMOS to reliably achieve high swings and (b) compact on-chip distributed active transformer (DAT) to achieve low-loss 4-way power combining. By using these techniques, a 3-stage, 39 GHz PA for 5G user equipment (UE) applications is implemented in 28 nm bulk CMOS, with a saturated output power (P_{sat}) of 26 dBm while maintaining a peak PAE of 26.6%. The PA delivers up to 23.5/21.5/19.5 dBm average P_{out} for SC-QPSK/16QAM/64QAM modulations respectively and is also shown to be compatible with the newly developed 5G-NR 64 QAM OFDM Uplink signals at an average P_{out} of 14.7 dBm. Long-term reliability of the PA is also demonstrated through voltage and temperature stress tests over multiple samples for continuous operation at saturated output power (P_{sat}) and OFDM measurements.

II. Power Amplifier Design

A. Stacking in bulk CMOS

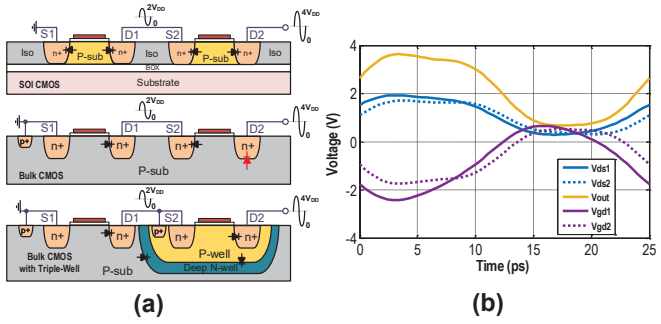

Fig. 1. (a) Cross-sections of a 2-stack cell showing critical breakdown junctions (red diodes) for SOI-CMOS, bulk CMOS, & bulk CMOS with triple-well transistors. (b) Simulated voltage swings at critical nodes.

Device stacking [5] in deep sub-μm SOI CMOS is a well-established technique to alleviate breakdown voltage limits by dividing the voltage swing across several transistors,

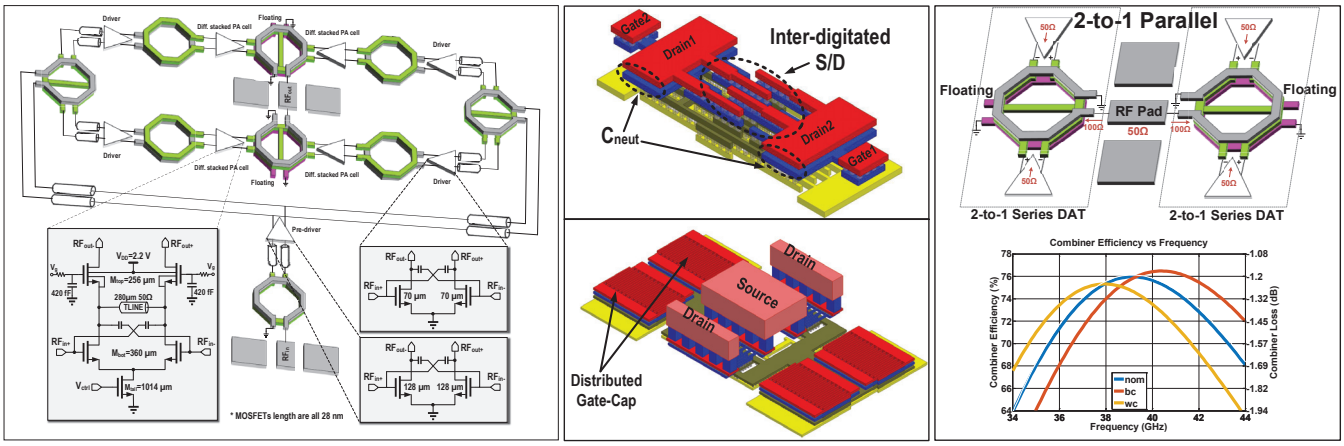

Fig. 2. (a) Block diagram of the 3-stage 39 GHz power amplifier showing schematics of the stacked output stage and common-source driver stages. (b) 3D view of the PA unit cell for the common-source device for M_{bot} and 3D view of two parallel stacked transistors with their corresponding gate capacitances as the unit cell for M_{top}. (c) 3D layout view of 4-to-1 series-parallel combiner showing output pad arrangement to minimize parasitic losses and simulated combiner efficiency over BEOL corners.

thus improving reliability. Furthermore, SOI CMOS PAs do not face explicit drain-bulk breakdown issues while sustaining higher swings at the output node, and therefore benefit dramatically from stacking (Fig. 1(a)). While stacking can be implemented in bulk CMOS, drain-bulk reverse breakdown generally restricts usable supply voltages and therefore limits swing and power enhancement (red diode in Fig. 1(a)).

To mitigate these concerns, this work utilizes triple-well transistors in a bulk CMOS process where the top stacked transistor is a triple-well device with its p-well tied to its source. Since the source on the stacked device swings in phase with its drain, shorting the source to its p-well relieves the breakdown stress on the drain-bulk diode. As an added benefit, the topology also eliminates source-bulk capacitance. Fig. 1(b) shows the simulated single-ended voltage swings across the critical drain-source and gate-drain junctions demonstrating proper stack operation.

Fig. 2(a) shows the architecture and schematics of the 3-stage PA with neutralized differential driver and pre-driver stages and a 2-stack neutralized differential output stage. Four such output stages are power combined using a 4-to-1 series-parallel DAT based low-loss combiner.

B. Power Cell Design

A compact, low-parasitic yet reliability-compliant PA transistor layout is key to maxime the efficiency of the output stage. In order to reduce source-drain parasitic capacitances, the bottom transistor differential pair is implemented using an inter-digitated layout with a shared source connection. The layout also utilizes inherent opposite-sided gate-to-drain metal overlap parasitic for gate-drain neutralization, thus improving gain and stability (Fig. 2(b)). The top transistor ($\mathrm{M_{top}}$ in Fig. 2(a)) is a triple-well transistor which is layed out in a distributed fashion with interleaved gate capacitors to minimize parasitic inductances (Fig. 2(b)). Inter-stage impedance matching between the top and bottom transistors is achieved through a differential T-line. Compared to a single-ended T-line [3], a differential T-line eliminates lossy decoupling capacitors used in single-ended designs, thus improving efficiency. A single output stage with a lossless output matching network achieves a simulated P_{sat} of $21.5\,\mathrm{dBm}$ with drain-efficiency of $43\,\%$ from a $2.2\,\mathrm{V}$ supply.

C. Low-loss DAT-based power combining

Enhancing P_{sat} to higher than achievable by pure device stacking requires on-chip power combining. Amongst power combining topologies, DAT-based combiners are well established as low-loss and small form-factor combiners of differential PA stages [6]. However, since most antenna drives are single-ended, differential to-single-ended conversion in a DAT often creates severe impedance-imbalance, thus leading to significant degradation in efficiency. The imbalance is inherently created due to the asymmetry in inter-winding capacitance on the secondary coil. To mitigate this problem, the implemented DAT balances the inter-winding capacitance by utilizing an opposite floating dummy winding underneath the primary to equalize electrical coupling [7].

To further increase P_{out}, two parallel 2-to-1 series-combined DATs are arranged on two sides of the RF output pad thus forming a 4-to-1 series-parallel combiner (Fig. 2(c)). This transforms the $50\,\Omega$ load to a $50\,\Omega$ optimum impedance required by each PA. The opposite-sided arrangement also eliminates extra leads to the RF pad as in [6]. The designed 4-to-1 combiner achieves a simulated loss as low as $1.2\,\mathrm{dB}$ in the nominal BEOL corner (Fig. 2(c)).

In simulation, the 3-stage PA achieves a P_{sat} of $26.4\,\mathrm{dBm}$ with an overall drain-efficiency of 27.8%, including the driver stages. Simulations were also performed to verify the PA performance over VSWR events caused by antenna mismatches. The PA maintains a P_{sat}>$24\,\mathrm{dBm}$ over a

3:1 VSWR (Fig. 3). The corresponding simulated drain efficiencies and peak gate-drain voltages are also shown in Fig. 3.

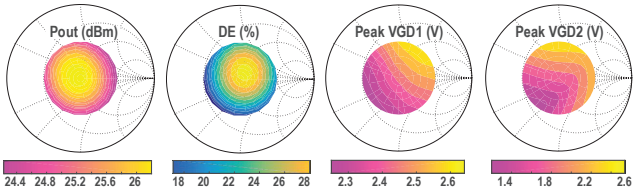

Fig. 3. Simulated performance of the PA against 3:1 VSWR mismatch.

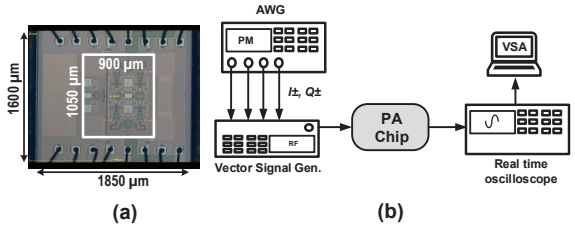

Fig. 4. (a) Die micrograph. (b) Setup for modulated measurements.

III. Measurement Results

The 5G mmWave PA test-chip was fabricated in a standard 28 nm bulk CMOS process and occupies an active area of 0.95 mm^2 including RF pads (Fig. 4(a)). DC supplies and biases are wire-bonded to a standard FR4 PCB while the GSG input and output signals are probed.

A. Static Performance

The measured small-signal gain is 38 dB centered at 38 GHz with an S_{11} <−10 dB bandwidth of 37 - 42.3 GHz (Fig. 5(a)). The peaking in small-signal gain is attributed to over-neutralization in the amplifier stages. Unconditional stability was confirmed over the entire frequency range of 10 MHz to 50 GHz (Fig. 5(b)).

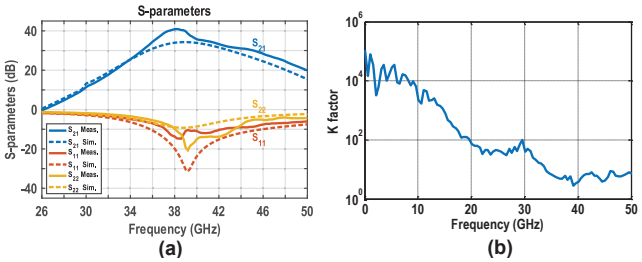

Fig. 5. (a) Measured and simulated S-paramters and (b) measured stability factor (K) showing unconditional stability over frequency.

The PA achieves a P_{sat} of 26 dBm at a peak drain and power-added-efficiency (PAE) of 26.7% and 26.6%, respectively (Fig. 6). The measured output P_{1dB} is 21.5 dBm and the 1-dB P_{sat} bandwidth is from 36.5 to 42 GHz with a >20% efficiency over the same frequency range (Fig. 6). Measurements over various supply voltages including the process nominal of 0.9 V per transistor demonstrate the flexibility of operation of the PA with a P_{sat}>24 dBm even at the lowest supply voltage (Fig. 6).

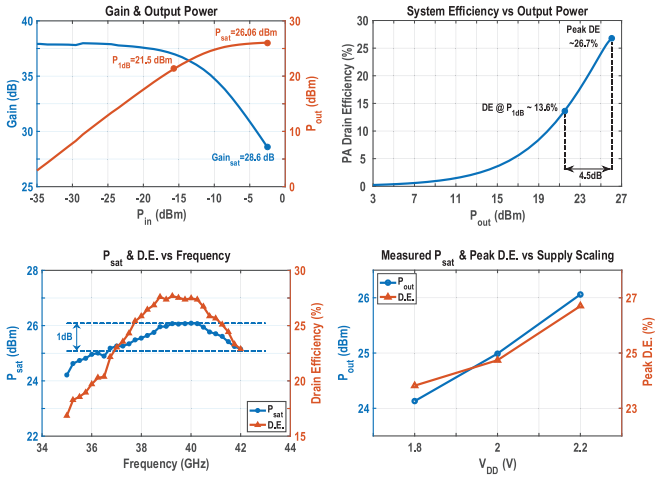

Fig. 6. Measured large signal performance.

B. Dynamic Performance

For dynamic measurements, an AWG is used to generate differential I/Q signals which are then up-converted to 39 GHz with a vector signal generator (Fig. 4(b)). The chip output is analyzed using a real-time oscilloscope and VSA software with equalization disabled. Measurements were performed to demonstrate the high average P_{out} of the PA when transmitting both single-carrier (SC) and OFDM modulated signals. A simple look-up-table based memory-less pre-distortion (DPD) was applied at high output P_{out}s for 16/64 QAM. Measured SC-QPSK/16 QAM/64 QAM modulations at average P_{out}s of 23 / 21.3 / 19.5 dBm and average efficiencies of 16.2 / 13.3 / 8.3% demonstrate the feasibility of high-power bulk CMOS PAs in mobile handheld 5G devices (Fig. 7(a)). EVM measurements at the maximum P_{out}s for the same constellations were performed across varying symbol rates (Fig. 7(b)).

Finally, the PA was measured using the recently standardized [1] FR2-5G-NR 39 GHz 50 MHz bandwidth (limited by setup) 64 QAM OFDM signal (μ=0.2). Without any DPD, an average output power of 14.7 dBm was measured with an ACPR of −33 dB (Fig. 8).

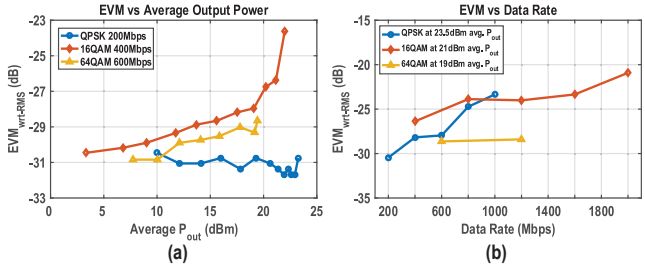

Fig. 7. (a) Measured EVM vs output power for SC-modulations. (b) Measured EVM vs data-rate for SC-modulations. RRC filtering was deployed for all SC modulation schemes with a roll-off factor of 0.35.

C. Reliability Measurements

A major concern for high P_{out} CMOS PAs is long-term reliability including transistor aging due to large voltage

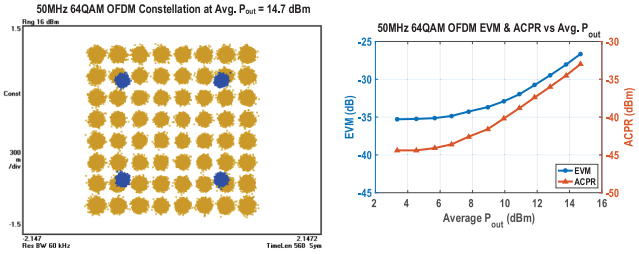

Fig. 8. Measured constellation and ACPR of the PA for a 5G NR 50 MHz 64 QAM OFDM signal.

swings. To test these concerns, the PA was operated continuously for over 22 hours at peak P_{out} without any additional thermal relief. The measured power showed no appreciable degradation (>0.1 dB) over the entire period (Fig. 9(a)). Similar measurements at the highest average P_{out} for OFDM also verified no degradation. For long term reliability evaluation, the PA was operated continuously at peak power at an elevated V_{DD} of 2.6 V and 80°C for over 66 hours. The PA lifetime can then be estimated based on the acceleration factor as shown in equation 1, where T_{J0} & T_{JS} are the nominal and stressed junction temperatures of the chip, V_0 & V_S are the nominal and stressed supply voltages and β_1 & β_2 are constants which depend on the breakdown mechanisms. A lifetime of >8 years was predicted for the PA at a P_{out}>24.8 dBm.

$$AF = e^{\beta_1\left(\frac{1}{T_{J0}}-\frac{1}{T_{JS}}\right)}.e^{\beta_2\left(V_S-V_0\right)} \quad (1)$$

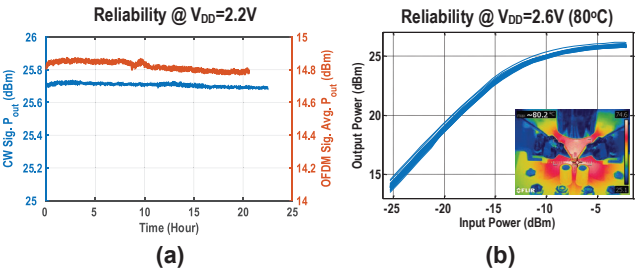

Fig. 9. (a) Measured CW and modulated performance over >20 hrs. (b) Superimposed P_{out} vs P_{in} measurements conducted every hour at V_{DD}=2.6 V and 80°C showing minimal degradation in large and small-signal performance over 66 hrs.

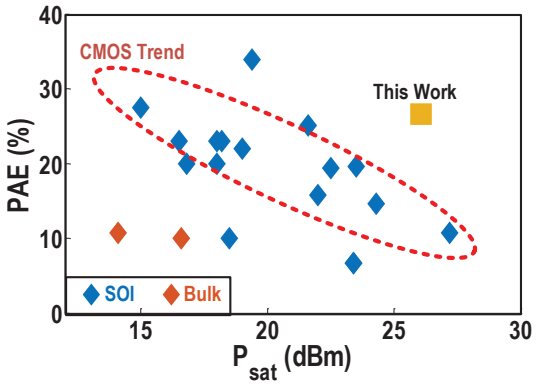

Fig. 10. State-of-art comparison against published CMOS (SOI & bulk) PAs at 35-45 GHz [11].

Table 1. Comparison with >23 dBm 5G mmWave CMOS PAs

Metric	This work	[8]	[9]	[4]	[10]
Technology	28 nm bulk	90 nm bulk	45 nm SOI	45 nm SOI	45 nm SOI
Freq. (GHz)	39	28	28	29	40
V_{DD} (V)	2.2	2.4	10.8	5.2	4.8
P_{sat} (dBm)	26	26	24.6	24.8	26.8
PAE (%)	26.6	34.1	15	26	10
OP_{1dB} (dBm)	21.5	23.2	23	21	-
1dB BW (GHz)	5.5	8	4	10	13
Gain (dB)	38	16.3	17.3	13	19.4
ITRS FoM (dB)	110	86.6	82.6	80.9	88.3
Modulations	SC-QPSK 16/64QAM OFDM	256QAM	-	-	-
Reliability Measurements	Yes	No	No	Yes	Yes

ITRS FoM=$\mathrm{Gain(dB)+P_{sat}(dBm)+20log_{10}(Freq.(GHz))+10log_{10}(PAE(\%))}$

IV. Conclusion

Compared to state of art high-power 5G mm-Wave PAs (Table 1), this work achieves the highest ITRS FoM with high unconditionally stable gain (30 dB), and can therefore be driven with minimal overhead. Compared to the state-of-art 90 nm CMOS PA [8] at a lower frequency and with unknown long-term reliability, this work achieves equal output power in a 28 nm CMOS process with >8 year predicted lifetime. This works achieves the highest PAE among published works in CMOS (bulk & SOI) with >20 dBm P_{out} at 35-45 GHz (Fig. 10). Compared to the state of art PA demonstrated with 5G NR OFDM signaling [2], this PA achieves similar modulation capability at 10× higher average P_{out}. Reliable mm-Wave high-power generation in a fine-grain bulk CMOS process, as presented in this work, would substantially simplify integration and lower cost in 5G handsets.

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