A Circuit Level Variability Prediction of Basic Logic Gates in Advanced Trigate CMOS Technology

E. R. Hsieh[1], C. M. Hung[1], T. Y. Wang[1], Steve S. Chung[1], R. M. Huang[2], C. T. Tsai[2], and T. R. Yew[2]
[1]*Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Taiwan*
[2]*United Microelectronics Corporation (UMC), Hsinchu, Taiwan*

Abstract- Variability has been one of the major scaling issues in advancing the CMOS technology. In this paper, a variation model from the device level to circuit level has been proposed and demonstrated on advanced trigate FinFETs. First, a simple and accurate transport model was developed to model variability at the device level. It was then implemented in Spice and the calculation of variation of basic logic gate building block was demonstrated with only *W/L* and the slopes, A_{vt}, A_{gm}, in the Pelgrom plot, as inputs. Finally, a unified simple analytic form was developed to predict the variability of various basic logic circuits regardless of the number of devices and the complexity of circuits.

1. Introduction

With the scaling of CMOS devices, the device or circuit faces various fluctuation sources of V_{th}, I_d, and noise-margin, which have been one of the major scaling issues. Among them, V_{th} and I_d are suffered mainly from random dopant fluctuation (RDF) [1] in the channel, random trap fluctuation (RTF) [2] in the gate dielectric, random telegraph noise(RTN) [3] of oxide trap, surface roughness of thin dielectric film [4], and metal grain fluctuation of metal gate [5], which have been extensively studied for over a decade. However, few studies have been focused on circuit-level variation [6] and the circuit variability in commercial tool, e.g., Spice, in not available.

In this work, a variation model from the device level to circuit level will be proposed and demonstrated on advanced trigate FinFETs. It will be constructed from the carrier transport of CMOS devices based on Virtual Source Model (VSM) [7], Fig.1, which describes carrier behavior with injection velocity, V_{inj}, being injected from the source to the drain, considering the series resistance, R_{sd}, effect. I_d can be modeled by VSM adequately. Then, the dominant variation factors of I_d will be analyzed. This leads to the development of a *variation model* which can be built-in Spice. A guideline for ***circuit level variation*** will be developed for basic logic gates such as NAND, NOR, CMOS inverter, and latch circuits.

2. Device Fabrication

The 28nm technology node of bulk trigate CMOS devices with poly-Si gate made on a pilot foundry platform, with EOT (SiON) = 20Å, various W/L sizes, were prepared. Also, bulk-planar devices on the same technology node were made for comparisons, Fig. 2.

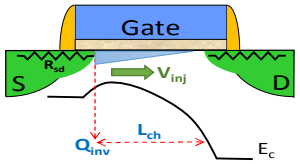

Fig. 1 The schematic to describe the carrier transport, in which V_{inj} is the velocity injecting from the peak of channel barrier, and Q_{inv} is the channel charge density at the same position.

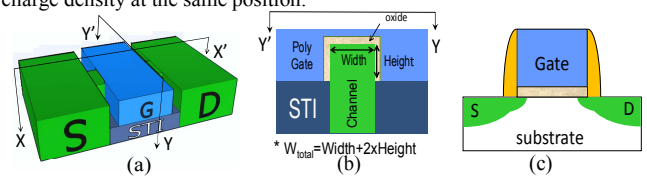

Fig. 2 The devices used in this work: (a) the trigate MOSFET, (b) the cross-section in the direction Y-Y' of (a), and (c) the planar MOSFET for comparisons.

3. Results and Discussion

A. The Device Transport Model

Figure 3 is the flow chart of a device model, improved from VSM (Virtual Source Model) [7]. I_d-V_{gs}, I_d-V_{ds}, and *C-V* are measured, and V_{th}, Q_{inv}, and R_{tot} can be extracted by following initial guesses of V_{inj} and μ, with iterations in just few loops. Finally, I_d-V_{gs} and I_d-V_{ds} are obtained from Eq. (1) in Table 1. Fig. 4 compares fitted I_d-V_{gs} results of trigate CMOS devices against the measured data, showing good matches. Fig. 5 shows the comparison between fitted I_d-V_{ds} of trigate CMOS devices and the measurement. Also, very good matches can be achieved. Fig. 6 shows the performance of trigate devices in terms of V_{inj}, which exhibits a higher V_{inj} obviously, compared to planar ones. On the improvement of the original VSM, the source-drain resistance effect, a gate bias dependent R_{sd} has been elaborated, Fig. 7, such that accurate mobility characteristics can be obtained, the blue curve in Fig. 8. This assures the accuracy of the device's level model.

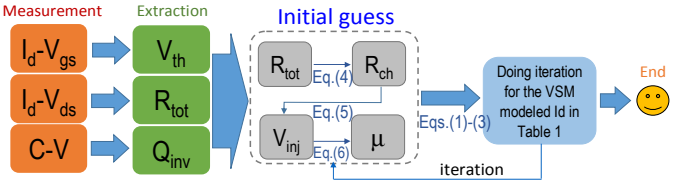

Fig. 3 The flow chart of Virtual Source Model (VSM). From the measured I_dV_{gs}, I_dV_{ds}, and C-V characteristics, V_{th}, total resistance(channel resistance-R_{ch} and source-to-drain resistance -R_{sd}), and inversion charge density can be extracted. Followed by initial guess from Eqs. (4)-(6) in Table 1, injection velocity, effective mobility, etc. parameters can be determined. Finally, the modeled I_d-V_{gs} and I_d-V_{ds} can be calculated, Eqs. (1)-(3) in Table 1.

$$I_d / W = Q_{inv} \cdot V_{inj} \cdot F_{sat} \quad \text{- Eq. (1)}$$

$$Q_{inv} = C_{inv} \cdot \frac{S.S.}{2.3} ln(1 + e^{(V_{gs}' - V_{th} + \alpha \cdot \phi_t \cdot F_t)/n \cdot \phi_t}) \quad \text{- Eq. (2)}$$

$$F_t = \frac{1}{1 + e^{(V_{gs}' - V_{th} + \alpha \cdot \phi_t / 2)/\alpha \cdot \phi_t}}; F_{sat} = \frac{V_{ds}'/V_{dsat}}{[1 + (V_{ds}'/V_{dsat})^{\beta}]^{1/\beta}} \quad \text{- Eq.(3)}$$

$$R_{tot} = \partial I_d / \partial V_{gs}; R_{sd} = R_{tot} - R_{ch} \quad \text{- Eq. (4);}$$

$$\frac{Q_{inj} \cdot V_{inj}}{V_{dsat}} = \frac{1}{W \cdot R_{ch}} \quad \text{- Eq. (5);} \qquad V_{dsat} = \frac{V_{inj} \cdot L_{ch}}{\mu} \quad \text{- Eq. (6)}$$

Table 1 The equations used in VSM. Eq. (1) models the drain current of MOSFETs, in which F_{sat} is the saturation function to determine the $V_{d,sat}$ in I_dV_{ds}; F_t is the transfer function to describe the sub-threshold characteristics.

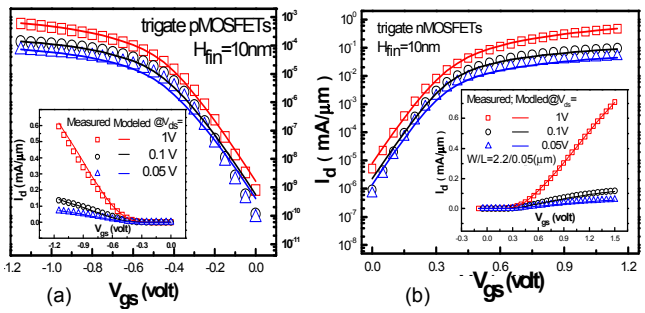

Fig. 4 Comparisons of the I_dV_{gs} curves for the measured data and Spice modeled data in trigate (a) nMOSFETs and (b) pMOSFETs, in logarithm scale and linear scale (the insert) with different V_{ds} values, which shows good matches.

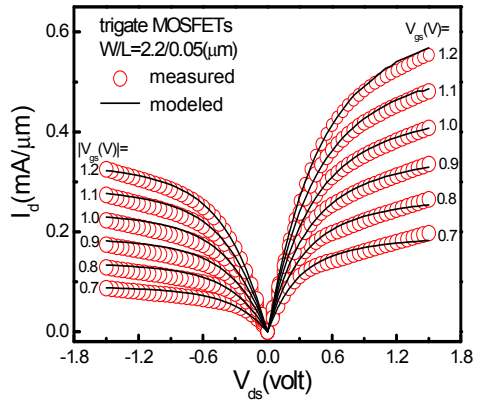

Fig. 5 Comparisons of the I_dV_{ds} curves between the measured data and Spice modeled data in trigate CMOS devices in the linear scale with different V_{gs} values, which show good matches.

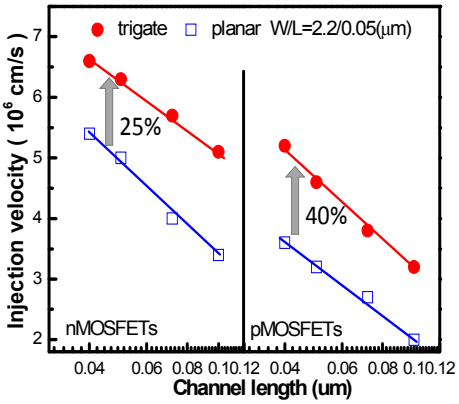

Fig. 6 The comparisons of V_{inj} between trigate and planar devices for (left) nMOSFETs and (b) pMOSFETs. It reveals that p-channel trigate devices show a much larger improvement since its sidewall has (110) orientation.

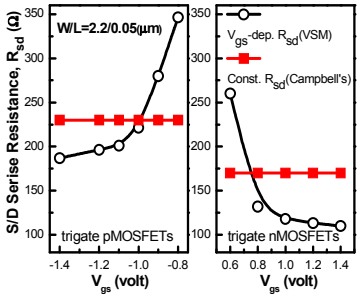

Fig. 7 Comparisons of the R_{sd} between Campbell's constant R_{sd} method and the current gate bias dependent method. The latter is more reliable for inclusion in the present VSM.

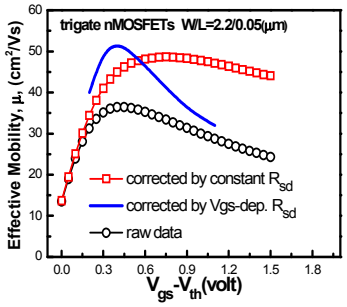

Fig. 8 Comparisons of the effective mobility extracted by split C-V and corrected by gate bias dependent R_{sd}. The blue curve in the present model is more reliable considering the R_{sd} effect.

B. The Variation Model-from Device to Circuit

To understand which parameters dominate I_d variation, Fig. 9 shows the method by decoupling I_d into V_{inj} and V_{th}. V_{th} can be further decoupled into *DIBL* and $V_{th,lin}$. From Fig. 10, σV_{inj} is closely related to $\sigma g_{m,max}$, whose scattering plot shows a strong dependency. Furthermore, multi-variant analysis (MVA) that we developed in [8] was adopted here to analyze the contribution of V_{th} and g_m variations to the I_d variation. Results in Figs. 11 and 12 show that both V_{th} and g_m variations exhibit strong dependency on I_d variation, which should be taken into account to construct the I_d variation model.

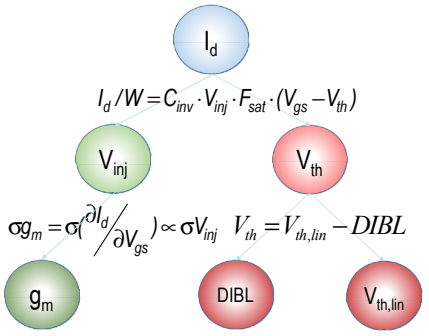

Fig. 9 The multi-variable analysis to show the variation sources of I_d equation based on VSM, in which the factors of V_{inj} and V_{th} can be extracted. The variation of V_{ing} is attributed to the g_m variation, while V_{th} variation is decoupled into DIBL and $V_{th,lin}$.

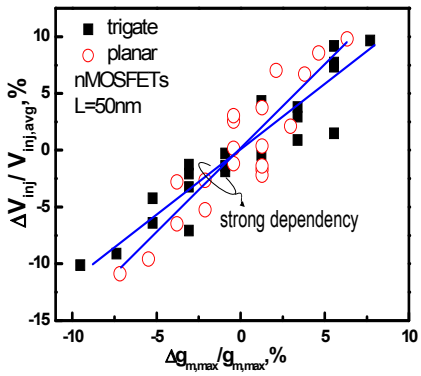

Fig. 10 The scattering plots of V_{inj} versus $g_{m,max}$ of trigate and planar nMOSFETs, showing strong dependency, i.e., the variation of V_{inj} comes from g_m variation.

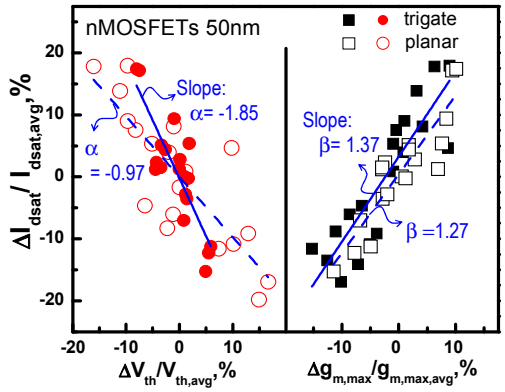

Fig. 11 I_d variation can be decoupled into the variations of V_{th} and g_m. This scattering plots show the strong dependency, and the slopes represent the strength of this dependency.

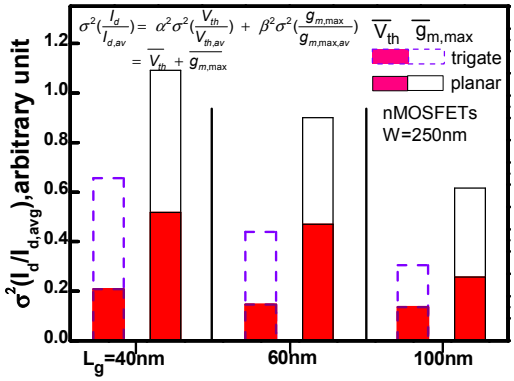

Fig. 12 By multi-variant analysis (MVA), the variance of normalized $I_d(\sigma^2 I_d)$ is expressed as the contributions from the variances of normalized V_{th} and $g_{m,max}$. Both V_{th} and $g_{m,max}$ carry about the same weight to the variation of I_d.

Furthermore, in Fig. 9, we need to examine which factor dominates V_{th} variation, $V_{th,lin}$ or *DIBL*? Fig. 13 shows that, in trigate devices, $V_{th,lin}$ is dominant, but DIBL is a secondary factor with less contribution to the V_{th} variation. So, eventually, in the framework of Fig. 9, we may simply use V_{th} and g_m Pelgrom plots [9], Figs. 14 and 15, to model I_d variation for any device sizes. In short, by providing few experimental inputs, *W/L*, A_{vt}, and A_{gm}, we will be able to develop a built-in Spice model, as described in Fig. 16. For device-level verifications, Figs. 17 and 18 show I_d-V_{gs} and I_d-V_{ds} variations. Gaussian distributions of measured statistical data and the Spice-modeled function, showing good matches. Fig. 19 is the normalized I_d variation, which verified the accuracy of the modeled data in Figs. 17 and 18 against the experiment.

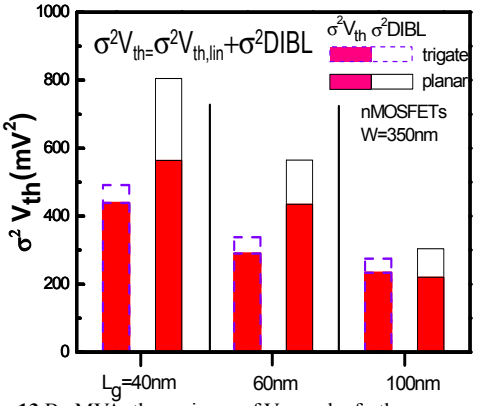

Fig. 13 By MVA, the variance of V_{th} can be further expressed as the summation of $V_{th,lin}$ and DIBL variations. Results show that $V_{th,lin}$ dominates in both trigate and planar devices.

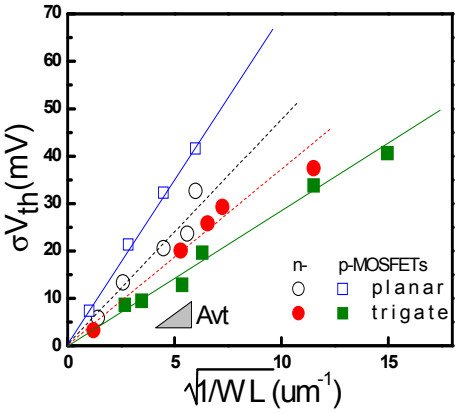

Fig. 14 In order to model I_d variation, the Pelgrom plot of V_{th} was first used to predict the V_{th} variation in terms of the device areas from the slope of the Pelgrom plot, A_{vt}.

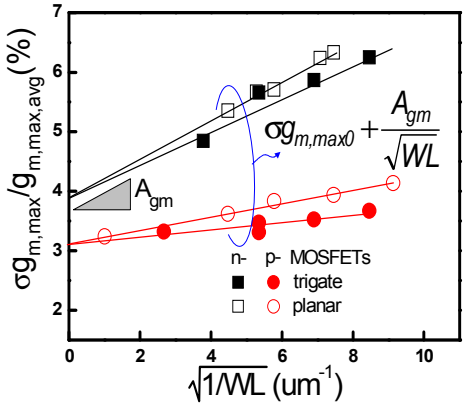

Fig. 15 Because g_m variation is closely related to the I_d variation, a Pelgrom plot on g_m is utilized to model the g_m variation of any areas from the slope, A_{gm}, and the intercept with y axis is defined as $g_{m,max0}$.

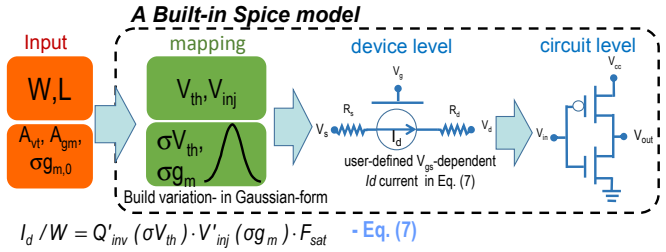

Fig. 16 The flow chart of the proposed Spice Variation Model which describes the variation of devices and circuits. Just few parameters, W, L, A_{vt}, and A_{gm}, as inputs, V_{th}, V_{inj}, σV_{th}, and σg_m can be directly calculated automatically in spice based on Table 1. Then, these variables are transformed into a user-defined element to simulate the CMOS devices at the device level. As a result, the variation of any complicated circuits can be modeled by building the block of devices, based on Eq. (7).

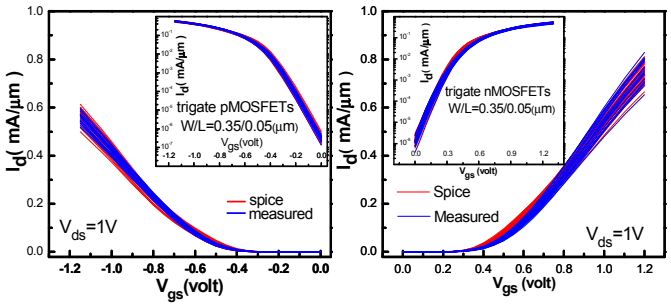

Fig. 17 Comparisons of measured and Spice modeled results of the variations of I_dV_{gs} for (a) pMOSFETs and (b) nMOSFETs in the linear scale and logarithm scales, showing good matches.

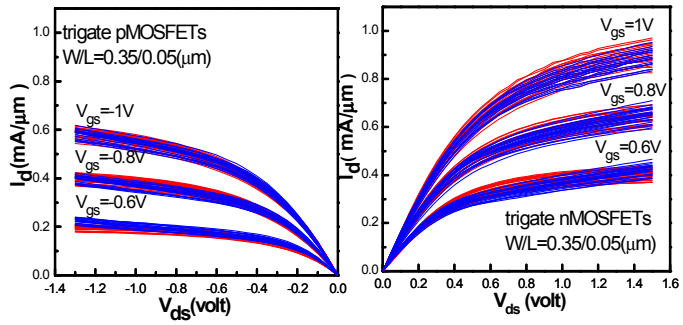

Fig. 18 Comparisons of measured and Spice modeled results of the variations of I_dV_{ds} for (a) pMOSFETs and (b) nMOSFETs, showing good matches.

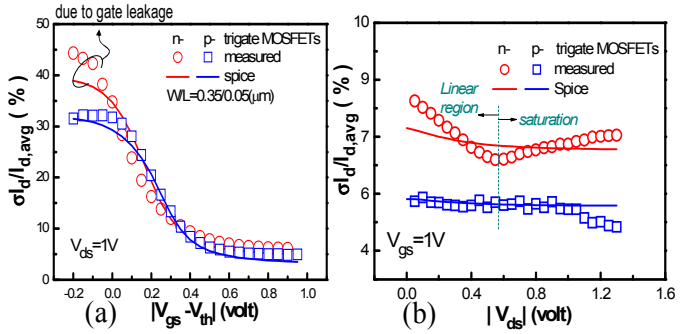

Fig. 19 The dependence of the I_d variation in various operating regions: (a) Validation of the Spice and measured I_d-V_{gs} variation data in Fig. 17. (b) Validation of the Spice and measured I_d-V_{ds} data in Fig. 18.

C. Circuit Variation- for Basic Logic Gates

For circuit level applications, three basic circuit connections are examined first, i.e., parallel, series, and two-port. Since parallel connection of devices is simply the summation of device area, which is naturally governed by the

Pelgrom plot, next, we focused on the other two connections. Fig. 20 compares series connection of two devices, whose behavior is similar to the single device. In other words, the variation of two series devices, exhibit a similar linear relationship in Pelgrom plot, Fig. 21. Again, Fig. 22 is the variation of CMOS inverters where its switching voltage, V_{sw} (Fig. 23), can be simply predicted by the A_{vt}. It was found that variation of switching voltages, such as, V_{th} or $V_{sw.}$, of circuits can be described by a typical form of the square-root of the inverse of area, Eq. (8) in Table 2.

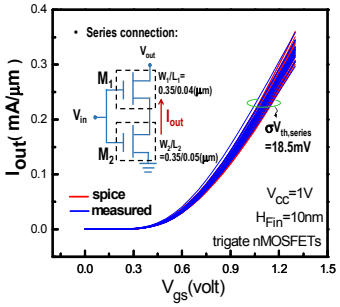

Fig. 20 The measured and Spice modeled characteristics of the variation for two series-connected trigate nMOSFETs. Both data show good matches. The insert is the schematic of this series circuit.

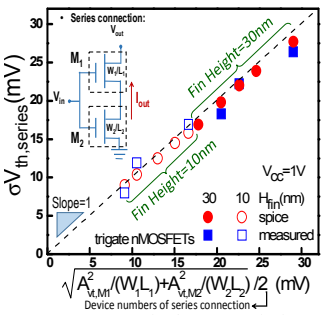

Fig. 21 $\sigma V_{th,series}$ is the V_{th} variation of the series-connected circuit, which is linearly proportional to the square-root of summation of each V_{th} variance divided by the device number, predicted by A_{vt}, i.e., this type of circuit can be directly calculated by A_{vt}.

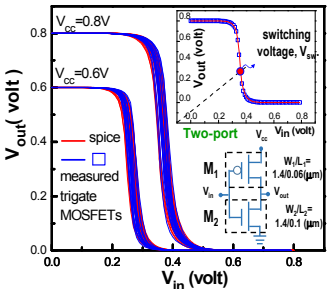

Fig. 22 CMOS inverter: This result compares the variation of inverters for spice and measured data, showing good matches. The variation parameter is defined as the switching voltage, V_{sw} (the insert).

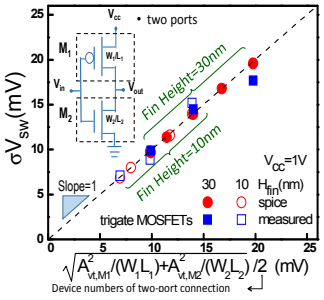

Fig. 23 CMOS inverter: σV_{sw} is linearly proportional to the square-root of the summation of each V_{th} variance divided by the device number, as predicted by A_{vt}, i.e., the variation of two-port CMOS connection can be directly predicted.

$$\sigma V_{sw} = \frac{\sqrt{\sum_{i=1}^{n}\left(\frac{A_{vt}^2}{LW}\right)_i}}{n} \quad \text{Eq.(8)}$$

Table 2 For three basic types of circuit connection, the variation of the switching voltage can be empirically described by a square-root of the inverse of area, divided by the number of connected devices.

Further, we demonstrated on two-input, NAND and NOR, CMOS circuits. Fig. 24 is the variation of the transfer curves for NAND and NOR, showing good matches between Spice and measured data. Again, Fig. 25 shows its variation of the butterfly curves that are the transfer curve of latch circuits, which serve as the storage component of 6T SRAM. *A summary was drawn* in Fig. 26 where σV_{sw} of NAND, NOR, and latch, also obey Eq. (8) in Table 2, in which V_{th} or V_{sw} variations can be easily calculated from the device size and the respective A_{vt} of Pelgrom plot. Finally, Fig. 27 is σV_{sw} of a multi-stage inverter circuit versus the device numbers. Each curve belongs to a specific technology with different A_{vt}. It reveals that σV_{sw} decreases with the increasing number of stages, especially the trigate with shorter fin-height shows the lowest variation. The above results provide us a convenient way to predict the variations of any types of logic circuits regardless of the technology and the complexity of circuits.

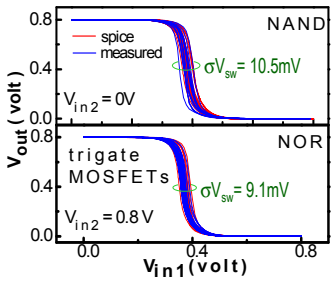

Fig. 24 The Spice and measured variation characteristics of (a) NAND and (b) NOR. The NAND and NOR circuit show almost the same variation, 10.5mV vs. 9.1mV.

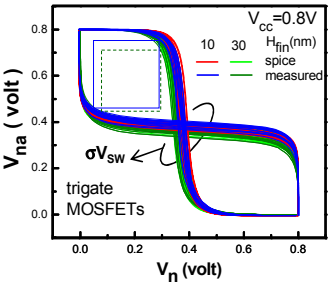

Fig. 25 Comparisons of the variation of butterfly curve between Spice and measured data with different fin heights, showing that the taller fin height induces more fluctuations.

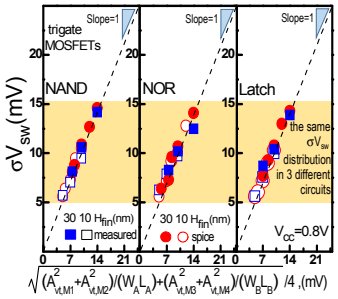

Fig. 26 The plot of σV_{sw} based on Eq. (8) for (a) NAND, (b) NOR, and (c) Latch circuits. It reveals a linear dependency in terms of the device area and Pelgrom plot coefficients for all the cases, which make it easier to estimate the circuit variations.

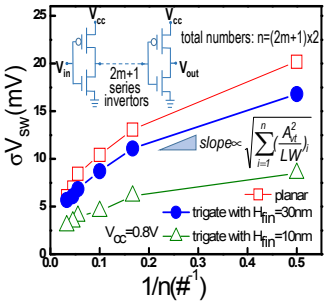

Fig. 27 The plot of σV_{sw} versus device numbers in a multi-stage CMOS inverters. The variations decrease with increasing number of stages.

In summary, *for the first time*, a *circuit level variation model* has been developed and demonstrated on an advanced trigate CMOS technology. The device model was improved from the Virtual Source Model (VSM) by including accurate R_{sd} and mobility calculations. Then, the model was implemented in Spice as a built-in model and for use in the circuit variation predictions. It was verified on several typical logic gates, NAND, NOR, inverter, latch etc. and the conclusion was reached with a ***unified form***, Eq. (8) in Table 2, which can be used to estimate the circuit variations with only few parameters, i.e., *W/L, A_{vt}, and A_{gm}*, required as inputs. This provides us a simple guideline to the variability design of more complex integrated circuits.

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References: [1] E. R. Hsieh et al., ***VLSI***, p.194 (2011). [2] H. M. Tsai et al., ***VLSI***, p. 189 (2012). [3] E. R. Hsieh et al., ***IEDM***, p. 454 (2012). [4] E. R. Hsieh et al., ***IEDM***, p. 770 (2013). [5] X. Wang et al., ***TED***, p. 2293 (2011). [6] Y. Cao et al., ***TCAD***, p. 1866 (2010). [7] A. Khakifirooz et al., ***TED***, p. 1674 (2009). [8] E. R. Hsieh et al., ***VLSI-TSA***, p. T25 (2012). [9] M. J. M. Pelgrom et al., ***IEEE J. Solid-State Circuits***, p. 1433 (1989).