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An Energy-Efficient BBPLL-based Force-Balanced Wheatstone Bridge Sensor-to-Digital Interface in 130nm CMOS

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***Abstract*—An energy-efficient time-based sensor interface in 130nm CMOS technology is presented for resistive sensors. Traditionally resistive sensors are interfaced with a voltage divider or a Wheatstone bridge to transform the sensor signal to a voltage. However, both the voltage divider and the unbalanced Wheatstone bridge are highly affected by supply voltage variations, especially in smaller CMOS technologies with low supply voltages. As alternative to ratiometric measuring, this paper presents a force-balanced Wheatstone bridge interface circuit with a highly digital architecture, that offers the advantage of low power consumption with highly improved overall PSRR. It has a noise-frequency-independent PSRR of 52dB for in-band supply noise and supply noise amplitudes up to +10dB$_{FS}$, which is an improvement of 46dB over the voltage divider and of 26dB over the unbalanced Wheatstone bridge. Apart from the sensor calibration, no other calibration or absolute precise clock or voltage references are needed due to the BBPLL-based architecture. The complete interface consumes only 124.5μW from a 1V supply with 10kHz input bandwidth and 10.4 bit resolution and 8.9 bit linearity, resulting in a state-of-the-art sensor Figure of Merit of 13.03 pJ/conversion.**

I. Introduction

Sensors become increasingly important in today's society. A growing range of application domains, such as Wireless Sensor Networks, Cyber-Physical Systems, the Internet Of Things, Smart Sensors, home automation, automotive, etc. make sensors ubiquitous. Since more and more applications are based on wireless sensing, power and energy consumption is a major concern. Although capacitive sensors are widely preferred as sensing elements for low-power applications, resistive sensors such as piezoresistive elements, thermistors, strain gauges, etc. still occupy a large share of the sensor market. The focus of this paper is on an energy-efficient readout circuit for all applications with resistive sensing elements with maximally two variable elements, such as for instance an ultra-miniaturized MEMS pressure sensor for medical applications [1].

Traditionally resistive sensors can be interfaced with a voltage divider or a Wheatstone bridge in combination with an A/D converter (see Fig. 1). A major disadvantage of a voltage divider is the low Power Supply Rejection (Ratio) (PSR(R)), since the output is directly proportional to the supply voltage (see Fig. 2). Therefore, a Wheatstone bridge is generally preferred to interface resistive sensors. However, although supply noise in principle is fully rejected in an ideally balanced Wheatstone bridge, due to mismatch in the bridge resistors or a ΔR change due to the measurand, the unbalanced bridge does suffer from supply noise in practice, resulting in a finite PSR. This can be solved by applying the ratiometric measurement method in which both the bridge's output voltage and the excitation voltage V_{DD} are measured [2]. However, the dynamic range of the bridge's output voltage and the excitation voltage can differ by a factor 10 or more, which needs the introduction of voltage dividers or amplifiers. This introduces extra complexity and extra power consumption and the accuracy is limited by resistor matching [2].

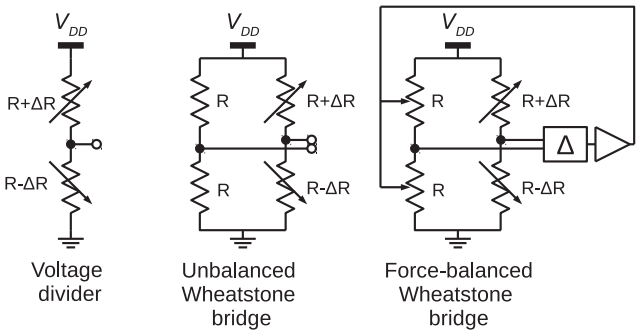

Fig. 1. Traditional techniques to interface resistive sensors: (a) Voltage divider and (b) Wheatstone bridge. (c) is the proposed force-balanced Wheatstone bridge to improve the overall PSR.

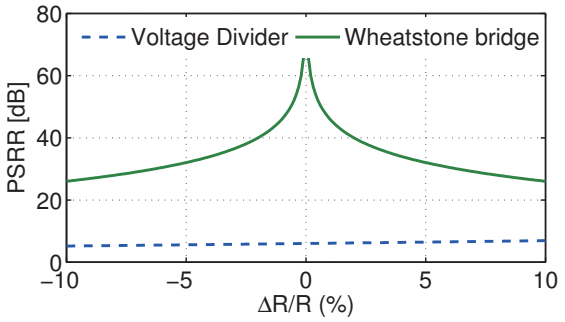

Fig. 2. PSRR as a function of the sensor resistance deviation due to a change in measurand magnitude for the voltage divider and the Wheatstone bridge with ideal A/D converter of Fig. 1.

This paper presents an alternative readout approach in which no (external) reference voltages or amplifiers are needed to achieve a high PSRR in combination with low power. The technique actuates one half of the Wheatstone bridge so that the bridge is always balanced [3]. By this force-balancing of the bridge with a digital loop, a high PSRR is always maintained and the sensor-to-digital conversion is done inherently. The sensor interface is based on a highly-digital Bang-Bang Phase-Locked Loop (BBPLL). Highly digital time-based interfaces can take advantage of smaller CMOS technologies that have increased timing resolution, and are more resilient to lower supply voltages and noise. This enables to design a low-voltage energy-efficient, supply-noise-resilient sensor interface. By employing the phase-locked loop structure, no other absolute precise voltage or clock references are needed, which saves power and is a major advantage.

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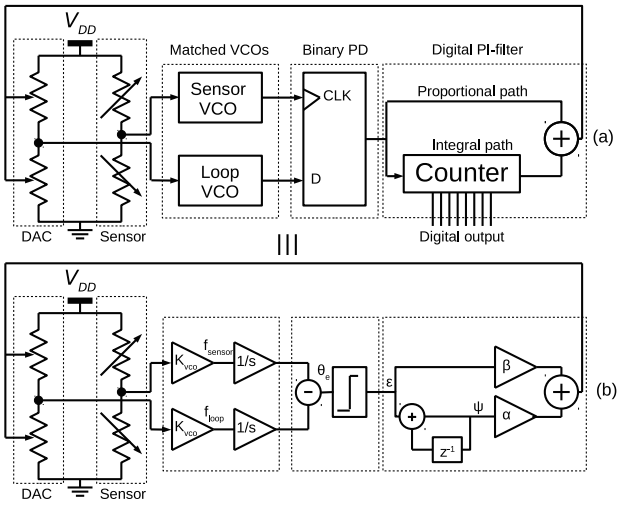

Fig. 3. Time-based architecture of the force-balanced Wheatstone bridge, BBPLL-based sensor interface (a) and equivalent block diagram (b)

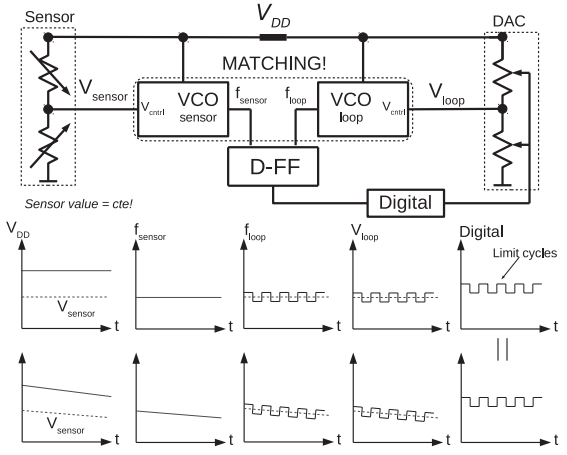

Fig. 4. Illustrating the influence of a varying supply voltage on the internal signals and the digital output.

The paper is organized as follows. In section II-A, an overview of the design approach and interface architecture is given. Next, section III discusses some of the implemented building blocks. The circuit has been prototyped in UMC130 CMOS technology. Finally, in section IV, the measurement results are discussed and compared to other state-of-the-art resistive sensor interfaces. Section V concludes this paper.

II. System-level overview

A. Resistive sensor readout approach

Supply-voltage non-idealities such as supply noise, digital switching noise, EMI, etc. have always been very important when dealing with sensors and sensor readout circuits. With the downscaling of CMOS technologies, these non-idealities become even more important due to the decreased voltage headroom. The PSR(R) is thus a very important parameter for such systems. Fig. 2 shows that the PSRR is infinite for a perfectly balanced Wheatstone bridge. Therefore, in this paper a force-feedback mechanism is employed to force the Wheatstone bridge to its balanced position, achieving high PSRR at all times. This is done by measuring the voltage difference between the two branches and actuating one branch of the Wheatstone bridge via a feedback loop to balance the bridge. Due to this feedback mechanism, the sensor-to-digital conversion is done inherently. Instead of comparing both voltages in the amplitude domain, in our design (see Fig. 3) these voltages are first converted to the time/frequency domain by a Voltage-Controlled Oscillator (VCO), whereafter they are compared and processed in the digital domain. This enables the interface to be time-based and highly digital. The complete mechanism to compare the two frequencies and to control the feedback loop is based on a Bang-Bang Phase-Locked Loop (BBPLL), which is explained in the next subsection.

B. Interface architecture

Fig. 3 (a) shows the schematic diagram of the implemented interface architecture which is based on a second-order BBPLL [4]. The conversion is based on the locking of two identical VCOs: one controlled by the right Wheatstone branch which contains the sensor, and one controlled by the left branch which is implemented as a resistive D/A converter. Due to the BBPLL dynamics, both oscillators will run at the same frequency if the PLL is locked. Since both VCOs are implemented identically, the loop will make their control voltages (almost) identical, thus making the differential voltage of the Wheatstone bridge almost zero. As a result, the Wheatstone bridge is balanced and the digital code is proportional to the sensor value, which means that the sensor value is digitized. Because both frequency signals of the VCOs are compared relatively to each other by a phase difference detector, no absolute clock reference is needed to do the time/frequency-to-digital conversion. A simple D-FlipFlop quantizes the phase difference of the VCOs with 1 bit. The digital filter in the loop consists of a proportional and an integral path and the latter is implemented with an 8-bit digital counter (see Fig. 3 (a)).

To understand the working principle of the converter, an equivalent block diagram of the architecture is depicted in Fig. 3 (b). The input frequency f_{sensor} represents the sensor signal of the right Wheatstone branch and is equal to

$$f_{sensor} = f_{nom} + K_{vco} \cdot V_{sensor} \tag{1}$$

with f_{nom} the free-running frequency and K_{vco} the gain factor of the VCO. The frequency of the VCO in the loop equals

$$f_{loop} = f_{nom} + K_{vco} \cdot (\epsilon \cdot \beta \ + \alpha \cdot \psi) \tag{2}$$

with $\epsilon = sign[\theta_e]$, with θ_e being the phase error between the two VCOs, ψ is the accumulation of ϵ in time and α and β are the gain factors of the proportional and integral path respectively. One can derive that when both VCOs are running at the same frequency (in lock):

$$V_{sensor} = mean(\epsilon \cdot \beta + \alpha \cdot \psi) \tag{3}$$

Averaging (mean) is necessary since the output exhibits deterministic limit cycles due to the quantized system, which are proportional to the input signal [4]. Due to the loop dynamics, $mean(\beta) = 0$ [4], hence resulting in:

$$V_{sensor} = mean(\alpha \cdot \psi) \tag{4}$$

This means that the integral path (digital counter) tracks the input signal, while the proportional path ensures stability. The digital output of the counter is thus the digitized version of the analog sensor signal. Like a $\Sigma\Delta$-modulator, the loop can go in slope overload [4], limiting the input frequency, which is determined to be 10 kHz in this design, which is sufficient for most sensor applications. In addition, since the free-running frequency of the VCO is much higher (∼8 MHz), the oversampling nature of the structure is exploited by digitally filtering

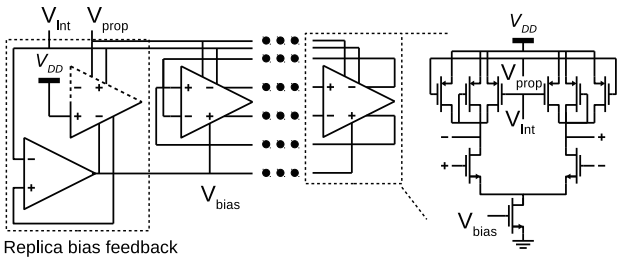

Fig. 5. 4-stage differential VCO with replica bias feedback. The differential cell is shown on the right.

the frequencies above 10 kHz. In this way bandwidth is exchanged for improved resolution beyond the number of counter bits.

C. Power Supply Rejection

In this sensor interface the force-feedback mechanism makes that the Wheatstone bridge is always balanced, hence the name force-balanced Wheatstone bridge. This means that common-mode supply voltage variations are in an ideal sense completely rejected at the differential output of the Wheatstone bridge. Since the BBPLL will only react to a difference in frequency between the VCOs (which equals the differential signal), the BBPLL will not react to common-mode supply voltage variations, even if the frequencies of the VCOs change in absolute magnitude. Of course, this is only true if both VCOs react identically to the supply voltage variations, hence good matching is required, which requires attention during design and layout. Fig. 4 illustrates the internal signals of the interface as a function of the supply voltage. Both situations output the same digital value at all times.

III. Implementation in CMOS

A. Voltage-Controlled Oscillator

A differential ring oscillator with replica bias feedback to bias the delay cells is implemented for both the VCOs (Fig. 5) [5]. The replica bias network dynamically biases the current sources and forces the single-ended output swing between V_{DD} and V_{Int}, resulting in a linear tuning characteristic [5]. It has been shown that the load elements of the differential cell lead to a high dynamic supply-noise rejection and the dynamically biased current sources provide high static substrate-noise rejection [5]. In Fig. 3 the proportional and integral path of the digital filter are added before the D/A conversion. In the implemented design, these two paths are added in the loop VCO by providing two almost equivalent inputs (V_{Int} and V_{prop}) to control the VCO frequency. This means that also two D/A converters need to be implemented in the feedback path. For the sensor VCO, V_{Int} is the sensor input while V_{prop} is connected to $V_{DD}/2$. One VCO consumes 31.24 μW maximally.

B. Subranging R-2R D/A converter in the integral path

Since the integral and proportional path are added in the loop VCO, two separate D/A converters are implemented. The proportional path has only two states (1 or 0), so this can easily be implemented with a resistive ladder. The integral path however contains an 8-bit digital word and needs to cover the same range as the sensor input range, which in our example is 10 % of V_{DD}. A simple resistive ladder would be very hard to implement, due to the matching constraints to achieve the high accuracy and the small output swing. Therefore a subranging R-2R D/A converter in voltage mode is implemented to fulfill the requirements (Fig. 6) [6]. The output range is solely defined by the ratio of the resistances R_x and R_y [6]. Therefore, we can avoid

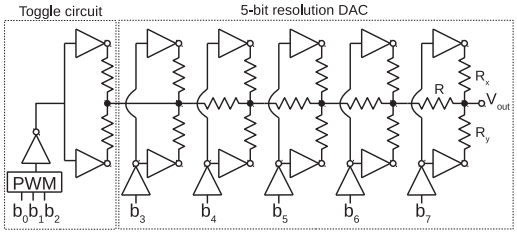

Fig. 6. The D/A converter in the integral path: this is a subranging R-2R D/A converter with extra toggle bit.

the use of low-output-impedance voltage references. To reduce the power consumption, a Pulse-Width Modulation (PWM) technique is used in the feedback path to reduce the 8-bit resolution D/A to a 5-bit resolution D/A with high accuracy [7]. The extra 3-bit resolution is obtained by modulating the output voltage of the D/A with a PWM signal during one period of the sensor VCO. The PWM signal is generated with the 8 internal signals of the sensor VCO. With PWM tuning, the power consumption of the D/A converter dropped with 30% to 31.46 μW, as 3 extra resistor branches would have been needed to achieve a resolution of 8 bit without PWM tuning.

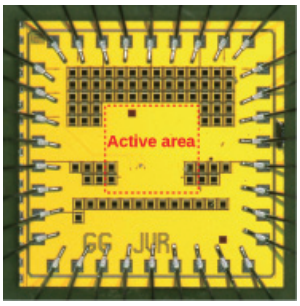

Fig. 7. Microphotograph of the chip prototyped in UMC130 CMOS technology. The active area of 455 μm x 435 μm is indicated.

IV. Measurement Results

The sensor interface has been prototyped in UMC130 CMOS technology (Fig. 7). Measurements have been performed with a resistive potentiometer of 10K emulating the resistive sensor. The maximal variation of the emulated sensor resistance is $\pm$10%, meaning that the dynamic input range of the interface is 10% of V_{DD}.

Fig. 8 (a) depicts the measured PSD of the digital output with a 1kHz -1dB$_{FS}$ (FS = 0.1·V_{DD}) sensor signal applied to the input. With f_{sample}=10 MHz and OSR=500, the SNR is measured to be 64.44dB and the SNDR 55.46dB, resulting in 10.4bit resolution and 8.9bit linearity. The complete sensor interface consumes only maximum 124.5μW from a 1V DC power supply. Phase noise (jitter) of the VCOs is the main contributor to the noise floor and limits the SNR, because the VCO phase noise has the same transfer function to the output as the input. In this design, the phase noise of -95dBc@100kHz with f_0=8MHz limits the SNR to 64.44dB. Technology limits such as the mismatch between the VCOs influence the dynamic performance such as distortion, as can be observed in Fig. 8 (a). This limits the total SNDR in practice.

Fig. 8 (b) shows the measured spectrum of the digital output for a constant resistive sensor value with different amplitudes and frequencies of noise added to the 1V DC V_{DD} (no external supply decoupling added). The supply-noise amplitude is normalized to the

TABLE I
COMPARISON OF RECENT RESISTIVE SENSOR INTERFACES

Reference	Topology	Input sensor variation	CMOS techn [μm]	ENOB	Power [μW]	Conversion time [ms]	Supply voltage [V]	FoM (pJ/conv)	PSRR [dB]	Measurement
[8]	time-based	$\pm$100 %	0.13	14.13	366	1	1.2	20.4	N/A	Yes
[9]	amplitude-based	$\pm$100 %	0.35	12.4	6000	10	3.3	11101	N/A	Yes
[10]	amplitude-based	2 %	0.35	9.67	270	3.3	1.5	1094	N/A	No
[11]	time-based	$\pm$70 %	0.35	13	27.5	5	2.5	16.78	N/A	No
[12]	amplitude-based	$\pm$1.6 %	0.7	21	1350	100	5	64.37	N/A	Yes
This work	time-based	$\pm$10 %	0.13	8.90	124.5	0.05	1	**13.03**	52	Yes

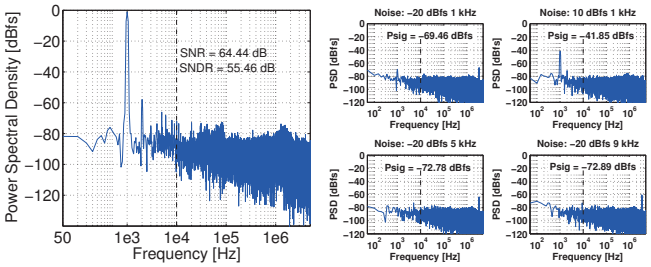

Fig. 8. (a) Measured output spectrum of the sensor interface with an emulated -1dB$_{FS}$ input signal, using a 200 000 points FFT. The vertical dashed line shows the cutoff frequency for an OSR of 500. (b) Different PSD plots of the digital output for various supply noise frequencies and amplitudes. The power of the noise frequency at the output is indicated as Psig in each plot.

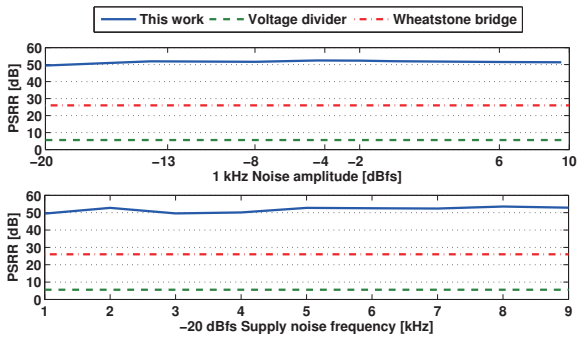

Fig. 9. (a) Measured PSRR a.f.o. -20 to +10 dB$_{FS}$ 1kHz supply noise added to the DC supply voltage. (b) Measured PSRR a.f.o. -20 dB$_{FS}$, 1 to 9 kHz added supply noise. Both measurements are compared with the simulated results of the voltage divider and the Wheatstone bridge of Fig. 2.

full-scale input of the interface, which means that the gain of the power supply to the digital output is equal to the PSRR. Fig. 9 plots the PSRR as a function of the supply noise amplitude at 1kHz and as a function of the frequency at -20dB$_{FS}$ noise amplitude. A noise-frequency-independent PSRR of 52dB on average is measured and noise amplitudes up to +10dB$_{FS}$ are tolerated, which corresponds to a tolerance of 300mV noise on a 1V DC supply voltage. Due to the fact that the interface is based on relative changes between the two VCOs and not on the absolute changes, the interface can withstand very large voltage variations, up to 300mV. An improvement of the PSRR with 46dB over the voltage divider and 26dB over the unbalanced Wheatstone bridge with ideal A/D converter is reported.

Table I compares this interface to other recent resistive sensor interfaces. Although this interface does not achieve a very high ENOB, it combines low power consumption with a fast conversion time, resulting in an energy-efficient interface. From the table it is clear that time-based topologies are more energy efficient (low $FoM = P[W] * conv.time[s]/2^{ENOB}$) than amplitude-based topologies. The sensor Figure of Merit (FoM) of 13.03 pJ/conversion for this interface is the best reported compared to recent state-of-the-art resistive sensor interfaces.

V. CONCLUSION

This paper has described a novel BBPLL-based sensor interface that combines an energy-efficient time-based design with high supply-noise tolerance for the readout of resistive sensors. The circuit has been prototyped in 130nm CMOS technology. The proposed force-balanced Wheatstone bridge technique provides a noise-frequency-independent PSRR of 52dB for noise amplitudes up to +10dB$_{FS}$, which is an increase in PSRR of 46dB over the standard voltage divider and 26dB over the unbalanced Wheatstone bridge with ideal A/D converter. Apart from the sensor calibration, no other calibrations or absolute precise voltage or clock references are needed. The chip consumes 124.5 μW from a 1V supply voltage and achieves 10.4b resolution and 8.9b linearity with a bandwidth of 10kHz. This results in a sensor FoM of 13.03 pJ/conversion, which is the best sensor FoM for the current state-of-the-art resistive sensor interfaces.

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