SESSION VII: Microwave FETs

WPM 7.2: Performance of Dual-Gate GaAs MESFETs as Gain-Controlled Low-Noise Amplifers and High-Speed Modulators

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A DUAL-GATE GaAs MESFET with 18 dB available gain at 10 GHz and minimum moise figure of 4.0 dB with 12 dB associated gain will be described. Variation of the second-gate potential yields gain modulation with 44-dB dynamic range and 70 ps risetime.

A scanning-electron micrograph of the dual-gate MESFETs center section is shown in Figure 1. The device is fabricated on a Sn-doped N-type ($N_D = 7 \times 10^{16}$ cm^{-3}) layer, epitaxially grown from Ga solution on a semi-insulating GaAs substrate. Source and drain are alloyed Au-Ge contacts with 8.5 μm separation. The two gates form Schottky-barrier contacts, each 1 μm long and 400 μm wide. The first gate is separated by 1 μm from the source and by 2 μm from the second gate. The channel thickness is 0.2 μm.

Figure 2 shows the gain versus frequency for common-source operation with the second gate RF grounded (cascode circuit)[1-3]. At 10 GHz, the dual-gate MESFET has a unilateral gain of 21 dB and a maximum available gain of 16 dB. A single-gate MESFET exhibits 11-dB maximum available gain. The dual-gate MESFETs higher gain is due to a higher output impedance and lower drain-to-first-gate feedback capacitance. Below 6 GHz, both MESFET versions are potentially unstable ($k < 1$).

The gain of a dual-gate MESFET is also dependent on the second-gate bias, V_{G_2S}, and on the reactance, X, that is connected between second gate and source. In Figure 3, the forward gain, G_f, reverse isolation, G_r, and input VSWR are plotted versus second-gate voltage for an inductive ($\tau_3 = 1/\underline{153^\circ}$*) and for a capacitive ($\tau_3 = 1/\underline{-45^\circ}$*) reactance. The first gate and the drain are image matched at $V_{G_2S} = 2.0$ V. At this bias, the inductive reactance yields 18 dB maximum available gain. If V_{G_2S} is changed from +2.0 V to −2.5 V, the gain decreases by 44 dB. Over the entire bias range, the reverse isolation never rises above −25 dB and the VSWR does not exceed 2.1:1. The capacitive reactance yields less gain (10 dB max). In this case, however, the input impedance and the transmission phase are practically bias independent. The input VSWR does not rise above 1.3:1, and the transmission phase does not vary more than 5° if the gain is decreased by 20 dB; Figure 4.

The output power at 1 dB gain compression is +10 dBm for the dual-gate MESFET with 400 μm gate width. This result is obtained for an optimum load impedance (80 Ω) and for bias voltages* yielding 130 mW dc power dissipation. At 10 GHz, the resulting small-signal gain is 9 dB. In comparison, a single-gate MESFET with identical dc bias, power consumption and small-signal gain, operated with both ports image matched, delivers +9 dBm output power. The single-gate MESFETs drain-voltage swing can be larger. It is limited by $V_{DS} - V_{D_{sat}}$** as opposed to $V_{DS} - V_{D_{sat}}$** $- V_{G_2S}$ in the dual-gate counterpart. For equal gain performance, however, the load resistance of the single-gate transistor must be considerably higher (270 Ω) which offsets the advantage of the larger voltage swing.

The minimum noise figure and associated gain are plotted versus normalized drain current in Figure 5. A second-gate termination ($\tau_3 = 1/\underline{141^\circ}$) yields low noise figure and simultaneously high gain. For $I_{DS} = I_{DSS}$, the noise figure of the dual-gate MESFET is 6.6 dB with 18 dB associated gain at 10 GHz. As the first gate is reverse biased, the drain current decreases, and the noise figure decreases to a minimum of 4.0 dB with 12 dB gain. In comparison, a single-gate MESFET exhibits a noise figure minimum of 3.2 dB with 8.0 dB gain. The noise figure difference is only 0.8 dB; however, the gain difference is 4.0 dB.

The speed for pulse modulation of an RF-signal is demonstrated in Figure 6. An 8-GHz CW signal is fed to the first gate and a synchronized modulating pulse drives the second gate. With the RF signal turned off, a drain-voltage falltime of 65 ps and a risetime of 100 ps are measured. This result demonstrates the MESFETs capability to switch between gain and high insertion loss within less than one RF cycle at X-band frequencies.

In conclusion, the dual-gate MESFET yields higher gain than its single-gate counterpart. It also enables automatic gain control over a large dynamic range with minimum transmission phase shift. In addition, it allows gain-slope compensation with a simple circuit between second gate and source. The dual-gate MESFET is also a modulator with high on-to-off gain ratio, practically gain-independent input impedance, and subnanosecond switching speed.

Acknowledgments

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*τ_3 is the reflection coefficient of the reactance X in a 50-Ω system.

*V_{DS} = 4.5 V, V_{G_1S} = -0.5 V, V_{G_2S} = 2.0 V, $\tau_3 = 1/\underline{153^\circ}$.

**$V_{D_{sat}}$ is the threshold voltage for drain-current saturation.

[1] Turner, J. and Arnold, S., "Scotky-Barrier FET's ... Next Low-Noise Designs," *Microwaves*, p. 44-49; April, 1972.

[2] Asai, S., Murai, F. and Kodera, H., "The GaAs Dual-Gate FET with Low Noise and Wide Dynamic Range at Microwave Frequencies," *Int. Electron Devices Conference Digest of Technical Papers*, p. 64-67; 1973.

[3] Maeda, M. and Minai, Y., "Application of Dual-Gate GaAs FET to Microwave Variable-Gain Amplifier," *Int. Microwave Symposium Digest of Technical Papers*, p. 351-353; 1974.

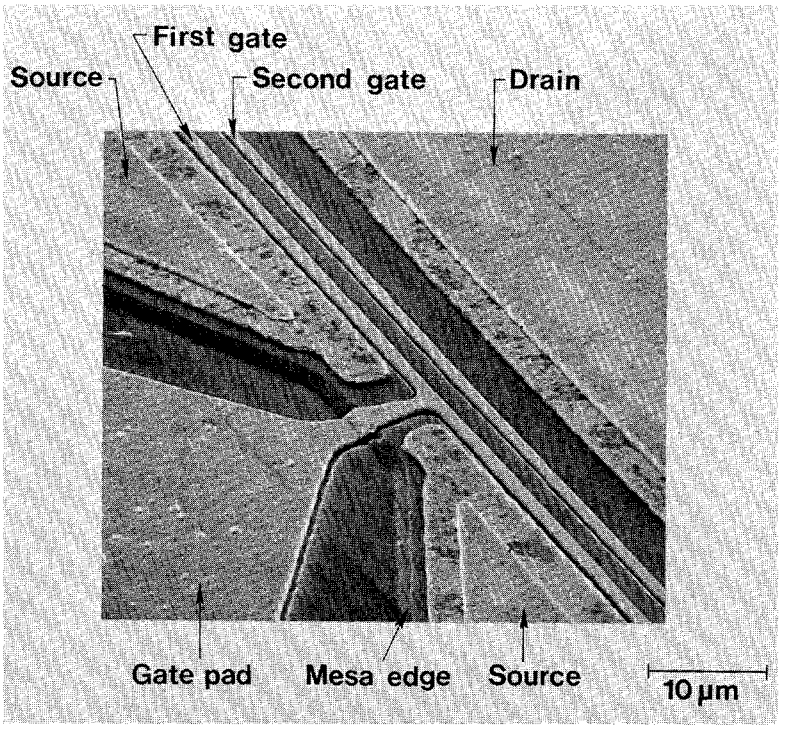

FIGURE 1—Scanning-electron micrograph of the dual-gate MESFETs center section.

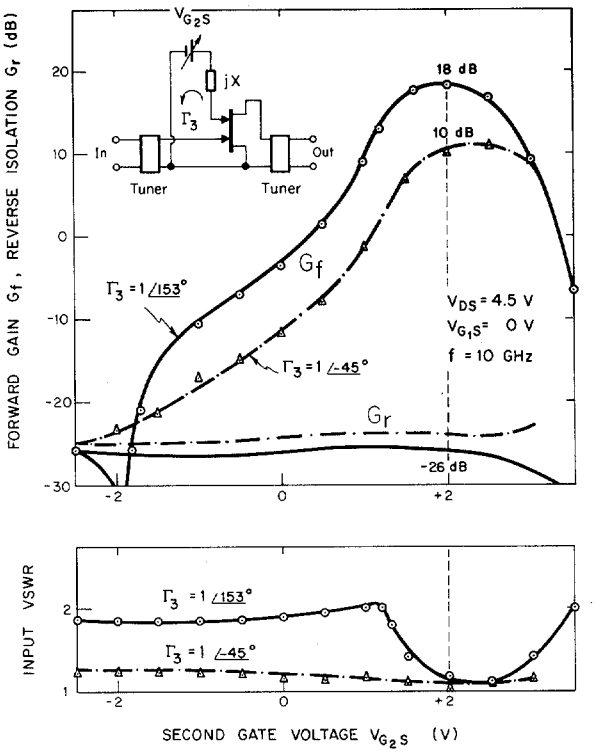

FIGURE 3—Forward gain, reverse isolation and input VSWR versus second-gate voltage for an inductive and for a capacitive reactance connected between second gate and source.

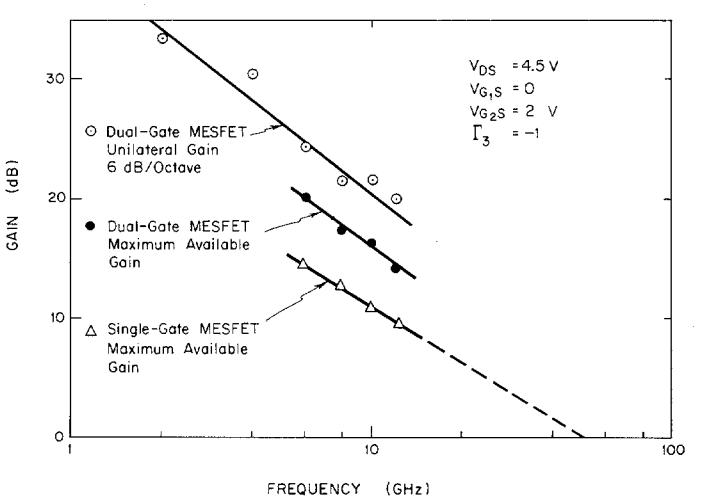

FIGURE 2—Calculated unilateral gain and directly-measured maximum available gain, plotted versus frequency for a dual-gate MESFET with RF-grounded second gate.

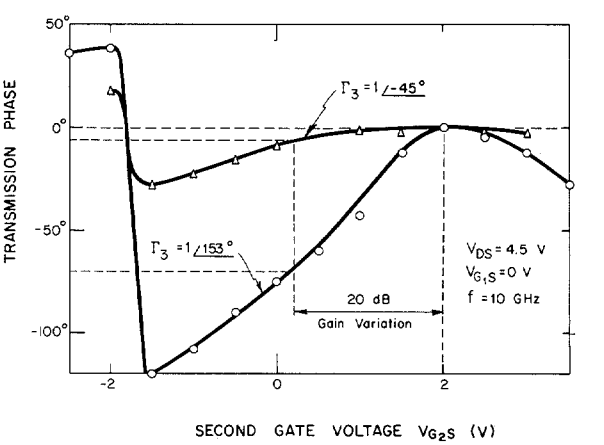

FIGURE 4—Transmission phase versus second-gate voltage for an inductive and for a capacitive reactance connected between second gate and source.

[See page 213 for Figures 5 and 6.]

An Evaluation of GaAs FET Oscillators and Mixers for Integrated Front-End Applications
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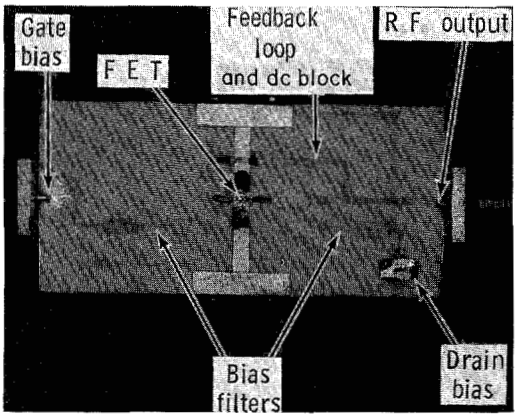

FIGURE 6—Photograph of an integrated X-band FET oscillator.

FREQUENCY (GHz)	PREDICTED POWER OUTPUT (mW)	MEASURED POWER OUTPUT (mW)
2.2	14.7 27.6	13.0 30.5
6.0	7.0 18.5	8.5 ---
11.0	6.0	6.2

FIGURE 7—Measured and predicted power output of a group of low-power FET oscillators.

Performance of Dual-Gate GaAs MESFETs as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators
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[Right]

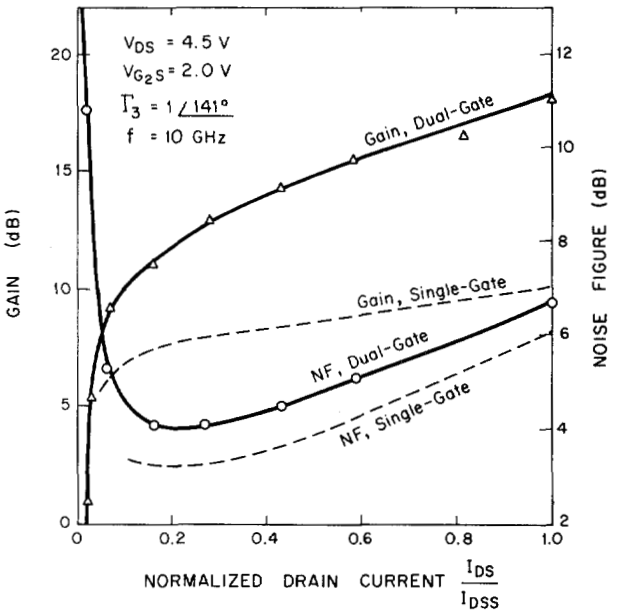
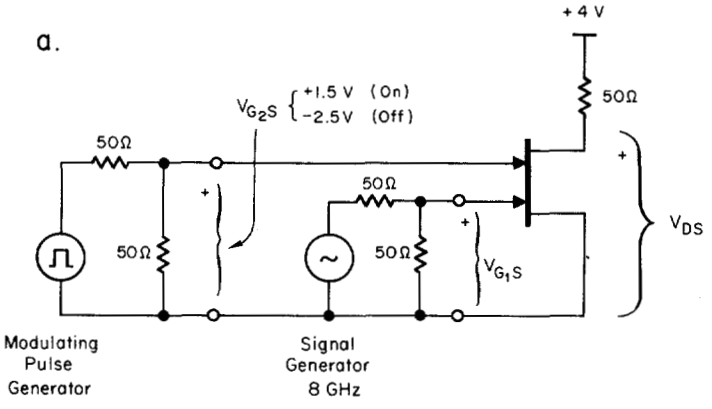


FIGURE 5—Minimum noise figure and associated gain versus normalized drain current for single-gate and dual-gate MESFETs. The current is varied by changing the first-gate bias voltage.

[Below]



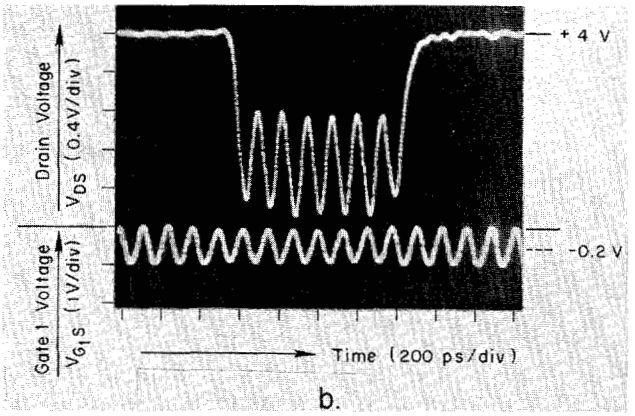


FIGURE 6—*(a)* Circuit schematic for pulsed amplitude modulation of an 8 GHz carrier; *(b)* voltage waveforms at the drain and at the first gate.