New System-in-Package (SiP) Integration Technologies

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***Abstract* — New System-in-Package (SiP) with innovative Wafer-Level-System-Integration (WLSI) technologies that leverage foundry core competence on wafer processes have been demonstrated. The WLSI technologies include Chip-on-Wafer-on-Substrate (CoWoS^{TM}) 3DIC and interposer, Integrated Fan-Out (InFO) and Chip-Scale Wafer-Level-Packaging. Wide application portfolio from very low I/O pin-count, low-cost devices, to medium, high and ultra-high pin-count are realized. Chip-partition followed by flexible powerful integration of single-chip or multi-chips, advanced or matured Si, logic and memory, SoC and sensor/MEMS. System values include low profile, low power, high bandwidth along with competitive cost can be readily achieved. With the chip-partition, we can sustain Moore's law longer.**

***Index Terms* — System-in-Package (SiP), CoWoS, 3DIC, Interposer, InFO, wafer level system integration (WLSI), TSV, fan-in, fan-out, chip partition, Moore's law.**

I. Introduction

New semiconductor market demands driven by mobile computing, wearable & health, automotive, cloud & big data, and Internet of Things (IoT) are pushing existing packaging level system integration beyond its technology limitation. Traditional packaging and assembly based system-in-package (SiP), multi-chip-module (MCM), chip-on-chip (CoC) stacking using wire bonding, and package-on-package (PoP) can only fulfill a small portion of the new market demands driven first by mobile computing and soon by wearable, health/medical, and IoT. Small form-factor and power efficiency requirement are the main challenges. These coupled with the highly cost sensitive mobile consumer market, have pushed not only the technology front, but also make change to the whole conventional semiconductor supply chain.

As the level of integration multiplied due to system scaling and product generation evolution, the off-chip interconnect pitch and density starts to dominate the system power consumption. Short battery life and device heating becomes an un-surmountable agony. The old PC-dominated power-hungry system integration strategy based on Moore's Law driving for high system performance can no longer sustain the new market needs. SoC Chip design and system integration/packaging strategy moves away from purely performance driven into more balanced approach weighing in additional key performance indicators such as power efficiency, system/product formfactor, cost, and environmental friendly requirements.[1-6]

II. Foundry Technology Platform

Wafer level system integration (WLSI) using wafer compatible process technology provides highest possible pitch density for system integration.

When different chips (heterogeneous) or similar chips (homogeneous) are interconnected/assembled using wafer process, there are two different approaches, side-by-side (horizontal 2D) or stacking (vertical 3D). Depending on the SoC design and the available process technologies for interconnection, 3D vertical stacking provides better interconnection with shorter electrical passage, and higher packing density. But it is technologically more challenging in terms of power distribution and heat dissipation, and in general with slightly higher cost. The following sessions will present available technologies that foundry established to meet the new market demands and challenges, including Chip-on-Wafer-on-Substrate (CoWoS^{TM}) 3DIC and Interposer, and Integrated Fan-Out (InFO) Wafer Level Packaging (WLP)

III. 3DIC CoWoS

3DIC Chip-on-Wafer-on-Substrate represents one of the ultimate 3D integration capabilities, where SoC and chips with transistors are stacked to form 3D interconnections. This removes off-chip interconnections and cut short all the chip-to-chip interconnection to its minimal. Needless to say, this represents the highest possible integration density and performance that current 3D IC technology can achieve.

The most important difference, compared to traditional SoC, needs to be understood is the impact of through silicon via (TSV), wafer/die thinning, and stacking to the n and pMOSFET, Fig 1 [7]. Experimental results show TSV keep out zone (KOZ) requires careful design and layout in 3DIC stacking while thinning and μbump stacking has minor effect to the transistor electrical performance for current structure and dimensions.

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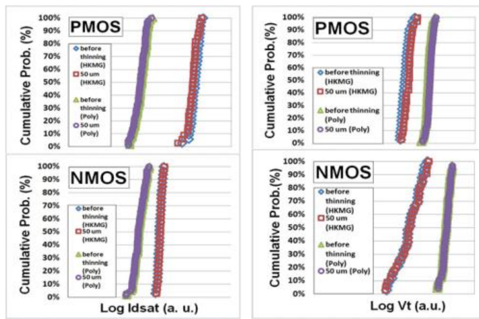
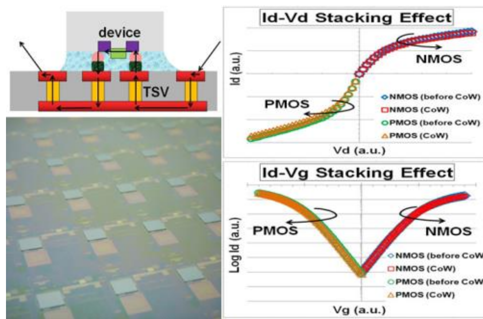
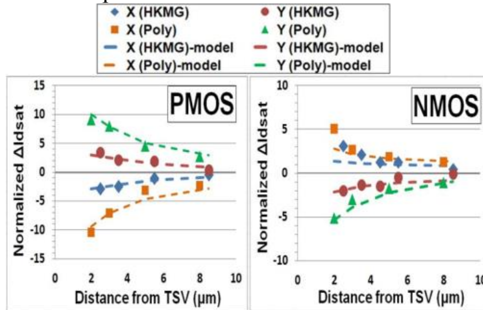


(a) Wafer thinning has little or no impact to the transistor performance



(b) Chip-on-Wafer (CoW) stacking has little or no impact to the transistor performance



(c) Δ Idsat for HKMG is smaller than for traditional polygate-SiON pMOS and nMOS.

Fig. 1 Impacts of (a) thinning, (b) stacking, and (c) TSV on advanced node transistors performance. [7]

IV. CoWoS Interposer

CoWoS interposer is already in foundry production 3D capability from 2012/2013. Since then, various sophisticated system and application have been demonstrated.

Fig 2 shows an SEM cross section image of a basic CoWoS stacking. And Fig 3 shows a few demonstrated homogeneous and heterogeneous integration examples.

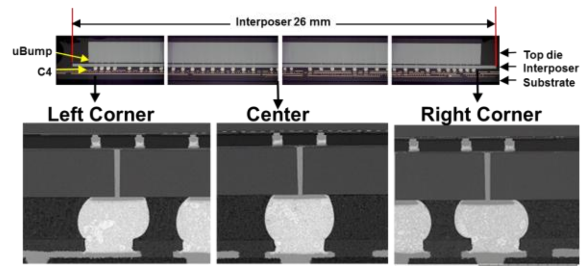


Fig 2. An SEM cross section image of a basic CoWoS stacking structure. [8]

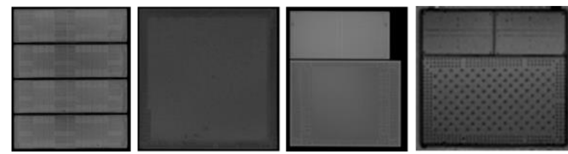


Fig 3 Both homogeneous and heterogeneous integration are demonstrated; from left to right, homogeneous 1x4, homogeneous 1x1, heterogenous 1+1, heterogeneous 1+2. [8]

The advantage of interposer system scaling compared to conventional MCM packaging is the "scaling down" in package dimension and most of all, the improvement in bandwidth and system electrical performance.

Fig 4 shows an example of a foundry turnkey system solution using a 28nm logic SoC, a 40nm eDRAM, and a 65nm GPS [9]. The 3 chips are integrated using a silicon interposer with BIST solution. Known good die (KGD) before CoW and known-good-stack (KGS) on wafer scale test are achieved before the CoW stack are ready for packaging and assembly (oS) and known-good-package (KGP) confirmed by functional tests.

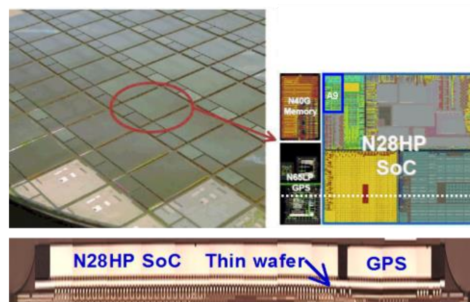


Fig 4 Foundry turnkey integration of a 28nm SoC, a 40nm eDRAM, and a 65nm GPS integrated on a silicon interposer. The system is tested known good system on wafer before packaging/assembly [9]

Another example involves 3 chips integration including a 3rd party wide IO DRAM along with a 40nm logic and a 40nm eDRAM [10]. Fig 5 shows the result of this product. This example demonstrates the possibility of getting a 3rd party chip into CoWoS turnkey flow and thus bypass any logistic hurdle that may have hindered current 3D supply chain issues. Once the 3rd party chip issue is resolved, there is no reason why CoWoS cannot integrate an HBM DRAM stack [10]. Fig 6 shows such integration has been demonstrated in foundry CoWoS platform.

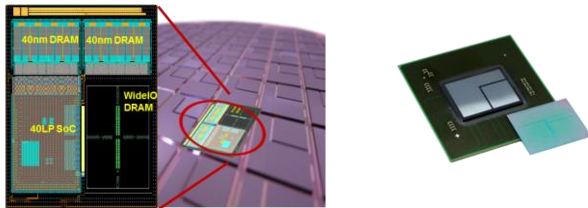


Fig 5 CoWoS interposer integration of a logic, an eDRAM, and a 3rd party wide IO DRAM onto an interposer. [10]

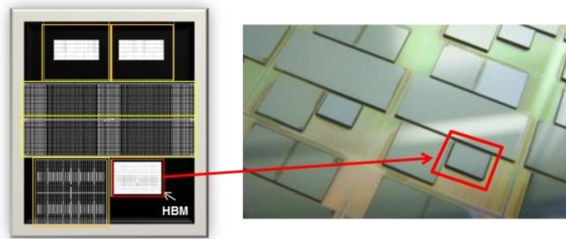


Fig 6 CoWoS interposer integration of a daisy chain HBM along with another 2 chips. Noticed the HBM stack is slightly thicker than the other chips. [10]

The first CoWoS in production is for FPGA both homogeneous and heterogeneous integration, as shown in Fig 7 [10]. The flexibility in system design and IP usage is fully demonstrated in CoWoS integration processes.

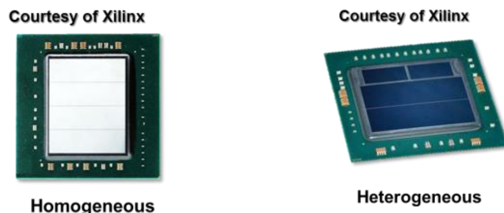
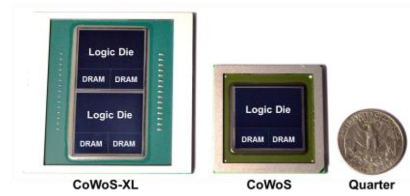
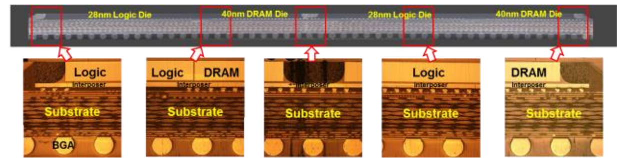


Fig 7 FPGA homogeneous and heterogenous integration using CoWoS interposer technology platform. [10]

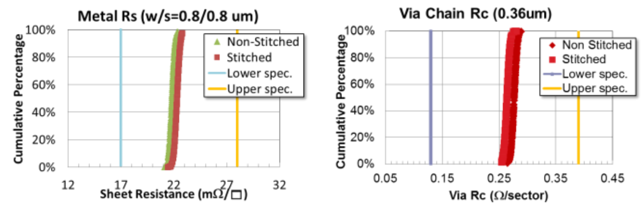
A larger interposer allows more flexible system integration capability. The interposer size limitation imposed by stepper tools reticle size is resolved by implementing a different lithographic strategy to extend the size limitation to larger than one reticle size. Fig 8 shows the result of such CoWoS-XL demonstration.



(a) Assembled CoWoS-XL and CoWoS devices size comparison.



(b) Cross section view on a stitched CoWoS-XL showing Logic-DRAM-Logic-DRAM side-by-side.



(c) Comparable resistance between stitched (CoWoS-XL) and non-stitched (CoWoS) test lines

Fig 8 CoWoS-XL demonstrated using daisy chain test vehicles.

The stitched CoWoS-XL not only performs as good as normal CoWoS, as seen in Fig 8(c), but has also passed stringent component level reliability test.

Both interposer and 3DIC are now ready for customer production and prototyping with their status summarized in Table I. [8]

Table I Summary on CoWoS 3DIC backend services [8]

Value	Integrated 3D IC backend services	
Technology	Interposer	3DIC
Baseline	CoWoS	CoWoS Co(CoS)
Prototype	Done	Now
Production	2012	2014
Market	FPGA, Server, High-end Computing,	Memory, Mobile

V. INTEGRATED FAN-OUT (INFO)

Integrated Fan-Out (InFO) is the technology using wafer scale process for chip-to-board interconnection or chip-to-chip integration using neither interposer nor organic substrate. Chips are embedded into supporting organic compound, which also serves as the basis for interconnection construction. Because of the extreme trimmed down structure, InFO has advantageous in cost, formfactor, excellent RF electrical performance, and better thermal performance compared to traditional wire bonding and flip chip packages.

Integrated fan-out wafer-level packaging (InFO-WLP) technology with state-of-the-art quality factor (Q) = 64 in 2.4GHz inductor has been demonstrated for RF systems Fig 9 and 10 [11]. For the first time, radio frequency (RF) circuits with InFO-WLP have been fabricated to illustrate how the high Q inductor can be used to dramatically improve performance and power consumption concurrently, Fig 11.

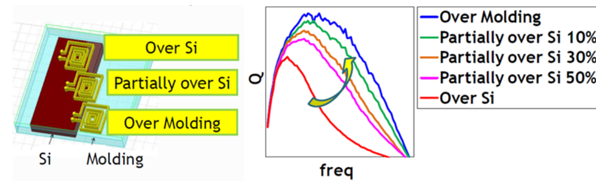


Fig 9 Q factor depends heavily on proximity to substrate. InFO Inductor (over molding) shows higher Q factor, higher f_{sr} (serial resonance frequency), and lower substrate coupling losses. [11]

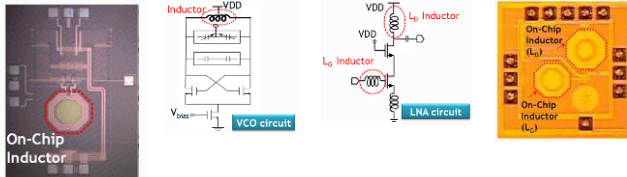


Fig 10 Voltage-controlled oscillator (VCO), benefit from the high Q inductor; Phase noise, FOM (Figure of Merit), and Power consumption. Low Noise Amplifier (LNA) benefit from the high Q inductor; improve noise figure and enhance max gain. [11]

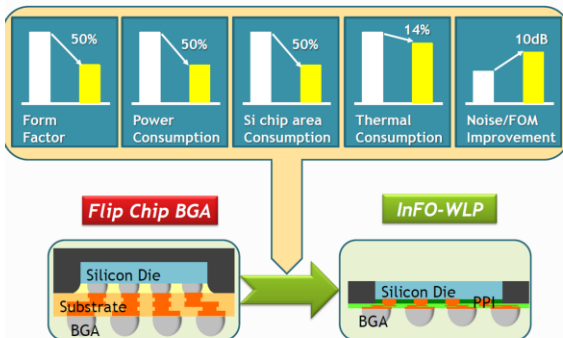


Fig 11 InFO-WLP provides formfactor reduction (50%), power saving (50%), smaller chip area (50%), lower thermal heating (14% less), and noise/FOM improvement (10 dB). [11]

InFO is an excellent platform for system function partition and integration. Fig 12 shows an example of InFO RF system with 3D vertical inductor integrated. Excellent power saving, noise reduction, and Q-factor are among the system performance improvement in additional to cost saving [12].

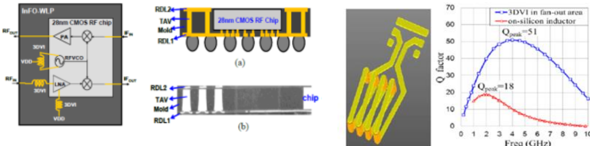


Fig 12 An integration of 28 nm CMOS RF system with 3D vertical inductors (3DVI) in integrated fan-out wafer level package (InFO-WLP). The 3DVI provides the performance of Q-factor of 51 and isolation of -53 dB. With the 3DVI, the RF system in the InFO technology results power saving of 58% and noise reduction of 80% in LNA and VCO, respectively, compared with those in RF SoC system. [12]

Another example is an integration of a 60 GHz millimeter wave system from chip, package, to PCB with a 4×4 array antenna on InFO-WLP technology as shown in Fig 13 [13],

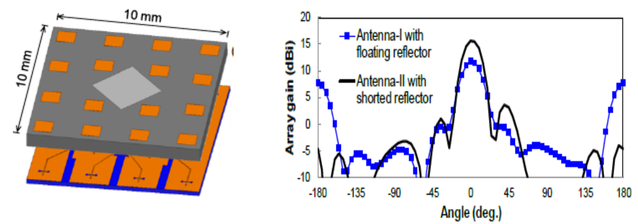


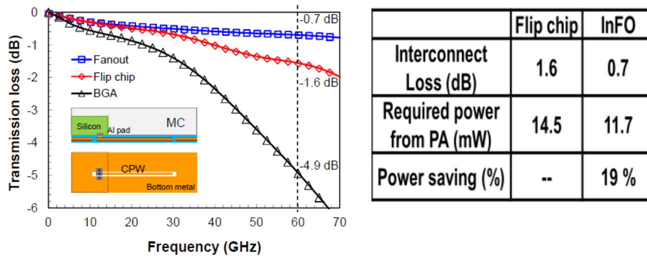
Fig 13 InFO technology provides high antenna gain of 15.6 dBi and highly competitive form factor of 10 × 10 × 0.5 mm^3 [13].

The gain of an antenna on InFO is 5.4 dBi in free space, but on a PCB with a floating reflector it decreases to 0.6 dBi. A design with a shorted reflector is applied to improve the antenna gain to 4.0 dBi. Based on the design, the performance of the mm wave system on PCB can achieve an array gain of 15.6 dBi in a form factor of 10 × 10 mm^2. To our knowledge, this represents record performance for a system with 10 × 10 mm^2 size [13].

Fig 14 shows an array antenna integrated with RF chip using InFO-WLP technology is proposed for millimeter wave system applications [14].

Aperture-coupled patch antenna is designed on the fan-out molding compound (MC). Meanwhile, the interconnect from chip to antenna feeding line is

demonstrated to only have 0.7 dB loss, which can save 19 % PA output power compared with that of flip-chip package.



	Flip chip	InFO
Interconnect Loss (dB)	1.6	0.7
Required power from PA (mW)	14.5	11.7
Power saving (%)	--	19 %

Fig 14 Transmission loss for interconnects from chip pad to antenna with InFO, C4 bump and BGA ball. InFO package only experiences 0.7 dB interconnect loss. 10 mW power required for antenna radiation. 19% more power saving in InFO interconnect than that in flip chip interconnect [14].

In summary, foundry ready InFO-WLP technology is a cost effective and versatile system integration platform enables not just the existing SiP system scaling, but also make possible of multitude of new applications.

VI. 3D Design Readiness

Foundry CoWoS and InFO system in package integration technologies are in production with complete design infrastructure in place. The CoWoS design solution includes silicon chips, stacked system, substrate, and memory IP. Fig 15 shows the high level design solution readiness [10].

3DIC	Capability	Readiness
Silicon Chips	Bump Assignment / RDL Routing	●
	Wafer-level DFT & BIST	●
	µbump DRC	●
	Cu-pillar Bump Implementation	●
	Custom Design Support	●
	TSV-to-TSV Coupling RCX / TSV RLC Subckt Replacement	●
Substrate	Substrate Routing	●
	Substrate RLC Extraction	●
Stacked System	Inter-die LVS/DRC	●
	Concurrent IR/EM	●
	Transient Thermal Analysis	●
	Integrated DFT & BIST	●
	Cross-die STA / Post-sim	●
	System PDN Simulation / TSV SSN	●
	Decap/Mimcap Co-optimization	●
	Chip-Package Bump Co-optimization	●
Memory IP	Controller, PHY	●

Fig 15 3DIC design solution CoWoS readiness [10].

For chip/InFO co-design environment, co-simulation environment to integrate chip and package design can reduce design cycle and ensure 1st silicon success. Fig 16 shows how they can be integrated into a comprehensive design environment.

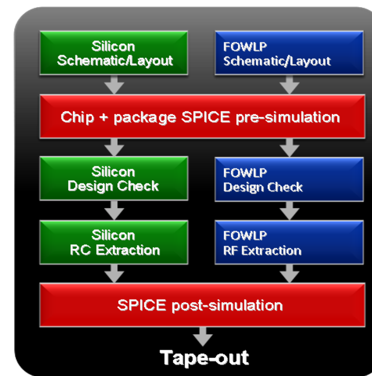


Fig 16 Chip-InFO co-design environment to integrate chip & package design that reduce design cycle and ensure 1st silicon success.

VII. Conclusion

The new versatile market demands in cloud, mobile computing, wearable & health, automotive, and internet of things, post brand new challenges for homogeneous and heterogeneous power efficient short time-to-market versatile products with volatile product life cycles. To meet such challenges, a new system in package solution using wafer level system integration platform has been demonstrated and readied based on foundry manufacture technologies and design solutions. CoWoS 3DIC and interposer are ready for server & network processors, FPGA, CPU, GPU, and mobile computing. InFO and WLP are ready for mobile, automotive, wearable & health, and IoT.

While application driven system integration diversifies beyond Moore's Law and customized system scaling demands balancing between cost and performance, foundry provides turn-key chip-package co-design and manufacturing solution to meet the new market demands and challenges. Weather it is for More Moore or More than Moore, the new foundry SiP integration technologies are here to meet the challenges.

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