High-resolution 60-GHz DCOs with Reconfigurable Distributed Metal Capacitors in Passive Resonators

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***Abstract*—Mm-wave digitally-controlled oscillators (DCOs) with reconfigurable passive resonators are proposed, which achieve wide tuning range (>10%) and fine frequency resolution (<1 MHz) simultaneously. Two 60-GHz implementations: a fine-resolution inductor-based DCO (L-DCO) and a transformer-based DCO (T-DCO) are demonstrated in 90-nm CMOS, exploiting metal capacitors only for frequency tuning. Both DCOs obtain >9.7% linear tuning range and phase noise lower than −90.5 dBc/Hz at 1-MHz offset across the 56–62 GHz range. The T-DCO achieves fine frequency tuning step of 2.5 MHz, whereas that of the L-DCO is better than 160 kHz. The L-DCO and T-DCO consume 10 mA and 12 mA, respectively, from a 1.2-V supply. The core size of each DCO is 0.4×0.4 mm^2.**

I. Introduction

Frequency-modulated continuous-wave (FMCW) radar sensors operating in the millimeter-wave (mm-wave) regime offer fine-resolution object detection and identification at short range. A linear frequency ramp with a minimum 6-GHz bandwidth is required to achieve a range resolution under 5 cm at 60 GHz [1]. To synthesize an FMCW carrier, the all-digital phase-locked loop (ADPLL) shown in Fig. 1 is proposed, which allows reconfigurability and permits the highest degree of integration of the radio front-end with the digital baseband [2]. MOS varactors are commonly used to tune DCOs in the low-GHz range. However, their quality factor (Q) is as low as ∼5 for 50 fF at 60 GHz and the varactor capacitance ratio, C_{max}/C_{min}, of 2–3 limits the DCO frequency tuning range. Moreover, a frequency tuning step lower than 1 MHz also cannot be achieved using varactor tuning. Thus, it is no surprise that only two DCOs operating above 50 GHz [3] [4] are reported, and none reported to date have achieved 10% tuning range and sub-MHz tuning steps simultaneously.

To achieve 6-GHz linear DCO tuning range with sub-MHz frequency resolution at 60 GHz, passive resonators loaded by reconfigurable distributed metal capacitors are introduced. Metal strips placed beneath a resonator (i.e., transmission line, inductor and transformer) are configured by MOS switches to load the tank with more (or less) capacitance, thereby varying the DCO resonant frequency. The influence of these strips on the tank varies with position along the length of the resonator. Strips close to the virtual ground node of a differential resonator introduce significantly less capacitance (on the order of aF) than strips near the RF input terminals. In this paper, a 60-GHz DCO prototype (inductor-based, L-DCO) demonstrated 160-kHz resolution with this technique. Another version (transformer-based, T-DCO) places the metal capacitor

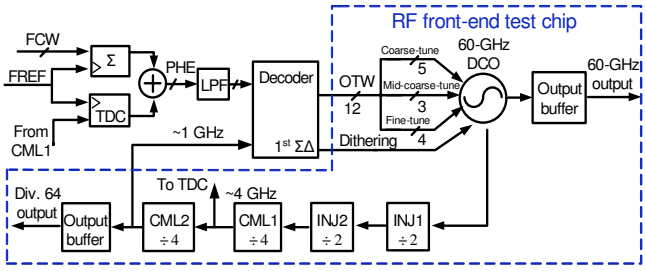

Fig. 1. 60 GHz ADPLL and RF front-end test chip block diagram.

bank (i.e., strips) at the secondary coil, which loads the primary tank via magnetic coupling to achieve fine-tuning. This 60-GHz T-DCO achieves 2.5 MHz tuning step with less than 5% mismatch. Coarse-tuning in both DCOs by digitally-controlling a reconfigurable transmission line (TL) achieves a 6-GHz linear tuning range. Both DCOs have measured phase noise (PN) better than −90.5 dBc/Hz at 1-MHz offset. Compared to MOS varactor-based tuning, the proposed approach is less sensitive to process, voltage and temperature (PVT) variations, facilitating calibration of the DCO in an ADPLL.

II. 60-GHz DCO with Inductor-based Fine-tuning (L-DCO)

The proposed tunable resonator for both L- and T-DCOs exploits the multiple metal layers available in nano-scale CMOS technologies (e.g., 7 to 9 metal layers). To achieve a tuning range of 10% and sub-MHz fine-tuning steps simultaneously, a 3-stage segmented tuning is employed. It consists of a coarse-tuning bank (CB), a fine-tuning bank (FB), and a mid-coarse-tuning bank (MB) to bridge the gap in step-size between CB and FB. Thermometer codes are used to ensure monotonicity.

A simplified 60-GHz L-DCO schematic is shown in Fig. 2(a). An NMOS cross-coupled pair ($M_{1,2}$) provides sufficient negative resistance to sustain the oscillation. One oscillator output drives a divide-by-64 chain, while the other drives a single-ended 50-Ω output buffer for characterization.

A. Design of Inductor-based Fine-tuning Bank (FB)

Advanced CMOS process lithography allows the creation of a differential least significant bit (LSB) varactor on the order of tens of attofarads [2], corresponding to a frequency resolution of ∼10 MHz at 60 GHz. Moreover, parasitic capacitance of the interconnections within the varactor bank is comparable to, or even higher than the minimum varactor capacitance at

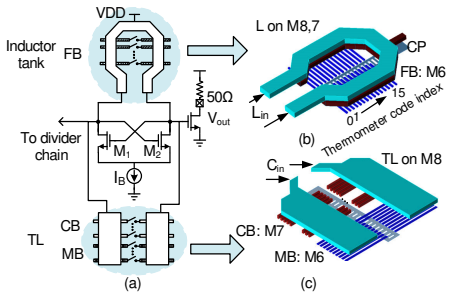

Fig. 2. (a) Schematic of the proposed 60-GHz L-DCO; (b) inductor-based fine-tuning; (c) reconfigurable TL as coarse- and mid-coarse-tuning.

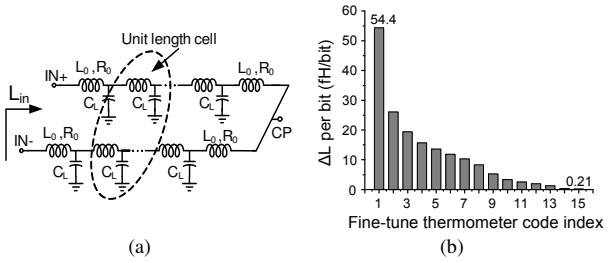

Fig. 3. (a) Simplified circuit model of inductor-based fine-tuning; (b) simulated ΔL/bit in the fine-tuning bank.

mm-wave frequencies, degrading matching in the tuning bank. To achieve frequency resolution on the order of kHz while avoiding the use of components with minimum dimensions, we propose the inductor-based capacitance reduction technique illustrated in Fig. 3(a). A differential inductor of length l is divided into several units differentially-loaded by $C_{load} = C_L/2$ in each sub-section. Although the C_{load} array is unit-weighted, the impact of each C_{load} on the equivalent input inductance (L_{in}) is different. Locating C_{load} close to center-tap (CP) has less effect on L_{in} compared to directly loading the inductor at its differential inputs.

Equal width metal shield strips are placed beneath the inductor of the L-DCO (see Fig. 2(b)) on M6 (1-μm width and 1-μm spacing). Shorting a metal strip pair with an NMOS switch increases C_{load} in the given sub-section. A thermometer code applied to the MOS switches from the differential inputs to CP gives the simulated L_{in} change per bit (ΔL/bit) plotted in Fig. 3(b). The ΔL/bit is reduced progressively from 54.4 fH to 0.21 fH, corresponding to a Δf at 60 GHz of 23 MHz and 140 kHz, respectively. L_{in} increases from 75.8861 to 76.0606 pH when the 15-bit thermometer code changes from all 0s to all 1s. Thus, high frequency resolution is achieved without exploiting minimum-sized capacitors or varactors for tuning. Moreover, a binary-weighted fine-tuning bank could be realized by carefully positioning the metal shield strips beneath the inductor with varied spacing.

B. Coarse- and Mid-coarse-tuning Bank (CB and MB)

A digitally-controlled reconfigurable transmission line (TL) is used for both coarse- and mid-coarse-tuning as shown in Fig. 2(c). Shorting metal strips beneath the differential TL via NMOS switches increases the capacitance per unit length,

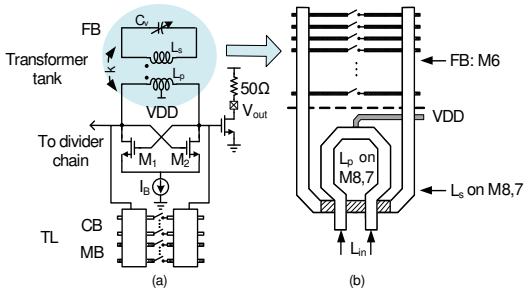

Fig. 4. (a) Schematic of the proposed 60-GHz T-DCO; (b) top layout view of T-DCO fine-tuning bank.

thus reducing the wavelength ($\lambda = 1/f\sqrt{LC}$) of the RF signal as shown in [5] [3]. This increases the phase shift along the TL and reduces the tank resonant frequency. The proposed CB makes use of this slow-wave attribute to digitally-control the phase shift on the TL by either opening or shorting the metal shield strips, thereby increasing or decreasing the frequency. Different metal layers beneath the TL are exploited to realize CB and MB (i.e., M7 and M6 in Fig. 2(c)) in a compact structure.

A 19-bit thermometer code CB and 8-bit MB are implemented as shown in Fig. 2(c). The 60-GHz oscillation signal runs on the top TL of 34.5-μm width, 120-μm length and 39.6-μm spacing. Each bit in CB (i.e., M7 strips) can introduce a ΔC of 1 fF corresponding to 315 MHz at 60 GHz, whereas the MB located on the (lower) M6 achieves a ΔC of 0.13 fF/bit ($\sim$1/8 of the CB step-size). The capacitance ratio (C_{max}/C_{min}) of 1.6 provides over 6-GHz tuning range and a minimum Q-factor of 8. Floating dummy strips added between the CB and MB minimize magnetic coupling between banks.

III. 60-GHz Transformer-based DCO (T-DCO)

Although the L-DCO achieves a fine frequency resolution of $\sim$100 kHz/bit, a linear tuning characteristic in FB is desired for the FMCW synthesis since a simple binary-to-thermometer decoder could be used. Therefore, another capacitance reduction technique based on a transformer resonator with linear tunability was also exploited. The schematic of the proposed T-DCO is show in Fig. 4(a). It uses the same CB and MB as the L-DCO and drives an identical divider chain. As shown in Fig. 4(a), the primary coil of the transformer (L_p) is connected to the MOS cross-coupled pair, while the secondary coil (L_s) is connected to a variable capacitor load (C_v). Varying C_v changes L_{in} as seen from the primary coil inputs. Compared to directly loading the primary coil inputs by C_v, the capacitive loading effect on L_{in} is reduced by a factor proportional to k^2. When the transformer windings are weakly coupled (e.g., $k = 0.3$), a capacitance reduction factor larger than 10 can be achieved. Moreover, a linear FB can be formed by replacing C_v in Fig. 4(a) by a unit-weighted capacitor array.

The detailed implementation of the transformer-based FB is shown in Fig. 4(b). Another digitally-controlled differential TL loads the secondary coil of the transformer. Shorting each strip pair introduces a ΔC of 50 aF. The primary and the secondary inductances of the transformer are 72.3 pH and 58.9 pH each,

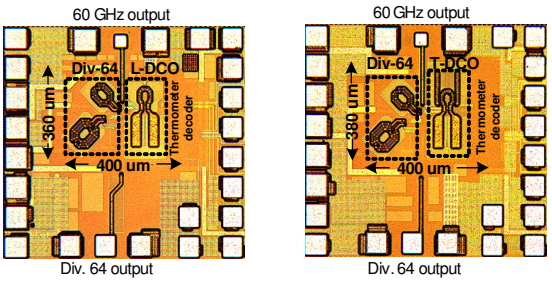

Fig. 5. Test chip microphotographs: (a) L-DCO; (b) T-DCO.

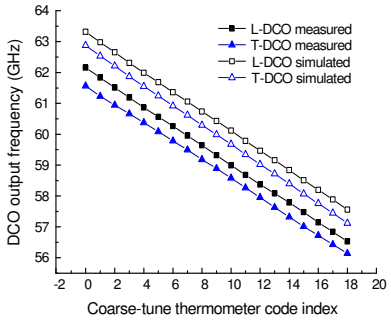

Fig. 6. Coarse-tuning curves in L- and T-DCOs.

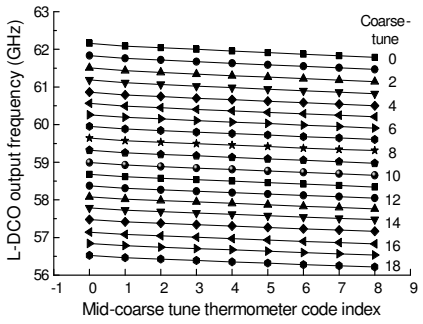

Fig. 7. L-DCO mid-coarse-tune (MB) curves for each coarse-tune (CB) code.

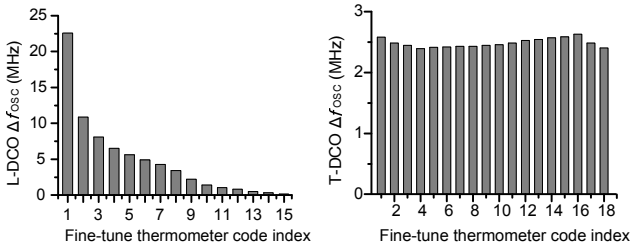

Fig. 8. DCO fine-tuning frequency step: (a) L-DCO; (b) T-DCO.

and the coupling factor k is 0.275. The equivalent inductance change seen from the primary coil is 6 fH/bit, corresponding to ∼2.5 MHz at 60 GHz. An 18-bit thermometer code FB is implemented in the test chip to prove the concept. Higher frequency resolution can be obtained by resizing the shielding strips on lower metal layers. The unwanted coupling between adjacent metal strips adds nonlinearity to the tuning curve. It is accounted for by optimizing the width of the metal strips and the gap between adjacent metal strips with the aid of EMX electromagnetic (EM) simulator [6]. The simulated Q-factor of the transformer-based FB is 16.5 in the 60-GHz band.

IV. Experimental Results

DCO test chips verifying the proposed idea are implemented in IBM's 90-nm CMOS on a 1.5 Ω-cm substrate [7]. Die microphotographs of the DCOs are shown in Fig. 5. The core size for both designs is 0.4×0.4 mm^2, including the RF parts and the binary-to-thermometer decoder. More than three dice are measured for each DCO. The L-DCO and T-DCO cores consume 10 mA and 12 mA, respectively, from a 1.2-V supply. The divide-by-64 chain and the output buffers added for characterization consume 18 mA in total.

A. L-DCO Measurement Results

The L-DCO has a measured tuning range from 56.15 GHz to 62.158 GHz. The measured and simulated coarse-tuning (CB) curves are plotted in Fig. 6. The CB of the L-DCO realizes linear tuning of 312 MHz/bit with less than 12% variation. Fig. 7 demonstrates the linear tuning of the MB at each CB code. More than 8% overlap between the adjacent frequency tuning curves in Fig. 7 guarantees continuous tuning across the entire range. A larger overlap ratio can accommodate larger PVT variations.

The measured L-DCO fine-tuning step for each bit in the FB (when CB=8 and MB=0) is shown in Fig. 8(a). A progressive reduction in the step-size is clearly observed from 22.5 MHz for the first bit in the FB (i.e., farthest from the CP point), to 160 kHz for the last bit. The minimum tuning range of the FB (52.3 MHz, obtained at maximum CB and MB codes) is over 30% larger than the tuning step in the MB, which ensures frequency tuning continuity for all DCO tuning codes.

The L-DCO RF output spectrum when oscillating at 60.864 GHz is shown in Fig. 9. After de-embedding the loss of the cables and probes, the measured output power is −3.4 dBm at 60.864 GHz. The PN at the divide-by-64 output is −127.83 dBc/Hz at 1-MHz offset from a 951-MHz carrier, as shown in Fig. 10. A separate measurement of the L-DCO output PN (−91.5 dBc/Hz at 1-MHz offset) agrees well with the theoretical $20\log_{10} N$ ($N = 64$) relationship. The measured L-DCO PN across the entire tune range is better than −90.5 dBc/Hz at 1-MHz offset (see Fig. 11), which is just 1 dB poorer than that predicted from simulation.

B. T-DCO Measurement Results

The measured T-DCO coarse-tuning characteristic, which is comparable to the L-DCO, is also plotted in Fig. 6. The T-DCO tuning range is from 55.7 to 61.56 GHz. The measured tuning step in FB for each thermometer code is plotted in Fig. 8(b). The FB has a mean DCO tuning step of ∼2.5 MHz with less than 5% systematic mismatch, which could be digitally predistorted. The mismatch can be further improved by adding dummy shield strips at the edges of the structure. One extra bit in the FB is reserved for sigma-delta dithering in the ADPLL

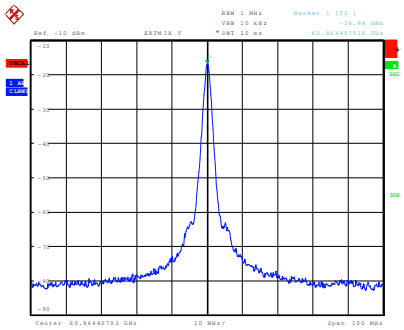

Fig. 9. 60-GHz L-DCO output spectrum.

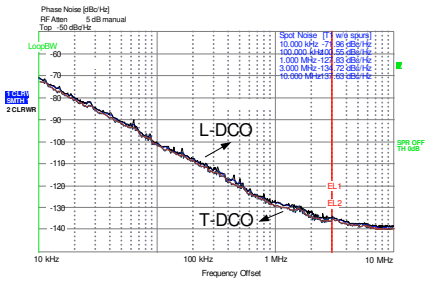

Fig. 10. PN plots of L-DCO and T-DCO at divide-by-64 output.

at the system level. A first-order sigma-delta with 8 fractional bits would yield a frequency resolution of 1 kHz in the 60-GHz band [8].

Phase noise at the divide-by-64 output of the T-DCO is plotted in Fig. 10. The PN across the entire tuning range is about 1 dB better than the L-DCO (see Fig. 11), and the output power is 0.5 dB higher due to the higher biasing current. The performance of the L- and T-DCOs are compared to the other designs from the recent literature in Table I. Only two DCOs above 50 GHz have been reported [3] [4]. A commonly used oscillator figure of merit, FoM_T, includes the frequency tuning range but fails to account for the frequency resolution that is crucial for DCOs. The proposed L- and T-DCO stand out with wide tuning range (FTR) and fine frequency resolution (f_{res}) for comparable PN performance.

V. Conclusion

Two 60-GHz DCOs (each including divider chain) intended for all-digital PLLs (ADPLL) are proposed and implemented in a 90-nm CMOS. Both DCOs demonstrate the advantages of a passive resonator loaded by reconfigurable distributed metal capacitors for frequency tuning. The inductor-based fine-tuning (L-DCO) progressively realizes finer frequency resolution that is ultimately better than 160 kHz at 60 GHz. Transformer-based fine-tuning (T-DCO) via weak magnetic coupling reduces the tuning capacitance required without the need for minimum-sized capacitors. The measured T-DCO fine-tuning step is ∼2.5 MHz. The T-DCO is not limited by the physical size of the inductor (a limitation of the L-DCO) and more fine-tuning bits can be implemented as required. Moreover, a simple binary-to-thermometer decoder is sufficient for tuning word generation in an ADPLL, since all three tuning banks in the T-DCO are linear. Both DCOs achieve

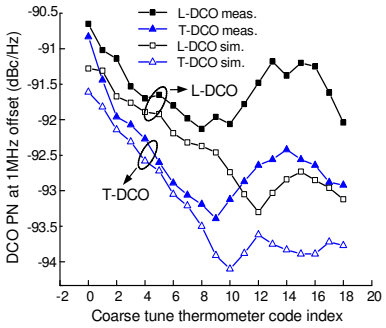

Fig. 11. PN of 60-GHz DCOs at 1-MHz offset across the tuning range.

TABLE I
Comparison of State-of-Art Oscillators above 50 GHz

Ref.	Type	F_0 (GHz)	FTR (%)	F_{res}	PN (dBc/Hz)	P_{DC} (mW)	FoM_T (dBc/Hz)	CMOS
[3]	DCO	58.27-63.83	9.3	2.3 bit	−90.1	10.6	−174.9	90 nm
[4]	DCO	51.3-53.3	4	10 bit 1.8 MHz	−116.5[1]	2.34	−179.2	90 nm
[9]	VCO	56-60.35	7.4	NA	−95	22(IQ)	−174	65 nm
[10]	VCO[2]	57-66	14.6	NA	−75	28(IQ)	−159.5	45 nm
L-DCO	DCO	56.22-62.16	10	12 bit 160 kHz	−93	12	−177.9	90 nm
T-DCO	DCO	55.83-61.55	9.75	12 bit 2.5 MHz	−94	14	−177.9	90 nm

[1] PN @ Δf=10 MHz; the rest are at 1 MHz. [2] High/low-band two VCOs.
$FoM_T = PN - 20\log_{10}(F_0/\Delta f \cdot FTR/10) + 10\log_{10}(P_{DC}/1\text{mW})$

∼6-GHz tuning range and PN better than −90.5 dBc/Hz at 1-MHz offset. Thus, digitally-controlled passive resonators avoid the use of low-Q MOS varactors and improve the manufacturability and repeatability of mm-wave ADPLLs.

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