3nm GAA Technology featuring Multi-Bridge-Channel FET for Low Power and High Performance Applications

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Abstract— As the most feasible solution beyond FinFET technology, a gate-all-around Multi-Bridge-Channel MOSFET (MBCFET) technology is successfully demonstrated including a fully working high density SRAM. MBCFETs are fabricated using 90% or more of FinFET processes with only a few revised masks, allowing easy migration from FinFET process. Not only on-target but also multiple Vt is achieved in challengingly limited vertical spacing between channels. Also, reliability of MBCFETs is shown to be comparable to that of FinFETs. Three representative superior characteristics of MBCFET compared to FinFET have been demonstrated — better gate control with 65 mV/dec sub-threshold swing (SS) at short gate length, higher DC performance with a larger effective channel width (Weff) at reference footprint, and design flexibility with variable nanosheet (NS) widths. The optimization of the standard cell design by using variable NS width is evaluated. The usefulness of MBCFET as a multi-purpose performance provider is proven by the modulation of effective capacitance (Ceff), effective resistance (Reff) and frequency by Weff control. Finally, mass production feasibility with MBCFET is proven through a fully working high density SRAM circuit.

I. Introduction

FinFET technology which was introduced to overcome limitations of planer technology is facing critical scaling challenges. As fabrication becomes increasingly complex, performance gain with continued scaling poses many difficulties and roadblocks. For the extension of FinFET technology, Fin width scaling for better gate controllability, Fin pitch scaling for capacitance reduction, and Fin height increase for DC current increase have been crucial factors [1-3]. Currently they are all facing the lack of process margin in areas of Fin etching, cutting, leaning and so on. Meanwhile, effective channel width (Weff) increase is continuously demanded for the performance improvement, although the cell height is reduced in the scaled technology nodes (Fig. 1). This has been achieved mainly by Fin height increase. However, the resulting performance improvement is less than expected because of parasitic capacitance increase. In addition, having a discrete number of Fins restricts the design optimization of standard cells and SRAM cells in terms of the balance between effective capacitance (Ceff) and effective resistance (Reff). Multi-Bridge-Channel MOSFET (MBCFET), having a vertically stacked NS and a Gate-All-Around (GAA) structure, has been proposed as a promising candidate for replacing FinFETs in the future nodes [4-7]. MBCFETs can have superior DC performance and better short channel control compared to FinFET due to the uniform channel thickness, the larger Weff and the GAA structure. The wide range of variable nanosheet (NS) widths, as opposed to the discrete number of Fins for FinFET, can also give the additional benefit in the design flexibility. Not only the performance gains but also the easy migration from the previous node should be considered for the mass production. The reusability of process and circuit design is also considered in this paper.

II. Device Design and Fabrication

The structural difference between FinFET and MBCFET is compared in Fig. 2. Contrary to vertically placed 3-dimensional channels of FinFETs, GAA channels are horizontally placed in MBCFETs. As a limitation of vertically placed channel, all Fins have a fixed height, and only a discrete number of Fins can be placed in a standard cell. On the contrary, various NS widths of MBCFET can be fabricated in the same wafer using direct patterning (Fig. 3). In addition, thin uniform thickness channel formed by epitaxial growth results in less variation than channel formed by etching.

Considering easy migration of process from previous technology, most FinFET processes are reused. On top of the FinFET baseline process, less than 10% of the processes are modified for MBC structure formation. The fabrication steps are as follows. Several pairs of Si channel and sacrificial layers are sequentially grown by epitaxial growth. Conventional Fin formation processes are used for channel definition and STI process. After Fin formation, similar processes are used for dummy poly gate (PC) formation. During the conventional source-drain process, inner-spacer is

formed for parasitic capacitance reduction and internal gate length definition at the source-drain module [8]. Sacrificial layers located between the channels are selectively removed at the Replacement Metal Gate (RMG) module for channel formation [9]. For the evaluation of sacrificial layer removal, gate conductance curves are compared with two different removal conditions (Fig.4). Contrary to humped curve induced by residue of sacrificial layer, the optimized process has clean conductance curve which means the full removal of sacrificial layer. Conventional IL/high-k and Work Function Metal (WFM) processes are used to meet the Vt target of the CMOS and multi Vt [10]. The following MOL and BEOL processes are with the same as the conventional FinFET ones.

III. Electrical Characteristics

The excellent gate controllability with very short gate length for both N- and PMOS devices is demonstrated by the MBCFET GAA structure as shown in Fig. 5. N- and PMOS sub-threshold swing (SS) of 65 and 67 mV/dec are achieved, respectively. In addition, improved N- and PMOS DC performance relative to FinFET is also demonstrated with MBCFET due to larger Weff and higher carrier mobility as well as better short channel control of the GAA structure. Fig. 6 shows a typical N- and PMOS Idsat-Idoff correlation, demonstrating 31% and 26% Idsat improvements, respectively, relative to FinFET with the same CPP and standard cell height. The reason for smaller DC improvement of PMOS compared to that of NMOS comes from the mobility difference due to the change in channel orientation from (110) to (100) [11].

For the vertically stacked NS structure, minimum vertical space between NS to NS is the key parameter to minimize the parasitic capacitance [12]. By full elimination of sacrificial layers and WFM and deposition of different types of WFM in a limited space, CMOS Vt targeting has been demonstrated (Fig. 7). On top of CMOS Vt process, three different flavors of Vt for N- and PMOS are achieved with modulation of WFM engineering (Fig. 8). High selectivity and a stable etch rate during the etch process for the various combination of WFM are inevitable processes to make different flavors of Vt.

Considering easy migration, modified standard cell from FinFET is used for evaluation. Contrary to restricted cell design of FinFET induced by the discrete number of Fins and fixed Fin pitch, flexible cell design with MBCFET is possible utilizing variable NS widths [13]. Considering the purpose of each device, wider or narrower NS widths can be used within the active area. Modification of NS size and position within the active region is also conceivable method for optimized cell design.

Modulations of DC performance and frequency using various NS widths are demonstrated on a single wafer (Figs.9, 10). Due to Weff increase without short channel effect degradation, DC performance can be improved by NS width increase. Frequency can be also improved by NS width increase because of the larger reduction of AC Reff than the increase in Ceff with increased Weff as shown in Fig. 11. Due to the relatively increased parasitic resistance at wider NS width, however, speed gain continuously decreases as NS width increases further. Using larger modulation of the frequency induced by freedom of circuit design, multi-purpose performance provider such as low power device or high performance device can be easily supported.

As shown in Figs. 12, comparable time dependent dielectric breakdown (TDDB) to those of FinFET is achieved with a reliable MBC formation. In addition, self-heating of MBCFET is investigated with 3D TCAD simulation by using the spherical harmonics expansion Boltzmann transport equation (SHEBTE) model. Channel peak temperature is analyzed at various test frequencies, while applying periodic pulses. Similar to SOI devices, the peak temperature of MBCFET converges to that of FinFET as the pulse frequency increases, resulting in no significant difference at a typical circuit speed (Fig. 13).

IV. MBCFET SRAM

To check the feasibility of mass production with MBCFET, high density SRAM macro is fabricated, in which all the 6T SRAM and peripheral circuits are composed of MBCFETs. The butterfly curves of the HC SRAM cell are measured at different voltages ranging from 0.4 to 1.1V. The Static Noise Margin (SNM) of 0.18V and 0.13V is achieved for 0.7V and 0.5V operation, respectively, which is comparable to that of FinFET SRAM with a similar footprint (Fig. 14). The Shmoo plot of high density HC SRAM macro illustrates full read and write capability with large V_{DD} margin (Fig. 15).

V. Conclusions

Highly manufacturable 3nm MBCFET technology is presented. Three representative superior characteristics compared to FinFET are demonstrated with hardware—near ideal SS of 65 mV/dec and 31% higher on current with a larger Weff at reference footprint and design flexibility with variable NS widths. Easy process and cell design migration from FinFETs are demonstrated using optimization based on the Fin process and mask set. Key reliability characteristics of MBCFET are also confirmed with reliable GAA processes. Finally, mass production feasibility with MBCFET at the 3 nm technology node is proven through a fully working high density SRAM circuit.

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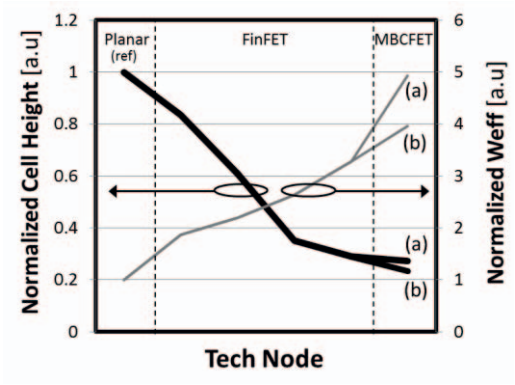

Fig. 1. Cell height and effective width trend with technology node scaling. (a) MBCFET with same design rule as FinFET (b) MBCFET with optimized standard cell design by variable NS width.

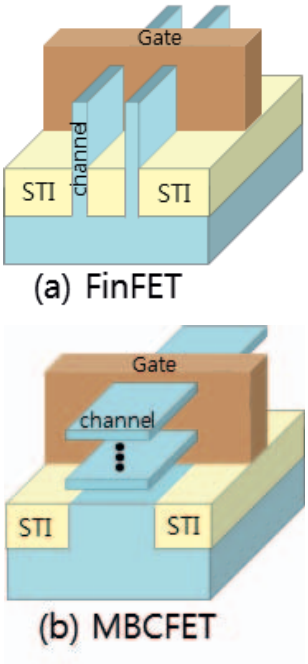

Fig. 2. Schematic comparison between (a) FinFET with vertical channel and (b) MBCFET with horizontal channel. Multiple numbers of NSs are vertically stacked.

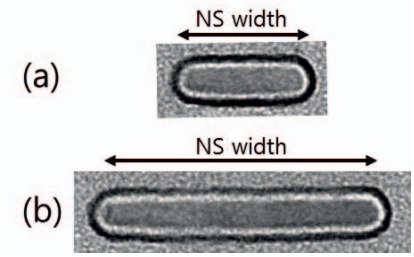

Fig. 3. Variable NS width formed by direct patterning. (a) Narrow width NS for high density SRAM or low power devices, (b) Wide width NS for high performance devices.

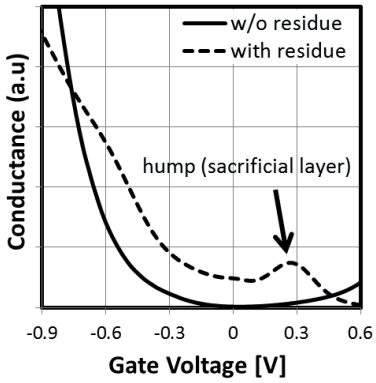

Fig. 4. Gate conductance comparison between two different sacrificial layer removal conditions. Clear curve without hump is proving the full removal of sacrificial layers.

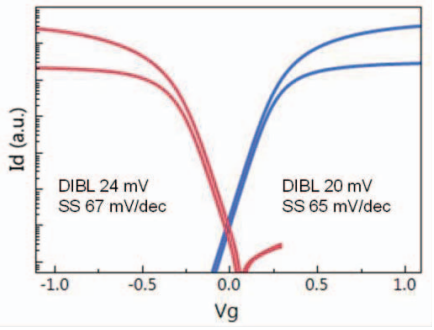

Fig. 5. Superior short channel effect with Gate-All-Around structure; N- and PMOS subthreshold swing of 65mV/dec and 67mV/dec, respectively.

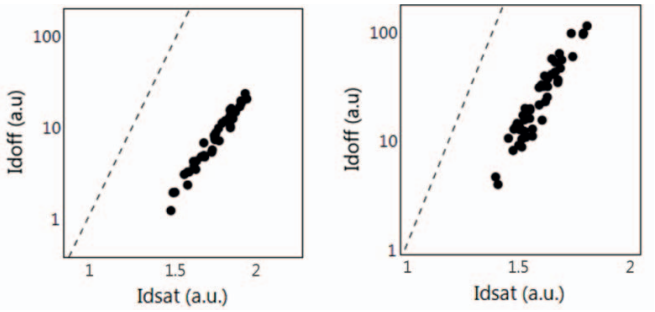

Fig. 6. MBCFET showing Idsat improvement of NMOS 31% and PMOS 26% compared to FinFET with the same CPP.

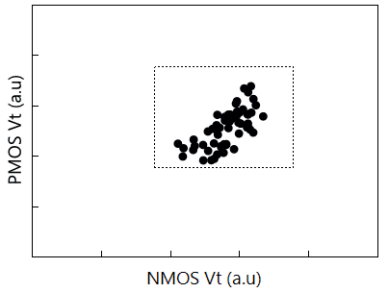

Fig. 7. Both NFET and PFET meet Vt targets with conventional WFM processing.

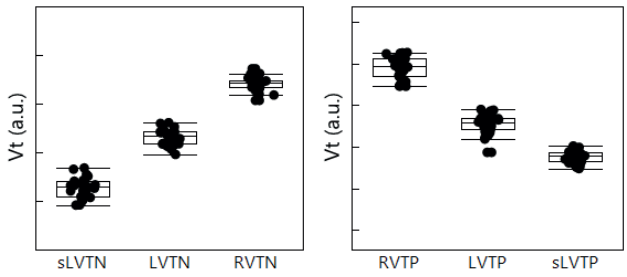

Fig. 8. Three different flavors of Vt are demonstrated with different WFMs.

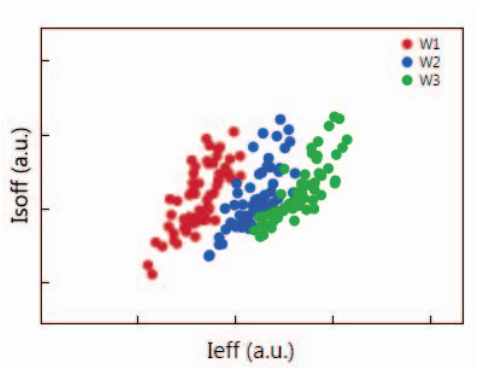

Fig. 9. DC performance modulation as a function of NS widths.

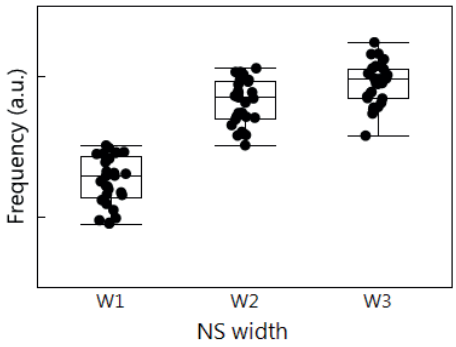

Fig. 10. Frequency modulation as a function of NS widths.

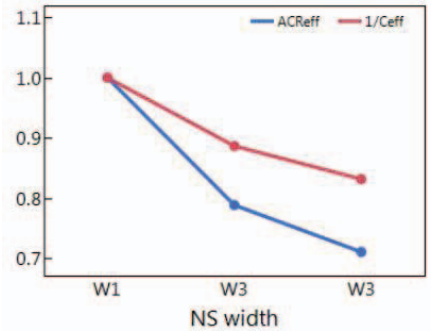

Fig. 11. ACReff and Ceff modulated by NW widths.

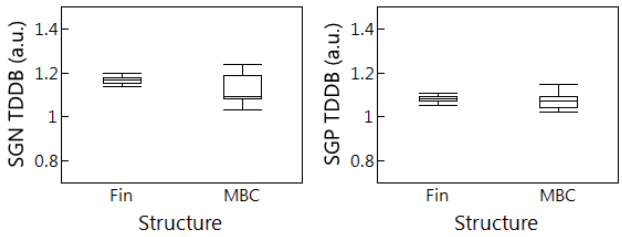

Fig. 12. Comparable TDDB characteristics of MBCFET NMOS and PMOS to those of FinFET.

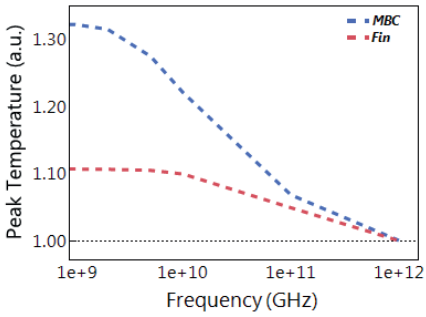

Fig. 13. Comparison of peak temperature between FinFET and MBCFET by 3D TCAD simulation.

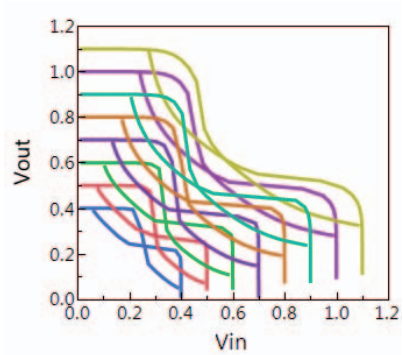

Fig. 14. SNMR characteristics of MBCFET SRAM cell. All the 6T SRAM and peripheral circuits are composed of MBCFETs

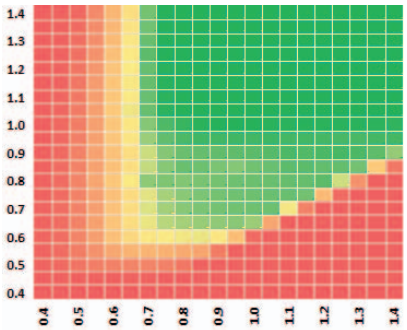

Fig. 15. Shmoo plot of high density SRAM macro having MBCFETs for SRAM cells and periphery devices.