Hybrid bonding for 3D stacked image sensors: impact of pitch shrinkage on interconnect robustness

J. Jourdon[1, 2, 3], S. Lhostis[1], S. Moreau[3], J. Chossat[1], M. Arnoux[4], C. Sart[1], Y. Henrion[1], P. Lamontagne[1], L. Arnaud[3], N. Bresson[3], V. Balan[3], C. Euvrard[3], Y. Exbrayat[3], D. Scevola[1], E. Deloffre[1], S. Mermoz[1], A. Martin[4], H. Bilgen[1],F. Andre[1], C. Charles[1], D. Bouchu[3], A. Farcy[1], S. Guillaumet[1], A. Jouve[3], H. Fremont[2], and S. Cheramy[3]
[1]STMicroelectronics, Crolles, France, email: joris.jourdon@st.com, [2]University of Bordeaux, IMS Laboratory, Talence, France, [3]CEA-LETI, Grenoble, France, [4]STMicroelectronics, Grenoble, France.

Abstract**—** Hybrid bonding is a high-density technology for 3D integration but further interconnect scaling down could jeopardize electrical and reliability performance. A study of the influence of hybrid bonding pitch shrinkage on a 3D stacked backside illuminated CMOS image sensor was performed from a process, device performance and robustness perspectives, from 8.8 µm down to 1.44 µm bonding pitches. As a result no defect related to smaller bonding pads was evidenced neither by thermal cycling nor by electromigration, thus validating fine-pitch hybrid bonding robustness and introduction for next generation image sensors.

I. Introduction

The emerging of 3D stacked BackSide Illumination (BSI) makes hybrid bonding process a key solution for CMOS Image Sensors (CIS). A high level of maturity has been recently demonstrated for a pitch of 4 µm [1], justifying the prediction of a significant growth of this technology in the field of CIS for the next years [2]. A low interconnect pitch (<2 µm) would enable to increase interconnect density and to reduce pixel size for applications such as Single Photon Avalanche Diode (SPAD). Early improvements of hybrid bonding levels scaled the pitch down to 2 µm and below for a single Cu bonding pad level architecture [3]. In the case of a dual damascene approach which enables to isolate hybrid bonding pads from last Back End of Line (BEoL) levels [4], the shrinkage of hybrid bonding could be limited as new failure mechanisms may occur.

In this paper the impact of reducing hybrid bonding pitch is investigated by comparing bonding quality, electrical and optical performance and robustness of 3D stacked BSI CIS with 8.8 µm down to 1.44 µm hybrid bonding pitches.

II. Test vehicle

The demonstrators are integrated on 300 mm wafers, stacking a BSI CIS on a digital CMOS technology node (Fig. 1). Wafers are connected thanks to Hybrid Bonding Metal pads (HBM) and Hybrid Bonding Vias (HBV) processed by a dual damascene architecture. The face-to-face hybrid bonding process is performed on an EVG GEMINI®FB system followed by a bonding annealing at 400 °C to strengthen the bonding interface and stabilize Cu microstructure.

The demonstrators consist in a BSI-CIS to detect the impact of HBM size on sensor performance and passive test structures designed for in-depth electrical and robustness studies of hybrid bonding levels. All these test vehicles are integrated with different hybrid bonding pitches (8.8, 7.2 and 1.44 µm). The other BEoL levels left unchanged enable to distinguish the physical HBM pitch from the electrical HBM pitch depending on how HBM are connected to BEoL (Fig. 1). FEM simulations of daisy chains identify HBV as the most resistive part of interconnects (Fig. 2a). Daisy chains with various geometries were designed as test structures to minimize or maximize the current density (Fig. 2b).

III. Process validation

A. Topography mitigation at wafer level

Hybrid bonding relies on global flatness and local topography. Finite Element Method (FEM) simulations of Cu-Cu interface closure during annealing were carried out for HBM with a given dishing profile (Fig. 3). An overall decrease of the contact area is observed with HBM width reduction at a given dishing depth value in agreement with the literature [5-6]. Dishing compensation thanks to thermal expansion is thus a critical parameter. The dishing has to be uniform and light enough to enable the contact of HBM during the post-bonding annealing. Controlled planarization process is thus required as dishing variation is affected by Cu pad width [7].

A dedicated CMP process was developed in response to obtain identical dishing from 1.44 to 8.8 µm HBM pitch on the same wafer, as confirmed by Atomic Force Microscopy (AFM) measurements (Fig. 4). The process also compensates the topography induced by prior BEoL levels. Scanning Acoustic Microscopy (SAM) performed after bonding annealing reveals no unbonded zone within the 50 µm limit of resolution of the SAM. Backside process steps and final annealing at 400 °C were completed with no defectivity.

B. Cu-Cu interface closure

Cu-Cu bonding relies on thermal expansion of Cu and on atoms diffusion at bonding interface. This mechanism is enhanced by a high density of grain boundaries. Electron BackScatter Diffraction (EBSD) indicates that the mean grain size decreases from 1.1 to 0.3 µm, respectively for 4.4 and 0.5 µm HBM widths. TEM pictures (Fig. 5) evidence a good closing of the Cu-Cu interface whatever the pitch. In both cases, bonding voids, caused by Cu oxide demixion and vacancies migration [4], have similar sizes. A good bonding quality is also obtained for smaller Cu grains.

Bonding quality is assessed thanks to resistance measurements of daisy chains with 100 or 30,000 links (respectively DC100 and DC30k). Each test structure reaches 100 % yield whatever HBM pitch (Fig. 6). Results are in agreement with FEM calculations indicating a negligible effect of interface resistance and of Cu microstructure on daisy chains resistance. Interconnects are simulated by FEM for different HBV diameters measured after the lithography step. According to extracted resistances, the dispersion evidenced at wafer edges is linked to HBV diameter variations (Fig. 7). The shift between experimental and theoretical values is attributed to process variations, such as HBV conical shape and diameter enlargement due to over-etching (Fig. 8).

C. Sensitivity to bonding overlay

Bonding misalignment reduces HBM contact area and brings interconnects laterally closer, potentially leading to resistance and capacitance increases. Full wafer overlay measurement gives a mean value of 200 nm (±3σ). The Cu-Cu contact area decreases faster for small HBM but the resistance of 1.4 µm pitch interconnects is demonstrated to be insensitive to misalignment (Fig. 9). FEM parametrical study of resistance variations as a function of misalignment indicates an increase lower than 1 % for a J_{max}-1.44 µm interconnect (Fig. 2) at maximum overlay (200 nm) (Fig. 10). This variation is not measurable as long as it does not overcome resistance standard deviation. Considering the dual damascene integration, overlay is not expected to become critical for fine pitch until HBM contact area reaches HBV section. For a 200 nm misalignment this critical pitch is estimated at 0.8 µm.

The capacitance measured on 3D combs with a redundant HBV and redundant HBM is 12 ± 1 pF. Simulation of 3D combs shows that a 200 nm overlay increases the capacitance by 0.2 % (Fig. 11). This increase is twice higher for combs containing dummies but remains negligible. The 7.2 µm electrical HBM pitch is therefore too large for the capacitance to be significant.

IV. IMAGE SENSOR DEMONSTRATOR

The influence of hybrid bonding pitch on optical performance is evaluated using a 14 Mpixels BSI imager with 1.5 µm pixel pitch. The top die contains exclusively the array of pixels while the bottom die has all analog blocks: Analog-to-Digital Converter (ADC), column decoder and control. It also comprises a state of the art High Dynamic Range (HDR) image signal processing pipeline able to sustain up to 600 Mpixels/s and a large cluster of computer vision processing engines including a hexa-core CPU. Two versions of the 3D stacked sensor are studied comparing hybrid bonding pitches of 8.8 µm and 1.44 µm with respectively redundant HBV or redundant HBM. The integrity of the whole stack is validated for both pitches according to TEM cross sections (Fig. 12).

The standard optical performance such as sensibility and Photo Response Non-Uniformity (PNRU) are measured at wafer level (Fig. 13). Cumulative distributions have a low dispersion and are similar from one pitch to another. After packaging and mounting in a specific set-up, the optical properties of the 3D BSI-CIS for 8.8 or 1.44 µm HBM pitch are tested based on the parameters described in Table 1 and are within the specifications. Identical values were obtained for both HBM widths. Both sensors can take pictures (Fig. 14), validating the use of fine pitch for 3D stacked CIS.

V. ROBUSTNESS OF BONDING INTERFACE

D. Thermal cycling

Since the bonding interface is made of Cu and SiO_2 with different Coefficients of Thermal Expansion (CTE), thermo-mechanical stresses can occur at ambient temperature or due to Joule heating. 2D FEM is carried out to localize the critical zones in an array of HBM. Fig. 15 shows that von Mises stress is higher in HBM corners and triple points formed by the bonding interface and HBM walls. At smaller pitch oxide spaces are not wide enough to release stress, so delamination is more inclined to occur at the Cu/SiO_2 bonding interface for the 1.44 µm pitch.

In order to evaluate this risk of delamination, thermal cycling tests at wafer level are conducted at -65/+150 °C and -55/+150 °C, 500 cycles, respectively for HBM pitches 7.2 and 1.44 µm. The resistance of the daisy chains is measured by 4-wire sensing before and after the test. All test structures remain fully functional after test and resistance variation is lower than 1 % (Fig. 16). Despite a higher stress pointed out by simulation for the smallest pitch, the bonding interface is robust.

E. Electromigration

Pitch reduction potentially associated with ever-increasing current densities [8] rekindles discussions about electromigration (EM) immunity of hybrid bonding level. For the 7.2 µm hybrid bonding pitch, EM-related failures localized in the BEoL confirm the previous studies on a demonstrator containing only daisy chains [9]. No specific hybrid bonding-related failure occurs with additional metal levels. For a BEoL made of four top metal lines and seven bottom metal lines, the bonding interface is immune (Fig. 17). The Black's parameters are typical ones of Cu interconnects [10]. EM test are conducted (350 °C, 30 mA, failure criterion: 10 % of electrical resistance increase) on DC100 (Fig. 18) with either J_{min}-7.2µm or J_{min}-1.44µm interconnects described on Fig. 2. The probability plots are similar and suggest the same failure mechanisms for both pitches.

CONCLUSION

The transition of hybrid bonding pitch from 8.8 to 1.44 µm is made possible thanks to the development of a new surface preparation process enabling flatness and uniform dishing. The physical characterizations and 100 % yield extracted on 30k daisy chains evidence the quality of this fine-pitch bonding. The electrical resistance was demonstrated to be insensitive to bonding overlay as long as the contact area remains larger than HBV section. The electrical and optical tests of a full BSI CIS demonstrate no fine-pitch hybrid bonding impact on performance. Aging tests point out no failure related to the HBM pitch shrinkage, thus confirming the dual damascene integration choice. These results evidence the robustness of dual damascene hybrid bonding down to 1.44 µm pitch.

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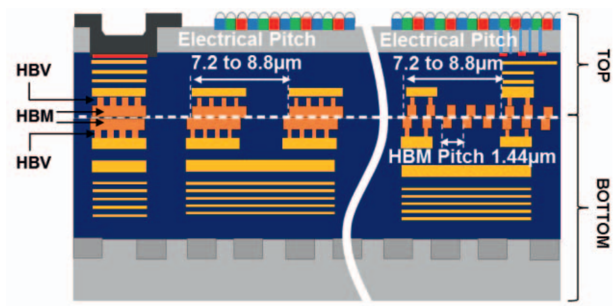

Fig. 1. Schematic cross section of the image sensor (top) stacked on advanced CMOS (bottom). The connection is achieved by interconnects with a hybrid bonding pitch of 8.8, 7.2 (left) or 1.44 µm (right). Electrical pitch is kept identical for a same set of electrical structures ranging from 7.2 to 8.8 µm.

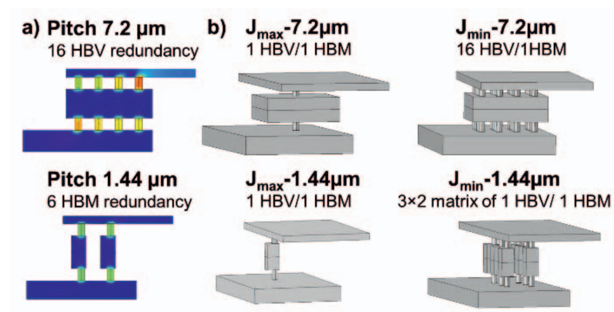

Fig. 2. (a) The current density extracted from FEM simulations is higher in HBV. (b) Schema of single interconnects. The current density can be maximized (J_{max}) or minimized (J_{min}) by varying width of HBM (7.2 or 1.44 µm) and redundancy (HBV for 7.2µm pitch or HBM for 1.44µm pitch).

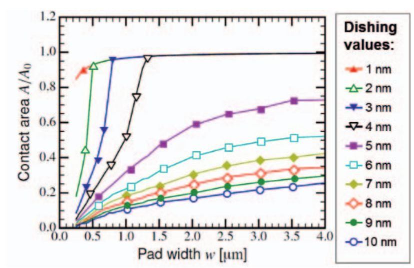

Fig. 3. Thermo-mechanical finite element simulations of dished Cu-Cu interface closure during annealing at 400 °C for varying HBM width and dishing depth.

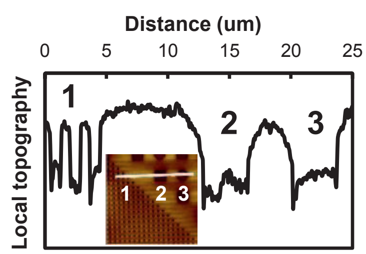

Fig. 4. AFM 2D scan on 0.72 and 3.6 µm-wide HBM with profile scan along white line showing identical dishing depth for both pitches.

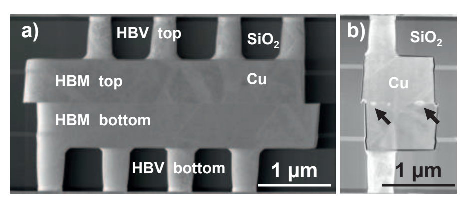

Fig. 5. TEM image cross section of (a) 4.4 and (b) 0.72 µm-wide HBM. Bonding voids (black arrows) are small compared to the large well-bonded Cu/Cu interface.

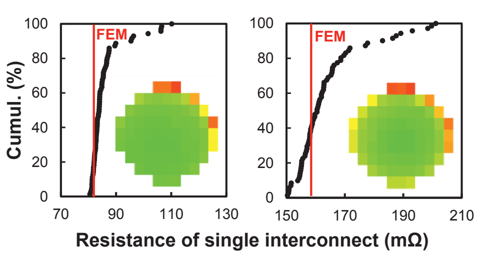

Fig. 6. Cumulative distributions of single interconnect resistances and mapping for DC30k (left) J_{min}-7.2µm and (right) J_{min}-1.44µm.

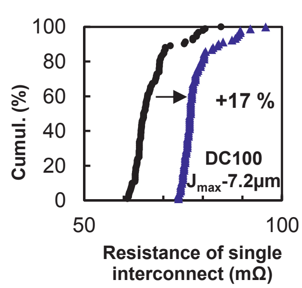

Fig. 7. Cumulative distributions of experimental (black circles) and FEM (blue triangles) resistance based on HBV diameters measured during HBV lithography step.

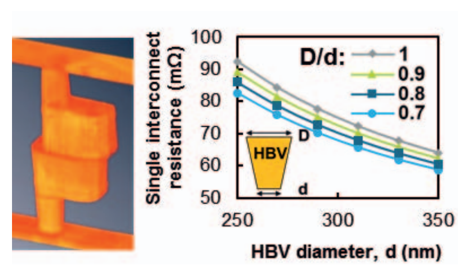

Fig. 8. FIB-SEM 3D reconstruction on J_{min}-1.44µm showing HBV conical shape (left). FEM simulation showing the resistance dependence to the HBV shape and diameter of HBV on J_{max}-7.2µm. (right).

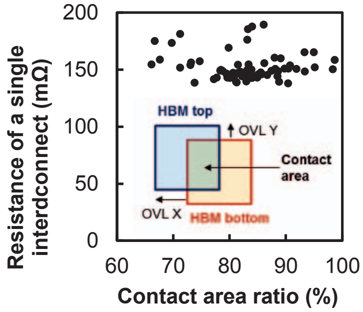

Fig. 9. Resistance of DC100 J_{min}-1.44µm as a function of contact area deduced from overlay (OVL) measurements.

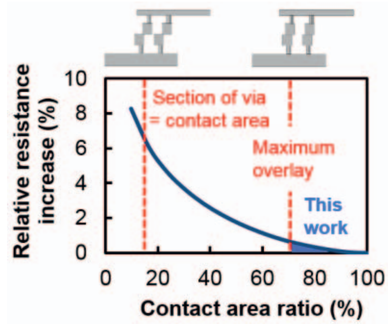

Fig. 10. FEM calculation of the resistance increase with contact area reduction (DC100 J_{min}-1.44µm).

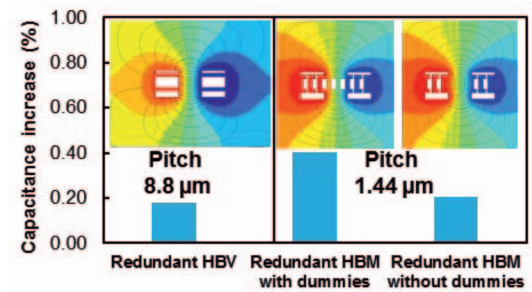

Fig. 11. FEM simulations of capacitance increase due to a 200 nm misalignment for various combs designs. Black lines represent the electric field between interconnect at a 1 V polarization.

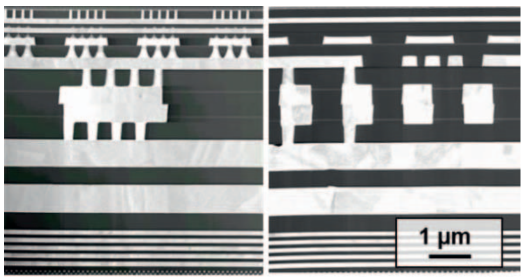

Fig. 12. TEM cross section of 3D stacked image sensor with 8.8 (left) and 1.44 µm-pitch (right). All BEoL levels are visible.

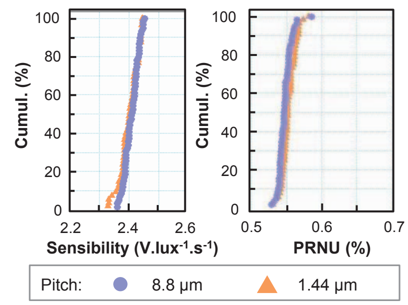

Fig. 13. Cumulative distributions of the sensibility and PRNU of 3D image sensor.

Optical Tests
Dark and light mean
Dark dynamic range
Dark & light defectivity
Dark defect line row
Dark defect line col
Light signal-to-noise ratio
Light fixed pattern noise
Light PRNU

Table 1. Electrical and optical parameters tested for 3D CIS with HBM pitches of 8.8 and 1.44 µm.

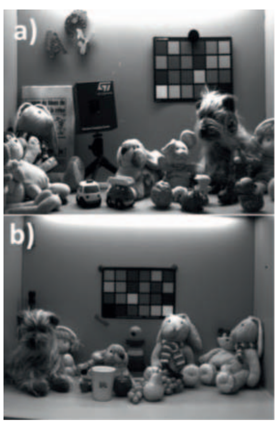

Fig. 14. Pictures taken with 3D stacked image sensor with hybrid bonding pitch (a) 8.8 and (b) 1.4 µm.

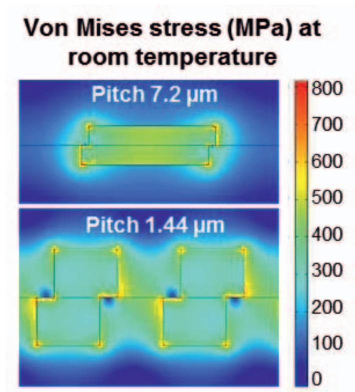

Fig. 15. 2D FEM simulations of thermo-mechanical stress due to CTE mismatch in an array of HBM.

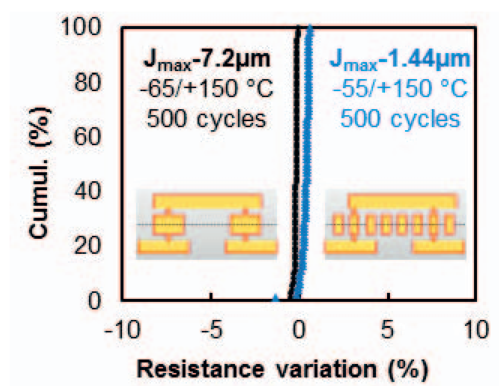

Fig. 16. Distribution of DC100 resistance variation after thermal cycling. J_{max}-1.72µm (black round) and J_{max}-1.44µm (blue triangle).

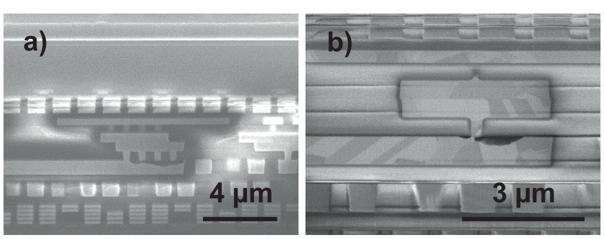

Fig. 17. Post-mortem cross-section of DC100 (a) J_{min}-7.2µm after an EM test at 350 °C/30 mA and (b) J_{max}-7.2µm after an EM test at 350 °C and 5 mA. Electrons flow from the top to the bottom of the test structure.

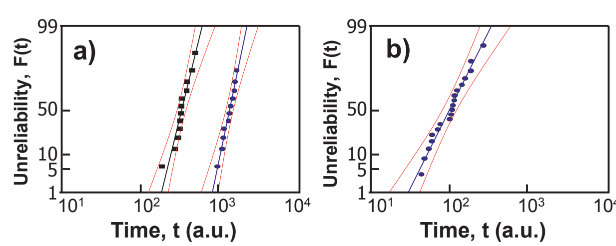

Fig. 18. Probability plot (lognormal distribution) for DC100 after EM tests at 350 °C (left) J_{max}-7.2µm with 20 mA (blue circle) or 30 mA (black square), and (right) J_{min}-1.44µm enduring an electromigration test at 350 °C and 30 mA. Confidence bounds: 90 %.