16.4 A 0.5-to-2.5GHz Multi-Output Fractional Frequency Synthesizer with 90fs Jitter and -106dBc Spurious Tones Based on Digital Spur Cancellation

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There is need for a low-power, compact, means of generating multiple, low-jitter, spectrally pure, clock signals at different frequencies using a single reference oscillator, both in wireline and wireless applications, owing to circuit size, cost, and complexity considerations. PLL-based frequency synthesis – analog or digital – can achieve very low jitter and spur levels, but the VCO size and/or power consumption concerns preclude its duplication for multiple on-chip clock generators [1,2]. Open-loop digital methods based on digital-to-phase or digital-to-time converters (DPCs) are compact and employ no power-hungry oscillators, but their circuit errors and mismatches result in strong spurious tones.

This paper describes a purely digital spur-cancellation technique that uses a bang-bang phase detector (BBPD) and a special noisy, but mostly spur-free, auxiliary clock generator to extract spurious tones precisely and digitally correct for them. When applied to a DPC-based frequency synthesizer, this technique achieves <90fs integrated jitter and spurious tones of <–106dBc for a 2.48GHz carrier.

Figure 16.4.1 shows a block diagram of the multi-clock generator based on the proposed technique. At the heart of each proposed clock generator are two 12b DPCs: *main* and *auxiliary*. The main DPC performs fractional division by $(N+\alpha)$ upon octant phases of frequency f_0 that are derived from an external low-noise PLL. A 2nd-order digital delta-sigma modulator (DDSM) and a phase-select-logic (PSL) block achieve the fractional division as described in Fig. 16.4.2. Even with a high-resolution DPC, inevitable errors in the DPC result in strong spurious tones. The auxiliary DPC performs the same fractional division, but uses a "spur-free" PSL that theoretically guarantees spur-free fractional division, at the expense of excessive phase noise. The BBPD extracts the instantaneous phase difference between divided versions of the low-noise main-DPC output and the noisy, but mostly spur-free, auxiliary-DPC output, both of which have the same frequency, $f_0/(N+\alpha)$. The one-bit BBPD output stream contains the spurious tones in the main DPC output along with the phase noise of the auxiliary DPC output. Digital comb filters with appropriately chosen center frequencies suppress the phase noise and extract just the spurs, including their harmonics [2]. The resultant phase error, *ph_err[n]*, is compensated for the effective bang-bang PD gain, β, (described below), converted to an effective frequency error, *freq_err[n]*, by digital differentiation, negated, and fed as a frequency correction signal to the main-DPC input fractional value, α. The BBPD, the DPCs, the DDSM, and the entire digital spur-cancellation logic run synchronized with the output clock, at a frequency of $f_{dig} = f_0/(N+\alpha)/4$.

Note that the technique assumes approximate knowledge of the spur frequencies. While fractional-spur frequencies can be predicted *a priori*, non-fractional-spur frequencies may have to be determined using frequency estimation techniques. Besides, in an industrial setting, they are generally known from preliminary lab measurements.

Figure 16.4.2 illustrates how fractional division is performed using a DPC and PSL and highlights the specific modifications of the "spur-free" PSL. As shown in Fig. 16.4.1, the fractional value, α, is quantized to a 12b sequence, v[n], using a 2nd-order DDSM. Once every cycle of f_{dig}, v[n] is integrated to generate the next 12b DPC-control code, e[n]. The 3 MSBs of e[n] choose an octant, whereas the 9 LSBs control an analog waveform interpolator, whose output frequency is divided by N. The generation of e[n] can be modeled as the 1st-order DDSM shown, where the feedback represents wrapping around a cycle of f_0. Consequently, adjacent low-to-high transitions of the DPC output are separated by $(N+v[n]/2^{12})/f_0$ seconds realizing fractional division by $(N+\alpha)$. The "spur-free" phase-select logic is different in one key respect. Large highpass-shaped phase dither (almost 0.5 cycles of f_0), generated using a one-bit random sequence $\eta[n]$ filtered by a highpass dither filter, G[z], is added to the integrated v[n]. It is theoretically established [4] that such filtered dither prevents memoryless DPC errors in the auxiliary DPC from causing spurious tones. Simulated baseband spectra shown in the figure confirm the same. Note that the auxiliary DPC is not useful for fractional synthesis because of the large amount of dither.

Figure 16.4.3 illustrates the linearized operation of the BBPD. This highly nonlinear block quantizes its input phase difference to just one bit. However, the large phase noise in its inputs renders its operation linear, modeled by a gain, β, and additive quantization noise, provided its inputs have a non-zero average phase difference. As shown in Fig. 16.4.1, any non-zero phase difference is estimated and fed back to the main DPC. This shifts its output phase just enough to remove the non-zero phase difference. In other words, it aligns the BBPD input edges on average. Furthermore, digital LMS algorithms, shown in Fig. 16.4.1, estimate the effective BBPD gain, β, and accordingly compensate the spur-cancellation path gain. Since the BBPD gain, β, can depend on the spurious-tone frequency location, each spur-cancellation path employs a dedicated gain-estimation LMS loop, as shown in Fig. 16.4.1.

A prototype IC was designed in UMC 28nm CMOS to demonstrate the proposed spur-cancellation technique. Two clock generators were designed to work in parallel. The 12b DPCs, frequency dividers, BBPD, and clock buffers were the only analog circuit blocks. Provisions were made to externally couple spurs into the buffers on the main-DPC output for measurement purposes, as shown in Fig. 16.4.1. The DPCs can operate up to 3GHz at nominal V_{DD} = 0.9V using standard mixed-signal circuit techniques. The rest of the circuitry was purely digital and was designed using a synthesis and place-and-route flow. A die micrograph is shown in Fig. 16.4.7. The core circuit consumes 2.6mW with area of 0.15mm^2.

Phase noise, jitter, and spurious-tone measurements were performed without and with spur-cancellation technique enabled on 3 different chips for multiple settings of α. Figure 16.4.4 shows measured power spectra for 2.48GHz carrier (for α = 1/40) without and with the spur-cancellation technique enabled. As is evident, >30dB spur cancellation is achieved, with measured spur levels limited only by the instrument noise floor. Similar results were obtained on all 3 chips measured. Note that the technique cancels both fractional spurs caused by the DPC and other circuit errors and "external spurs" introduced into the main-DPC output via intentional coupling into the supply of down-stream buffers. The external spurs are an attempt to emulate non-fractional spurs that are commonly observed in clock-generation circuits usually via supply, bias, or substrate coupling. It is important to note that similar spur cancellation was observed even as the fractional spur location was swept by using different values of α. Figure 16.4.5 shows example measured phase-noise plots for the same carrier frequency. As can be seen, 87fs rms jitter, integrated from 10kHz to 40MHz bandwidth was observed. Over the three measured chips and multiple carrier frequencies, the worst-case integrated jitter of 90fs was observed.

Figure 16.4.6 compares the performance achieved by proposed technique with recent prior art. As is evident, the technique achieves at least a 29dB-lower spurious tone and 8× lower integrated rms jitter for lower power consumption, *albeit* at a finer technology node.

Acknowledgement:
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[4] S. Pamarti and S. Delshadpour, "Spur Elimination Technique for Phase Interpolation-Based Fractional-N PLLs," *IEEE TCAS-I*, vol. 65, no. 6, pp. 1639-1647, June 2008.

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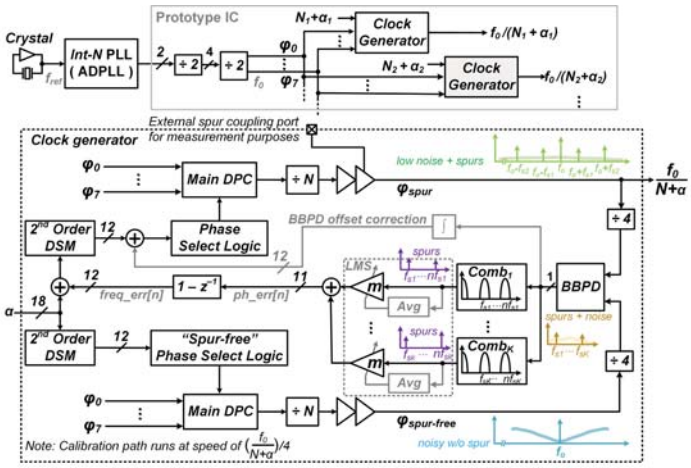


Figure 16.4.1: Proposed multi-output fractional frequency synthesizer based on digital spur cancellation.

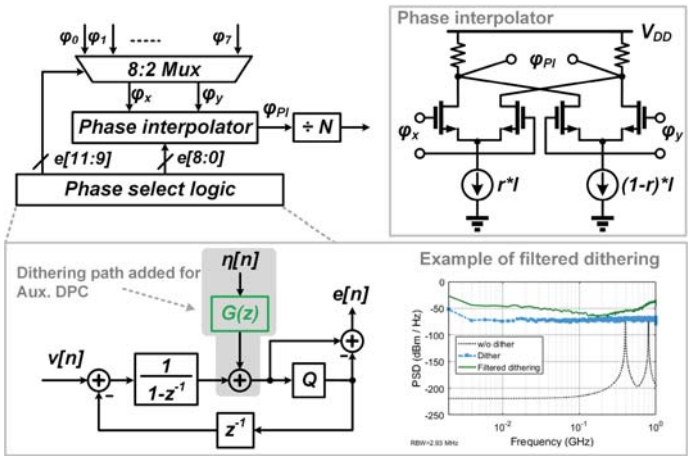


Figure 16.4.2: Implementation of 12b phase-interpolator-based DPCs. For the auxiliary DPC, a shaped filtering path is added to the phase-select logic.

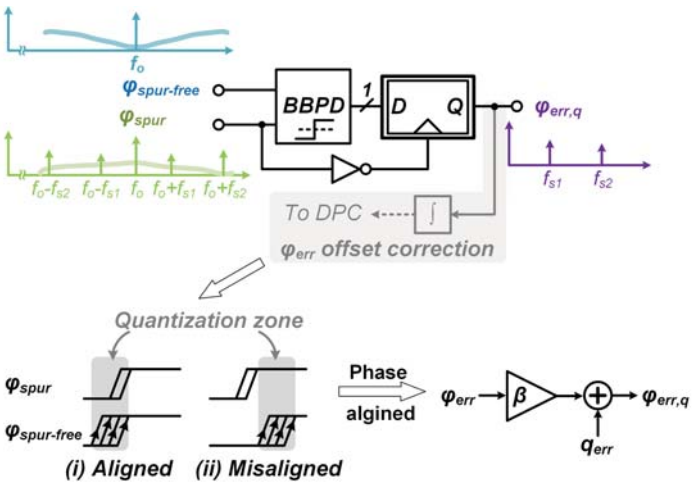


Figure 16.4.3: Linearized operation of a bang-bang PD for spurious phase-error quantization.

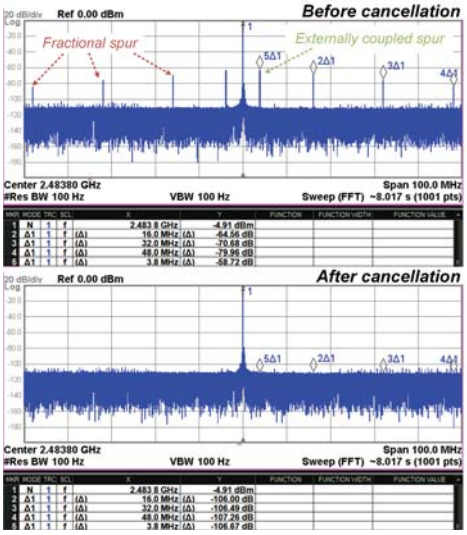


Figure 16.4.4: Measured cancellation of fractional spur and externally coupled spur.

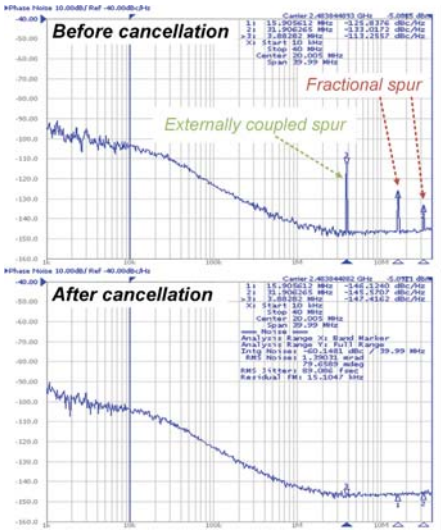
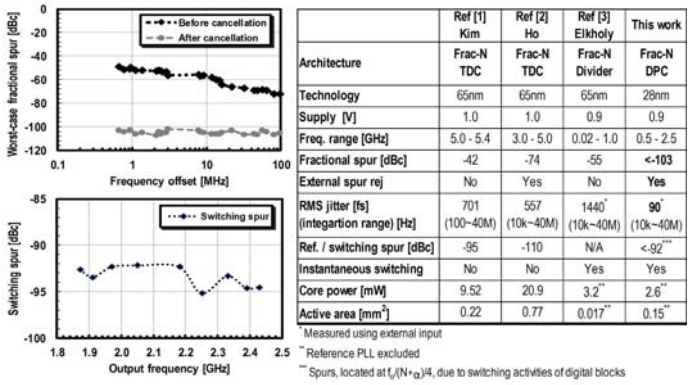


Figure 16.4.5: Measured phase-noise performance with and without spur cancellation.



	Ref [1] Kim	Ref [2] Ho	Ref [3] Elkholy	This work
Architecture	Frac-N TDC	Frac-N TDC	Frac-N Divider	Frac-N DPC
Technology	65nm	65nm	65nm	28nm
Supply [V]	1.0	1.0	0.9	0.9
Freq. range [GHz]	5.0 - 5.4	3.0 - 5.0	0.02 - 1.0	0.5 - 2.5
Fractional spur [dBc]	-42	-74	-55	<-103
External spur rej	No	Yes	No	Yes
RMS jitter [fs] (integartion range) [Hz]	701 (100~40M)	557 (10k~40M)	1440* (10k~40M)	90* (10k~40M)
Ref. / switching spur [dBc]	-95	-110	N/A	<-92***
Instantaneous switching	No	No	Yes	Yes
Core power [mW]	9.52	20.9	3.2**	2.6**
Active area [mm^2]	0.22	0.77	0.017**	0.15**

* Measured using external input
** Reference PLL excluded
*** Spurs, located at $f_o/(N+\alpha)/4$, due to switching activities of digital blocks

Figure 16.4.6: Performance summary and comparison with prior art.

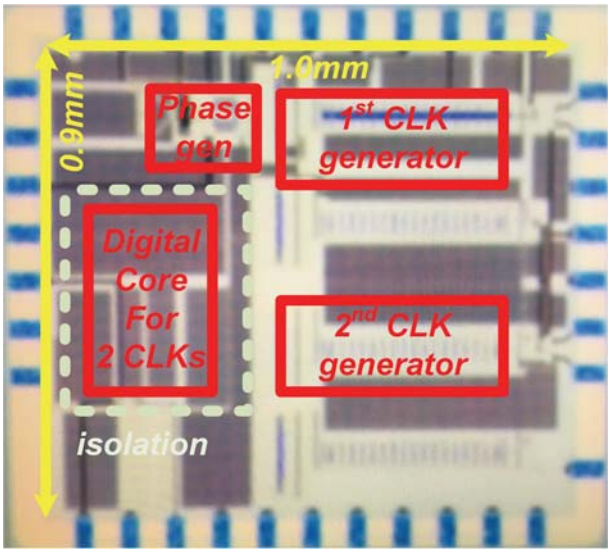


Figure 16.4.7: Die micrograph.

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