A 2.2 GHz CMOS VCO with Inductive Degeneration Noise Suppression

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Abstract

A 1.4 V, 9 mA monolithic LC-tank voltage-controlled oscillator (VCO) fabricated in a standard 0.35μm CMOS process is presented. The VCO is tunable between 2.0 GHz and 2.37 GHz, and displays a phase noise between -140 dBc/Hz and -138 dBc/Hz at a 3 MHz offset frequency across the whole tuning range. This low phase noise is achieved through the use of an on-chip LC filter and an off-chip low frequency inductor, which totally remove the noise of the tail current source. The phase noise improvement due to the off-chip inductor is between 2 dB and 6 dB, increasing with higher oscillation frequencies.

1. Introduction

Wireless applications typically require VCO's having low power consumption, low phase noise, small size, and low cost. The size and cost requirements make an integrated oscillator in a standard CMOS process with an on-chip resonance LC-tank a good choice. The attainable quality factor of the resonance tank is, however, quite limited in a standard CMOS process, which makes the oscillator design a real challenge. New approaches must be found to push the oscillator performance towards the fundamental limits, especially when the phase noise behavior is considered.

The mechanisms of phase noise generation in oscillators have been the targets of important research efforts. Recently, an expression quantitatively accounting for the phase noise of the popular tail current biased LC oscillator has been given in [1] (with the simplifying assumption that the current in the switching transistors is a square wave). On a more heuristic level, the access to simulators (such as spectreRF) capable of accurate noise analysis in very non-linear circuits such as oscillators and mixers has proven invaluable. From both simulation results and the theoretical achievements in [1], the previously neglected role of the tail current transistor as one of the main phase noise sources (indeed, often the major one) in differential LC oscillators has become apparent. The task is therefore to try to prevent the noise (both white and 1/f) of the tail current source from becoming phase noise.

The work presented in [2] shows that an LC low-pass filter can prevent the noise current at twice the oscillation frequency from reaching the switch transistor pair and being down-converted into phase noise.

The present paper shows how to avoid the low frequency tail current noise being up-converted into phase noise. In order to filter off noise at low frequencies, at least one large reactive component is needed. This component, in our case an inductor, must be discrete due to its size. The inductor is placed between the source terminal of the tail transistor and ground, and thereby acts as an inductive source degeneration. It will suppress the noise significantly at frequencies where the inductor impedance is larger than $1/g_m$, g_m being the transconductance of the tail transistor. A suppression over the (offset) frequencies of interest in most wireless systems is readily achieved using standard off-the-shelf inductors.

To demonstrate the proposed approach, an oscillator was designed in a standard 0.35μm CMOS process with three metal layers. Accumulation-mode MOS varactors were used to tune the oscillation frequency between 2.00 GHz and 2.37 GHz. The off-chip inductor was used together with the on-chip LC filter proposed in [2]. Consuming 9 mA from a 1.4 V power supply, the oscillator meets the demanding phase noise requirements of GSM-1800 over the whole tuning range.

2. Phase noise issues

If filtering techniques are not applied, the tail transistor (M_{src} in Fig. 1) contributes the majority of the phase noise in a differential CMOS LC oscillator. It does so through two different mechanisms: high frequency noise down-conversion, and low frequency noise up-conversion. High frequency tail current noise, mostly around twice the carrier frequency, is mixed down into phase noise around the carrier frequency [1]. This high frequency noise can be filtered out by an on-chip LC filter [2] (L_{flt} and C_{flt} in Fig. 1).

In the second mechanism, low frequency bias current noise is up-converted to amplitude noise around the carrier [1]. The amplitude noise is then converted to phase noise by the non-linear capacitance of the varactor and of the switch transistors.

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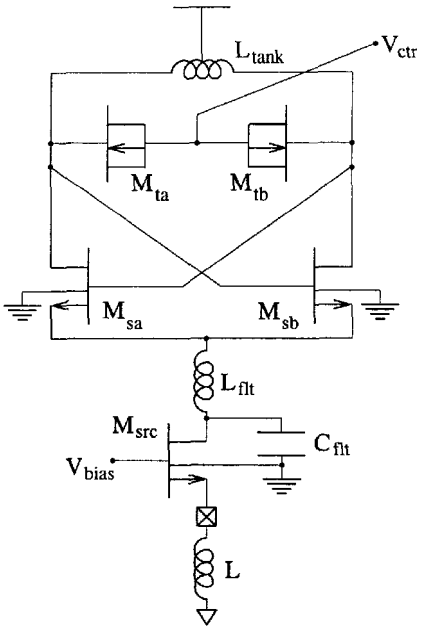

Figure 1. Schematic view of the VCO.

The MOS varactor has a strong tuning-voltage dependent nonlinearity, resulting in a large AM to FM conversion at high tuning voltages (frequencies). The phase noise will therefore have a large variation across the tuning range. This was dealt with in [2] by using a small varactor, resulting in a low AM to FM conversion. To achieve a large tuning range and be able to account for process variations, the small varactor was used together with an array of switched capacitors. In this work we present another approach, that prevents also the low frequency noise from reaching the switch transistors. Thus, the varactor nonlinearity is no longer critical, and any varactor can be used, avoiding the increased complexity of switched tuning. To filter off the low frequency noise, however, at least one large reactive component must be used. This component, in our case an inductor, must be off-chip.

The off-chip inductor is placed between the source of the tail transistor M_{src} and ground (inductance L in Fig. 1). The inductor degenerates the transistor, and the power of the noise current is reduced by the factor $|1 + j\, g_m\, \omega\, L|^2$, where g_m is the transconductance of M_{src}. The technique suppresses the noise in a frequency band which is limited upwards by the parasitic parallel capacitance of the inductor, and downwards by the inductance value (the larger the inductance, the lower the frequency limit). For a g_m of 50 mS, and an L of at least 30 μH, the noise reduction begins at about 100 kHz. Thus, standard off-the-shelf inductors with values in the range 10 μH-100 μH provide noise suppression over the offset frequencies of interest in GSM. The inductance value, the quality factor and the self-resonance frequency (10 MHz or higher for the inductors tested) are not critical; furthermore, unlike an external resonator, the off-chip inductor carries no high frequency signals, so the package parasitics and PCB layout are uncritical as well.

Table 1. Dimensions and values of the on-chip VCO components.

Transistors	
M_{src}	2000μm × 1.0μm
M_{sa}, M_{sb}	500μm × 0.35μm
M_{ta}, M_{tb}	1000μm × 0.35μm
Reactors	
L_{tank}	≈ 2.3 nH
Q of the LC-tank	≈ 9 at 2.2 GHz
L_{flt}	≈ 3.0 nH
C_{flt}	10 pF
Chip dimensions	1100μm × 850μm

An alternative method to combat low frequency noise upconversion is to reduce the cut-off frequency of the low-pass LC filter, thereby suppressing the low frequency and high frequency noise at the same time. This can be done by placing a large off-chip capacitance in parallel with the on-chip capacitance C_{flt}. This technique, however, is less robust than the inductive degeneration, since it creates a low impedance path through the large capacitance to ground for the low frequency noise of the switching transistors, which may well counteract the beneficial effects on the tail current noise (according to simulations). However, a new series of measurements will hopefully assess the relative merits of the two techniques.

VCO design. The scheme of the implemented VCO (a classical differential LC-tank topology) is shown in Fig. 1. The large inductor L is a discrete off-chip component, as explained previously. Since the quality factor of on-chip inductors are typically highest for small inductances, a 2.3 nH inductor was used for L_{tank}. To further maximize the quality factor, the three metal layers available in the process were used in parallel, and the octagonal differential inductor topology was adopted. Measurements give a quality factor for the whole LC-tank of about nine at 2.2 GHz.

The quality factor of the on-chip LC filter, on the other hand, is not critical, and physically smaller inductors than the one used in this work may be employed (the small library available to us contains only Q-optimized inductors). Table 1 shows dimensions and values for all on-chip VCO components.

2.1. Simulation results

Simulations have been performed with a 1.4 V power supply voltage and a 9 mA supply current (the same values were adopted during the actual measurements). The simulator used was spectreRF with the bsim3v3 MOS transistor model (with noimod = 2, the noise factor γ of the switch transistors was about 0.75). The simulated tuning range of the VCO (2.00 GHz-2.30GHz) is somewhat smaller than the measured one (2.00GHz-2.37GHz); however, due to the lack of a dedicated simulation model for the accumulation-mode MOS var-

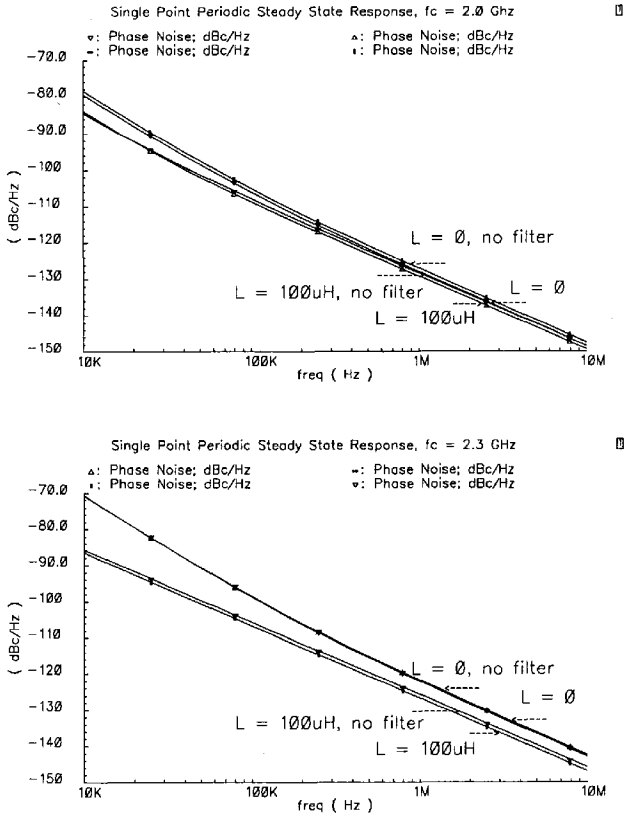

Figure 2. Simulations of the phase noise of the VCO at 2.0 GHz (top) and 2.30 GHz carrier frequency.

actor, the degree of matching between simulations and measurements is in fact very high.

Fig. 2 shows the simulated phase noise displayed by the VCO at the maximum and minimum oscillation frequencies. It should be noticed that these simulations yield worst-case results, since spectreRF does not distinguish phase noise from amplitude noise. In order to assess the benefits of filtering the tail current noise, four different simulations have been performed for each frequency. One simulation is for the VCO with neither on-chip LC filter, nor off-chip inductor (case "a" in Table 2). This is nothing but the standard VCO implementation. Case "b" is the VCO with on-chip filter, but no off-chip inductor; in case "c" there is no on-chip filter, but an off-chip inductor of 100μH. Finally, case "d" is when both on-chip filter and off-chip inductor are used. Fig. 2 clearly shows that the advantages yielded by the inductive degeneration increase with lower offset frequencies, where the 1/f noise of the tail transistor totally dominates the phase noise. At higher offset frequencies the effect of the inductive degeneration is more prominent at higher carrier frequencies, since the MOS varactor is then more nonlinear. Table 2 shows in detail the phase noise contributions of the different components of the VCO, at the offset

Table 2. Simulated phase noise of the VCO at 3 MHz offset frequency for the minimum and maximum carrier frequency. The four simulations cases are: a) L= 0μH, on-chip filter=no; b) L= 0μH, on-chip filter=yes; c) L= 100μH, on-chip filter=no; d) L= 100μH, on-chip filter=yes.

f_c = 2.0 GHz	a	b	c	d
Phase noise (dBc/Hz)	-136.3	-137.3	-138.3	-139.3
% R_{tank}	33.67	40.56	49.62	62.19
% M_{sa}+M_{sb} (white)	20.51	21.61	30.32	33.32
% M_{sa}+M_{sb} (1/f)	0.45	0.53	0.62	0.75
% M_{src} (white)	40.58	31.49	17.14	0.03
% M_{src} (1/f)	3.16	3.41	<0.01	<0.01
% Other sources	1.63	2.40	2.30	3.71
f_c = 2.30 GHz	a	b	c	d
Phase noise (dBc/Hz)	-130.8	-131.4	-134.9	-136.2
% R_{tank}	20.73	23.02	53.76	69.55
% M_{sa}+M_{sb} (white)	11.20	8.96	28.66	26.80
% M_{sa}+M_{sb} (1/f)	0.02	0.02	0.04	0.04
% M_{src} (white)	61.37	60.32	15.60	0.06
% M_{src} (1/f)	5.98	6.48	<0.01	<0.01
% Other sources	0.70	1.20	1.94	3.55

frequency of 3 MHz, for the four different simulation cases. At 2.0 GHz, the overall phase noise reduction is 3 dB, of which 2 dB are due to the inductive degeneration and 1 dB is due to the on-chip LC filter. At 2.3 GHz, however, the overall phase noise reduction is as high as 5.4 dB, of which 1.3 dB are given by the on-chip filter. Even more interesting is that the combination of on-chip filtering and off-chip inductive degeneration completely removes the tail current noise, which is otherwise the single largest phase noise source, as is manifested in Table 2. When the tail current noise is removed, the phase noise is mostly generated by the resonator tank itself, the switch transistor pair contributing roughly half as much (at high enough offset frequencies). Thus, the noise factor of the VCO is about 1.5 (between 1.43 and 1.60 according to Table 2).

3. Measurements results

The VCO was fabricated in a standard 0.35μm CMOS process (three metal layers with resistivity 70 mΩ/□, 70 mΩ/□, and 40 mΩ/□, respectively; gate resistivity 9 Ω/□; substrate resistivity 5 Ω·cm). A die photograph of the VCO is shown in Fig. 3. All measurements presented here were performed with a 1.4 V power supply voltage and a 9 mA supply current. The frequency of oscillation could be tuned from 2.0 GHz to 2.37 GHz, yielding a tuning range of about 17%. The phase noise of the VCO was measured at five different carrier frequencies (2.00 GHz, 2.10 GHz, 2.20 GHz, 2.30 GHz, 2.37 GHz), both with and without an off-chip inductance L = 100μH. Fig. 4 shows the phase noise of the VCO as a function of the carrier frequency, measured at offset frequencies of 600 kHz and 3 MHz. The phase noise reduction from the in-

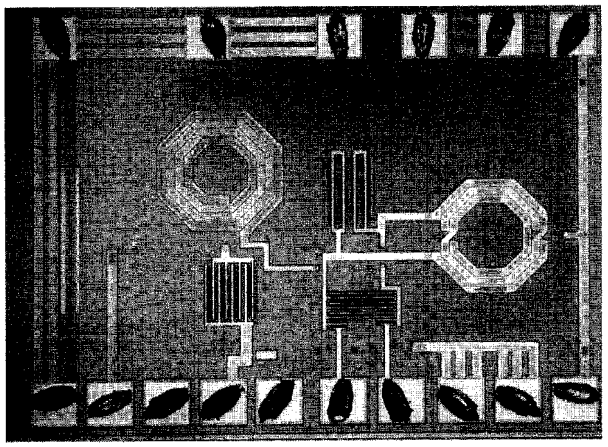

Figure 3. Die photograph of the VCO.

ductive degeneration is about 2 dB at lower carrier frequencies, and as high as 5-6 dB at higher carrier frequencies. The phase noise versus the offset frequency for the two extreme carrier frequencies is shown in Fig. 5. The agreement between these measurements and the simulations of Fig. 2 is excellent above 100 kHz, while both the rolloff at 5 MHz and the large increase in phase noise at offset frequencies below 100 kHz are artifacts of the Europtest phase noise measurement system.

4. Conclusions

A 1.4 V, 9 mA, 2.2 GHz LC-tank CMOS VCO with 17% tuning range has been presented. The proposed inductive degeneration technique, together with an on-chip LC filter, allows for the complete removal of the tail current noise, which is otherwise the largest cause of phase noise in a CMOS differential VCO. The noise factor of the VCO is consequently as low as about 1.5 over the whole tuning range.

5. Acknowledgments

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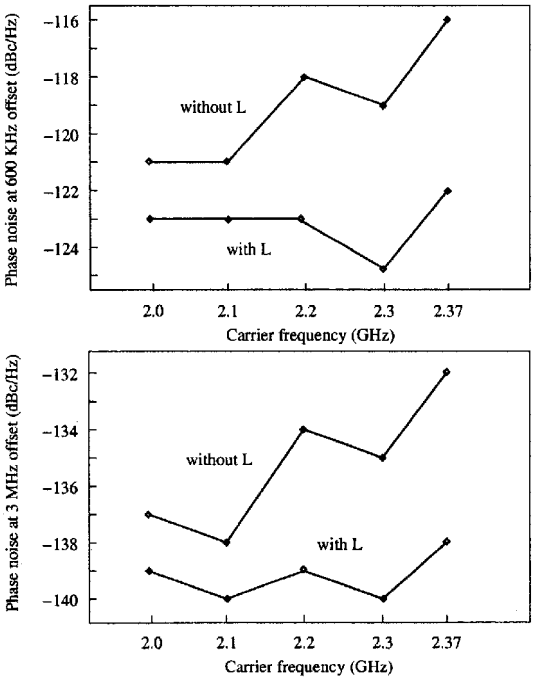

Figure 4. Phase noise of the VCO at 600 kHz (top) and 3 MHz offset frequency.

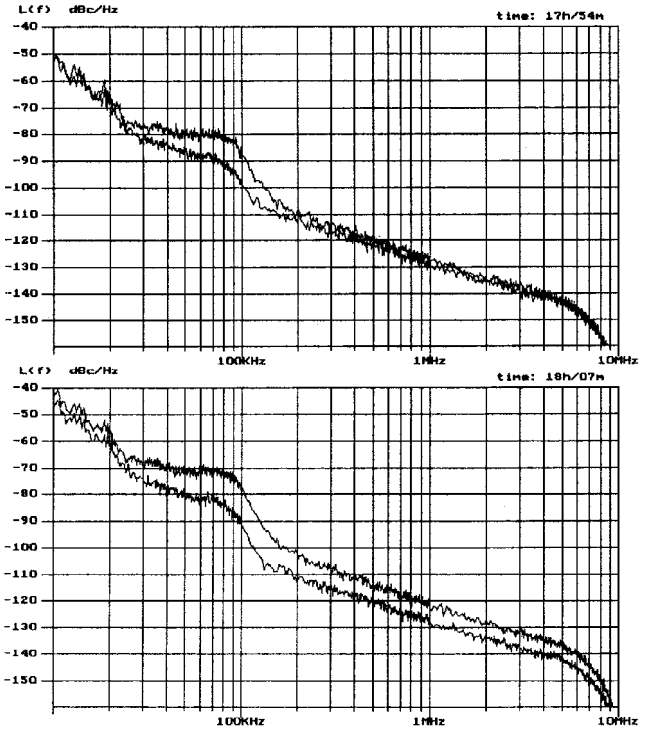

Figure 5. Phase noise of the VCO at 2.0 GHz (top) and 2.37 GHz carrier frequency, with L=0 (higher phase noise) and L=100μH.