A 1.6-to-3.0-GHz Fractional-N MDLL with a Digital-to-Time Converter Range-Reduction Technique Achieving 397fs Jitter at 2.5-mW Power

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***Abstract*—This paper presents an inductor-less fractional-N clock multiplier with low integrated jitter and power. The architecture is based on a multiplying delay locked loop with a sub-sampling bang-bang phase detector and a novel digital-to-time converter (DTC) range-reduction technique which limits the jitter added to the reference signal, at no additional power penalty. The prototype, implemented in 65nm CMOS, covers the 1.6-to-3.0-GHz range and achieves an absolute RMS jitter (integrated from 30kHz to 30MHz) of 397fs at 2.5mW power consumption, leading to a jitter-power figure of merit of -244dB. In-band fractional spurs are as low as -51.5dB and the occupied core area is 0.0275mm^2.**

***Index Terms*—MDLL, DTC, Multiplying Delay-Locked Loop, PLL, Injection-Locking, Low-Jitter, Low-Power.**

I. Introduction

Digitally-controlled multiplying delay-locked loops (MDLLs) [1]-[4], as well as inductor-less injection-locked phase-locked loops (IL-PLLs) [5]-[8], represent an attractive alternative to standard PLLs thanks to their smaller area occupation if compared to PLLs based on LC oscillators, especially in future scaled processes. Moreover, MDLLs and IL-PLLs feature a reduced jitter for a given power consumption, thanks to the wide filtering bandwidth of the controlled oscillator. Among those topologies, MDLLs, performing a periodic replacement of their recirculating edges with cleaner reference edges, offer the largest filtering bandwidth of the ring-oscillator phase noise, and, in practice, their ultimate jitter level is represented by the jitter introduced both on the reference and feedback paths.

The extension to fractional-N frequency multiplication presents some extra challenges due to the need of properly synchronizing injected and recirculating edges [4]. Typically, this synchronization is performed via the introduction of a variable delay to the reference signal before injection, by means of a DTC [1]. However, the DTC degrades the reference signal by introducing jitter which is proportional to the square of the added delay value and inversely to its power dissipation [9]. Thus, the maximum required delay on the reference path (i.e. the DTC range) becomes the key limiting factor of the jitter/power tradeoff in fractional-N MDLLs. This paper presents an innovative technique to reduce the range required by the DTC and thus to limit its jitter contribution.

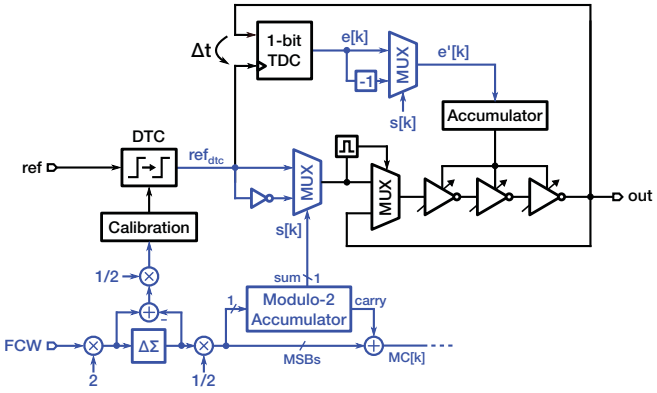

Figure 1. Conceptual representation of a fractional-N MDLL with DTC range-reduction technique.

II. DTC Range-Reduction Technique

Fig. 1 shows the proposed technique applied to a sub-sampling fractional-N MDLL, where a 1-bit time-to-digital converter (1b-TDC) is used to detect the Δt time error between the rising reference and oscillator edges and to generate an error signal, $e[k]$, accordingly. This error signal is then accumulated and used to frequency-tune the multiplexed ring-oscillator. The purpose of the DTC on the reference path is two-fold. On one hand it allows for the injected reference edges to be properly aligned to the recirculating ring oscillator edges. On the other hand, it allows the 1b-TDC to work within a narrow range around $\Delta t = 0$, for which its behaves like a linear phase detector [10]. Conventionally, the control signal for the DTC is directly derived from the quantization error of the $\Delta\Sigma$ re-quantizing the fractional part of the frequency-control-word, FCW. Thus, the range required by the DTC is directly related to the amplitude of the quantization error itself.

The key concept behind the proposed range-reduction technique lies in leveraging the periodicity of the sub-sampling 1b-TDC's characteristic, shown in Fig. 2. Since the 1b-TDC essentially acts as a D-type flip-flop directly sampling the oscillator waveform (with period T_v) on the rising edge of the reference signal (with period much larger than T_v), sweeping the Δt delay between reference and oscillator signals will result in a characteristic mimicking the original oscillator waveform, including its T_v-periodicity. In fact, whenever a high oscillator level is sampled by the reference, the TDC

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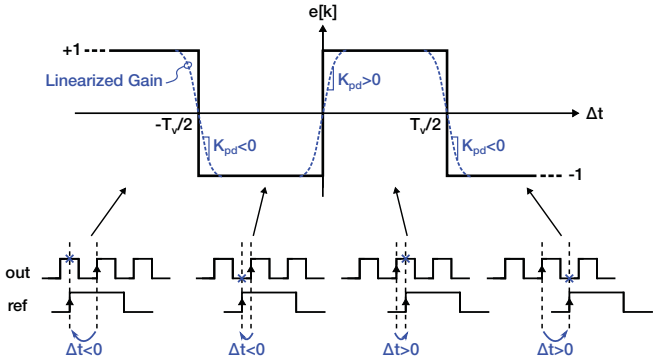

Figure 2. Sub-sampling 1b-TDC characteristic.

output will be $+1$, and when a low level is sampled the digital output is going to be -1.

Typically, only the linear-gain region around $\Delta t = 0$ (where the linearized TDC gain $K_{pd} > 0$) is used for phase detection. Thus, the DTC on the reference path is required to realign every rising reference-edge to its nearest rising output-edge, by providing a delay of up to T_v to ensure this condition.

It becomes evident that a substantial range reduction can be achieved by exploiting both $K_{pd} > 0$ and $K_{pd} < 0$ gain-regions for phase detection, i.e. by realigning every rising reference-edge to its nearest output-edge, be it a rising or a falling one. This effectively halves the required DTC range to only $T_v/2$, provided that the TDC's output is inverted when a $K_{pd} < 0$ region is used. Referring to Fig. 1, the selective inversion can be achieved by multiplexing between the original error signal $e[k]$ and its sign-changed version, depending on the value of $s[k]$. This signal is obtained from the FCW as follows. First, a $\Delta\Sigma$-modulator is used to re-quantize the fractional bits of the FCW, except for the MSB. This operation is represented by multiplying and dividing by two the modulator's input and output, respectively. The quantization error of the $\Delta\Sigma$-modulator is also divided by two and used to control the DTC. Then, the integer part of the FCW, together with the remaining MSB of the fractional part, are re-quantized by a modulo-2 accumulator which essentially behaves like a single-bit first-order $\Delta\Sigma$-modulator. The sum of the modulo-2 accumulator represents the control signal $s[k]$, which is used to selectively invert the 1b-TDC's output.

To further illustrate the behavior of the presented scheme, the diagram in Fig. 3(a) shows the relevant signals for the case of a first-order $\Delta\Sigma$ modulator. In the case of fractional-N operation, $MC[k]$ switches between N and $(N+1)$, and the time error between the edges of the output and the reference signal follows a ramp from zero to T_v. Instead, the accumulated $\Delta\Sigma$ quantization error driving the DTC ranges between 0 and $T_v/2$, resulting in a $T_v/2$ misalignment between rising edges of the DTC-delayed reference signal and the recirculating oscillator edges, in the second part of the ramp in figure (when $s[k] = 1$). Recalling the periodicity of the 1b-TDC characteristic in Fig. 2, this simply means that a $K_{pd} < 0$ region is targeted for phase detection and

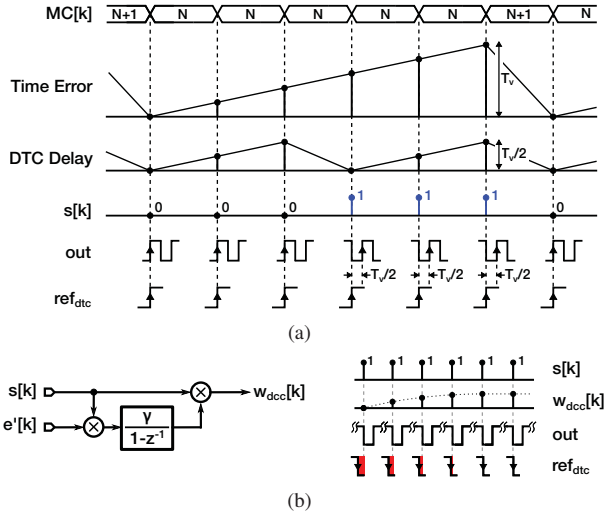

Figure 3. Signal diagram in fractional-N mode (a) and oscillator duty-cycle corrector implementation and signal diagram (b).

the correct time error can still be recovered by inverting the TDC output when $s[k] = 1$. Since the DTC-delayed reference signal ref_{dtc} is also used for injection into the multiplexed ring-oscillator, it would too exhibit a $T_v/2$ misalignment, resulting in a rising reference edge being injected in place of a falling oscillator edge, leading to severe spectral degradation and possible failure to achieve lock. Luckily, this issue can be easily solved by using $s[k]$ to also selectively invert the reference signal to be injected.

Since real ring oscillators may not ensure a perfect 50% duty-cycle, a residual time error between the injected reference signal and the recirculating edges will occur on the polarity switch, causing a degradation in the output spectrum. This issue is solved by the introduction of a least-mean-square (LMS) based duty-cycle corrector (DCC), illustrated in Fig. 3(b). The LMS converges to a digital value $w_{dcc}[k]$, which, summed to the DTC input, nulls on average the correlation between $s[k]$ and TDC error, $e'[k]$. In practice, this guarantees that the timing mismatches induced by duty-cycle errors of the ring oscillator are effectively canceled out by the DTC.

III. Circuit Implementation

Fig. 4 shows the full block diagram of the proposed MDLL, with key elements enabling the DTC range-reduction highlighted in blue. With respect to the previously discussed concept scheme of Fig. 1, a dual-phase-injected ring oscillator (DPI-RO) is used. The DPI-RO is made of five pseudo-differential inverter stages and a multiplexer is used to periodically open the ring and replace the recirculating edge with a reference one. A simple pulser circuit identifies the rising edges the signal to be injected and controls the multiplexer accordingly. A transmission-gate based polarity reverser on the reference path, allows for an effortless polarity swap of the differential DTC-delayed reference signal, when $s[k] = 1$.

Fine frequency tuning is achieved by the previously described 1b-TDC sub-sampling loop, whereas coarse frequency

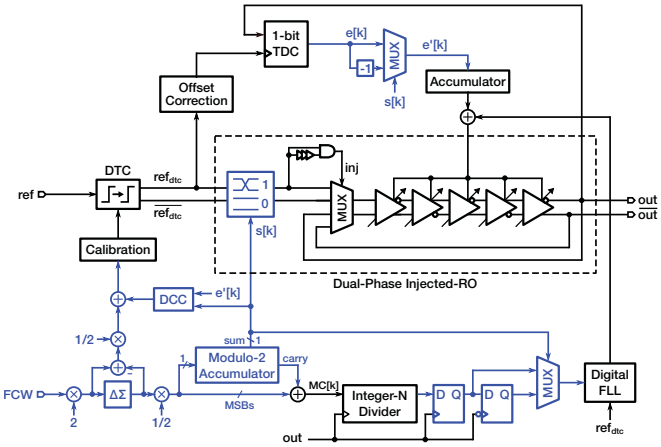

Figure 4. Schematic of the proposed MDLL with blocks enabling the DTC range-reduction technique highlighted in blue.

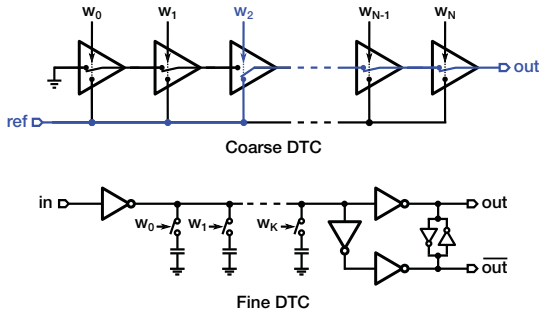

Figure 5. Coarse and fine DTC schematics.

acquisition is achieved by means of a digital frequency-locked loop (FLL). The FLL is switched-off after locking to save power and embeds an integer-N divider, whose modulus control is dithered by the two-step re-quantized FWC, $MC[k]$. The sum of the modulo-2 accumulator, $s[k]$, is also used in the FLL to selectively resample the divider output with either the rising or the falling edge of the oscillator (out). In practice, switching between the two resampled outputs of the divider introduces a $T_v/2$ additional delay on the divided signal, compensating for the reduced DTC range on the reference path. An automatic time offset compensation is used to cancel reference spurs arising from static timing mismatches between injection and locking reference paths [1].

The DTC circuit schematic, segmented into a coarse- and a fine-resolution stage, is shown in Fig. 5. The coarse DTC is comprised of a series of cascaded CMOS buffer cells. A multiplexer embedded into each cell allows the reference signal to be injected into one specific cell, effectively setting the delay line length and thus its total delay. The fine DTC is instead implemented by digitally varying the capacitive load of a CMOS inverter through a switched capacitor bank. Two cross-latched inverters then perform a single-ended to pseudo-differential signal conversion, to allow for the injection polarity inversion in the DPI-RO. A digital calibration block

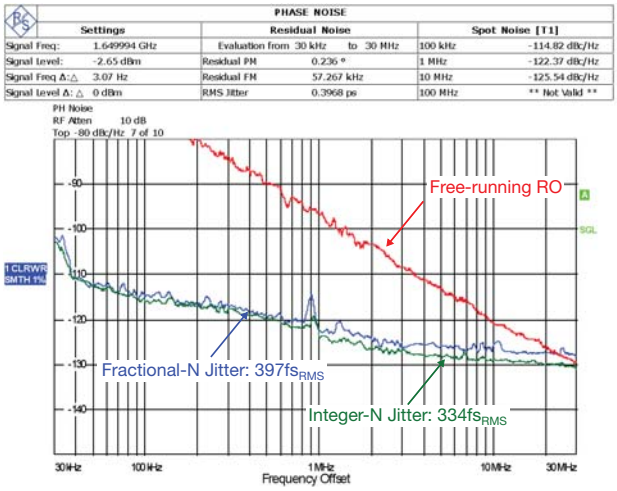

Figure 6. Comparison of phase noise measured in fractional-N operation (blue trace), integer-N operation (green trace) and open-loop ring-oscillator (red trace).

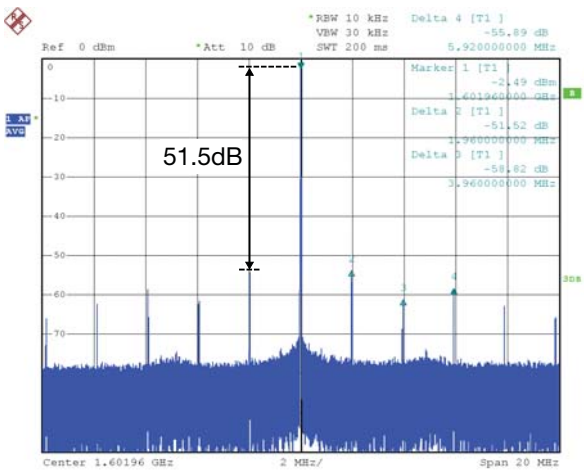

Figure 7. Near-integer fractional spurs.

takes care of the coarse DTC's non-linearity and mismatches, and also tunes the gain of the fine DTC to ensure perfect overlap between the segmented stages. Both calibrations are based on LMS-estimated gains and operate in background.

IV. Measurements

The proposed MDLL has been fully integrated in 65nm CMOS and occupies a core area of 0.0275 mm^2 (0.0175mm^2 for the digital core and 0.01mm^2 for analog blocks, excluding the output buffer). Fig. 6 shows the measured phase noise in both integer-N and fractional-N modes, as well as the free-running ring-oscillator profile, whereas Fig. 7 provides the spectrum for a near-integer channel. The highest fractional spur is at -51.5dBc, whereas the reference spur is at -50dBc. The maximum RMS jitter is 334fs and 397fs for the integer-N and the fractional-N case, respectively. The synthesizer core dissipates 2.5mW from a 1.2V supply. Table I and

Table I

	This Work	S. Kundu ISSCC '16	G. Marucci ISSCC'14	W. Deng ISSCC'15	A. Li JSSC'17	B. Liu CICC'18	J. Gong RFIC'18
Architecture	**MDLL**	MDLL	MDLL	IL-PLL	IL-PLL	IL-PLL	IL-PLL
Output Frequency (GHz)	**1.65**	1.4175	1.65	1.5222	1.152	0.97	2.431
Tuning Range (GHz)	**1.6-3.0**	0.2-1.45	1.6-1.9	0.8-1.7	N/A	0.6-1.7	1.8-2.7
Reference Frequency (MHz)	**100**	87.5	50	380	48	100	64
Multiplication Factor (N)	**16-30**	2-16	32-38	2-4	24	6-17	28-42
Reference Spur (dBc)	**-50**	-45	-47	-63	N/A	N/A	-43.6
Fractional Spur (dBc)	**-51.5**	N/A	-47	N/A	-57	-58.8	-45.8
Power Dissipation (mW)	**2.5**	8	3	3	19.8	2.5	1.33
Integrated Jitter (ps)	**0.397**	2.8	1.4	3.6	1.48	1.2	1.6
FoM* (dB)	**-244**	-222	-232	-224.2	-223.6	-234.4	-234.7
CMOS Process (nm)	**65**	65	65	65	65	65	40
Area Occupation (mm^2)	**0.0275**	0.054	0.4	0.048	0.6	0.12	0.13

$$*\text{FoM} = 10\log\left[\left(\frac{\text{Jitter}}{1\text{s}}\right)^2 \cdot \left(\frac{\text{Power}}{1\text{mW}}\right)\right]$$

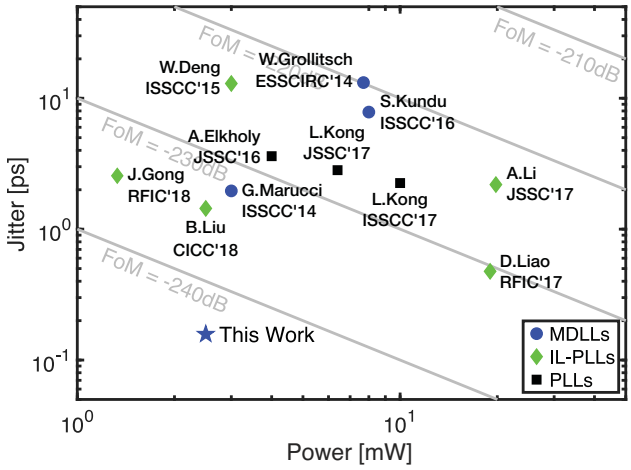

Figure 8. Comparison to state of the art fractional-N MDLLs, inductor-less PLLs and IL-PLLs.

Fig. 8 summarize the measured performances and provide a comparison to state-of-the-art digitally-controlled fractional-N MDLLs, inductor-less PLLs and IL-PLLs. In fractional-N mode, the synthesizer reaches a worst-case figure of merit (FoM) of -244dB. A die micrograph is shown in Fig. 9.

V. Conclusion

Thanks to the innovative DTC range-reduction technique, the presented fractional-N MDLL architecture achieves -244dB FoM, which is 10dB better than the best fractional-N inductor-less PLL [8].

Acknowledgment

The authors would like to thank Stefano Pellerano and Intel Corporation for supporting this work.

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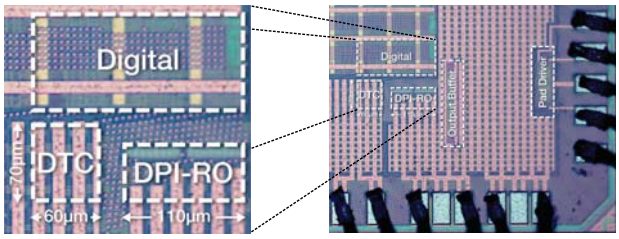

Figure 9. Die micrograph.

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