21.4 A 10b 50MS/s 820µW SAR ADC with On-Chip Digital Calibration

Masato Yoshioka, Kiyoshi Ishikawa, Takeshi Takayama, Sanroku Tsukamoto

Fujitsu Laboratories, Kawasaki, Japan

Rapid growth in the demand for "Green-IT" or medical applications requires power efficient ADCs. SAR ADC power scales with CMOS technology because it does not need operational amplifiers, which are getting difficult to design in deeply scaled CMOS. Recent published SAR ADCs have no static current, which improves energy efficiency [1, 2]. Split capacitor digital-to-analog converter (CDAC) is one of the best architectures for high resolution SAR ADC, but is very sensitive to the splitting capacitor because of its fractional value and parasitic. Conventional SAR ADC needs approximately 10 times faster external clock if it has no internal clock generator. However the internal SAR clock generation enables the external clock frequency to be the same as the sampling rate, but suffers from unstable operation caused by large PVT delay variation. This ADC is designed with on-chip digital calibration techniques, comparator offset calibration, CDAC linearity error calibration and internal clock frequency control to compensate for the PVT variation. The ADC is integrated in 65nm CMOS and achieved 10b at 50MS/s while consuming 820µW from a 1.0V supply.

Figure 21.4.1 shows the block diagram of the ADC. It consists of 10b split-CDAC, comparator, internal clock generator, SAR controller and digital calibration blocks. A 50MHz external clock with 25% duty ratio is required. The analog signal is sampled when CLK="H". When CLK="L", the analog signal is converted into digital using the internally generated clock Φ_C. Offset error of the comparator and CDAC linearity error are calibrated in the foreground and the frequency of the internal clock Φ_C is controlled in the background.

Figure 21.4.2 shows the comparator schematics and offset calibration. A dynamic latch comparator without preamplifier is used to reduce power consumption. The comparator offset appears as CDAC linearity error, so it must be calibrated prior to CDAC calibration. Body biasing technique is applied to the input differential pair NMOS, M_P and M_M, because it does not reduce speed like other trimming methods [1]. In the offset calibration period, the same input signal is connected to the input pair, VIP and VIM. The comparator output is fed back to either V_{BP} or V_{BM} to raise the body bias using the DAC. This is repeated until the comparator output changes. The offset is reduced less than 0.25 LSB.

The 10b split-CDAC is shown in Fig. 21.4.1. The analog input is sampled by upper 4b capacitors C_9-C_6, C_H, C_L and C_x. This design makes it possible to remove the reference voltage as well as reducing the input load. The unit capacitor is smaller than the mismatch limit for 10b accuracy, because it can be compensated by calibration. As a result, the input load capacitance is reduced down to 530fF which is necessary for 10b with 1.2Vp-p differential input. This also reduces the power needed to drive the switches of the CDAC. The split capacitor C_B and upper 3b C_9 to C_7 are calibrated to compensate for mismatch. For the first step, C_B is calibrated by adjusting the C_V. C_B is designed slightly larger than the ideal fractional capacitance and C_V is adjusted till the weight of C_5-C_0 and C_D becomes identical with C_6 [3]. As a result, mismatching between C_6 and the lower bit capacitors is compensated. After calibrating the C_B, mismatching between C_9 and the lower bit capacitors C_8-C_0 and C_D is calibrated. C_9 is connected to VDD and C_8-C_0 and C_D are connected to GND while comparator input node N_{IN} is set to V_{CM}, then V_{CM} is disconnected and C_9 is connected to GND and C_8-C_0 and C_D are connected to VDD. Ideally N_{IN} stays at VCM but any mismatch causes voltage change which the comparator detects. The Cal CDAC is adjusted until the comparator judgment output changes. The Cal CDAC control code is stored and is used in the actual conversion. C_8 and C_7 are calibrated in the same way [4].

Figure 21.4.3 shows the internal clock generator. It works as an oscillator, including the comparator during the hold period, CLK="L". Φ_C is provided as a clock of the comparator and SAR controller, and Φ_D is the CDAC control signal which synchronized with Φ_C. Approximately 70% of the cycle period of Φ_C is required by the SAR controller and CDAC delay time, which is independent of analog input voltage. Approximately 30% is needed by the comparator, which has a delay which varies with input level . This suggests that T_d should be adjusted to around 500ps based on SAR and CDAC response, Prior works have no means to adjust the delay, a fixed delay is used. An internal clock frequency controller solves these problems, for example too fast internal clock will cause incomplete CDAC settling and too slow clock degrades conversion rate. A variable delay controller is implemented to optimize the cycle period of Φ_C. The 4b delay stage is provides coarse tuning and load capacitance provides 3b fine tuning. The rising edges of the Φ_C are counted by the edge counter and the delay is adjusted to be 10 edges. Finally Φ_C is optimized against PVT variation. This is done in the background.

Figure 21.4.7 shows the chip micrograph. The prototype ADC is fabricated in 1P7M 65nm CMOS with MIM capacitors. The die area of the ADC is 0.039mm^2. The digital calibration area is 0.013mm^2. Figure 21.4.4 shows DNL and INL before and after calibration. DNL is improved from 1.4LSB to 0.82LSB, INL is improved from 3.9LSB to 0.72LSB. Figure 21.4.5(a) shows input signal dependency of SNDR at 50MS/s. SNDR is 56.9dB at 2MHz input frequency and 56.6dB at Nyquist frequency. Figure 21.4.5(b) shows conversion rate dependency of SNDR at 2MHz input frequency with and without internal clock frequency control. Conversion errors can be seen at high clock rates, caused by too large delay. Figure 21.4.5(c) shows the measured FFT spectrum at 50MS/s with a 2MHz input frequency. Power consumption including the digital calibration circuits at 50MS/s and 26MHz input frequency is 820µW with 1.0V supply voltage. This corresponds to FoM=30fJ/conv-step. Figure 21.4.6 summarizes the performance.

References:

[1] V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. Van der Plas, J. Craninckx, An 820µW 9b 40MS/s Noise-Tolerant Dynamic-SAR ADC in 90nm Digital CMOS, *IEEE International Solid-State Circuits Conference*, vol. 51, pp. 238 - 239, February 2008.

[2] A. Agnes, E. Bonizzoni, P. Malcovati, F. Maloberti, A 9.4-ENOB 1V 3.8µW 100kS/s SAR ADC with Time-Domain Comparator, *IEEE International Solid-State Circuits Conference*, vol. 51, pp. 246 - 247, February 2008.

[3] Y. Chen et al, Split Capacitor DAC Mismatch Calibration in Successive Approximation ADC, *2009 IEEE Custom Integrated Circuits Conference*, pp. 279 - 282, September 2009

[4] Hau-Seung Lee, David A. Hodges, Paul R. Gray; A self-calibrating 15 bit CMOS A/D converter, *IEEE Journal of Solid-State Circuits*, vol. 19, pp. 813 - 819, December 1984.

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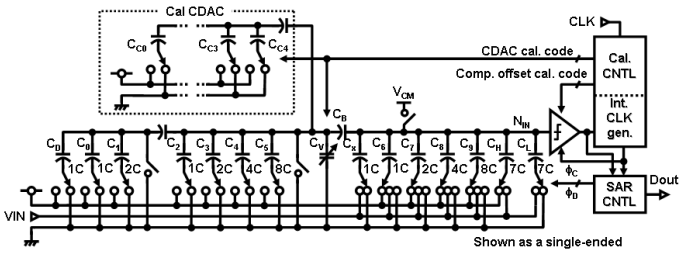

Figure 21.4.1: ADC block diagram.

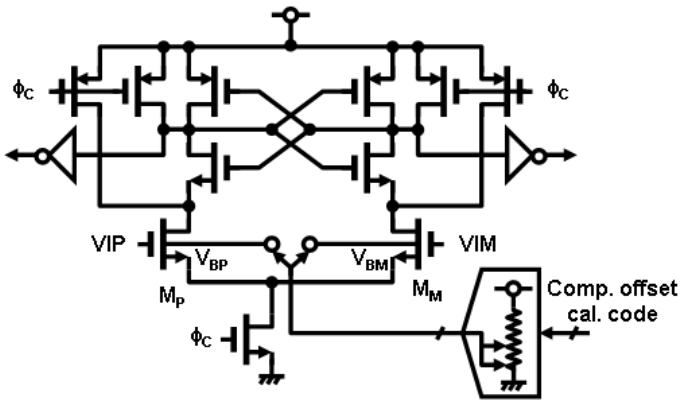

Figure 21.4.2: Schematic of the comparator.

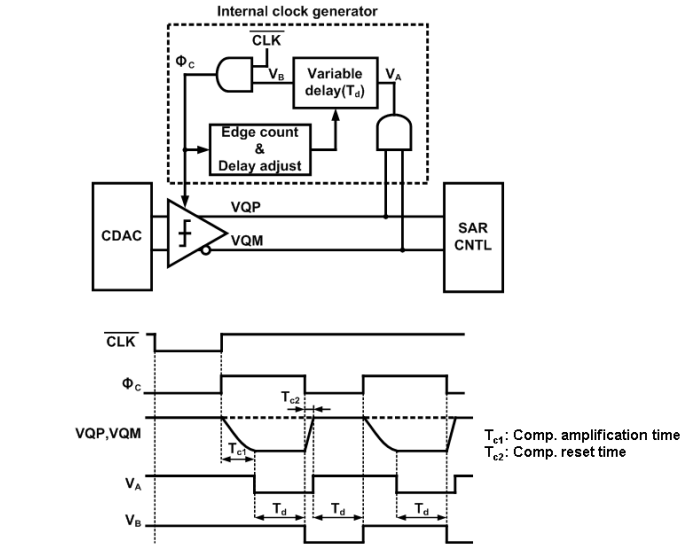

Figure 21.4.3: Schematic of the internal clock generator.

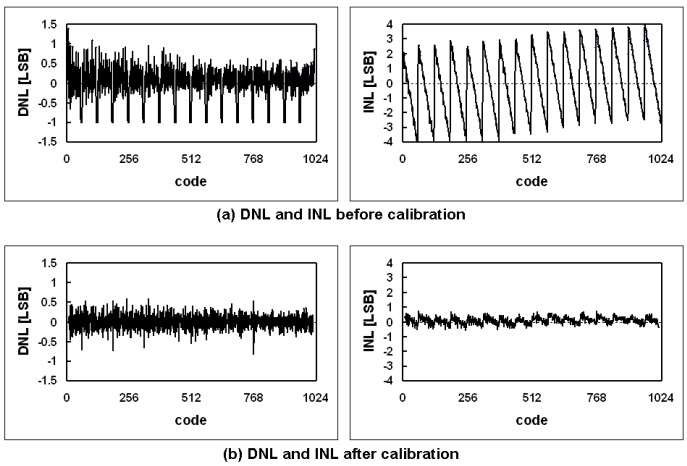

Figure 21.4.4: Measured DNL and INL at 50MS/s.

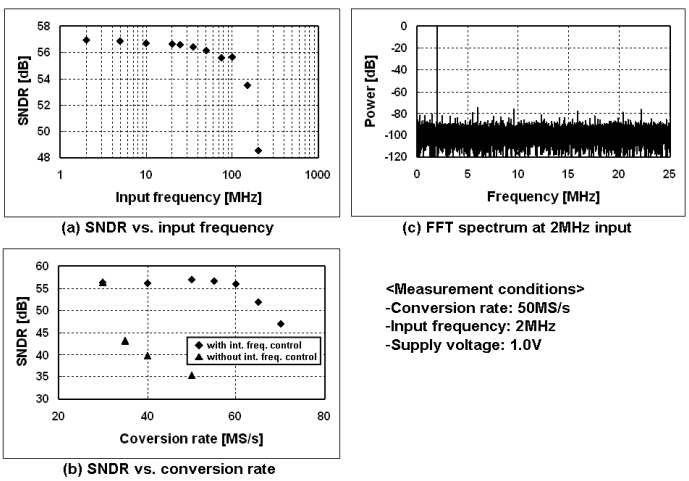

Figure 21.4.5: Measured SNDR vs. input frequency or conversion rate.

Technology	65nm CMOS process
Resolution	10bit
Conversion rate	50MS/s
Active area	0.039mm^2
Input range	1.2Vp-p differential
Supply voltage	1.0V
SNDR	56.9dB @ 2MHz input 56.6dB @ 25MHz input
Total power consumption	820μW (Analog:450μW, Digital:370μW)
INL	< 0.72LSB
DNL	< 0.82LSB
FoM (P/(2*BW*2^{ENOB}))	30fJ/conv-step

Figure 21.4.6: Summary of ADC performance.

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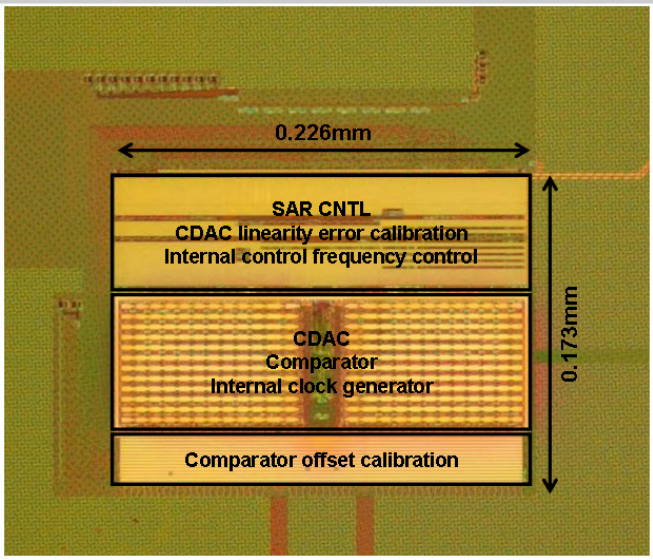

Figure 21.4.7: Chip micrograph.

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