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A High-Performance Stacked-CMOS SRAM Cell by Solid Phase Growth Technique

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1. INTRODUCTION

A stacked-CMOS SRAM cell with a polysilicon p-ch TFT load has been attracting much attention as a high density and low standby-current SRAM[1-3]. In this paper, we demonstrate a high-performance stacked-CMOS SRAM cell with remarkably improved polysilicon p-ch TFT load-characreristics ; leakage-current of 0.07pA/μm and on/off ratio of 10^5 at the logic swing of 3V, which could satisfy 4Mbit SRAM with standby-current of 0.3 μA. The high-performance operation has been attained as a result of enlarging the grain size of the polysilicon film for the active region of the p-ch TFT by a novel solid phase growth (SPG) technique.

2. Cell Design and Fabrication

The cross-sectional view of the CMOS inverter in the stacked-CMOS SRAM cell is shown in Fig.1, where the polysilicon p-ch TFT load with bottom gate structure is sited on the n-ch drive MOS transistor so as to reduce the cell area and the thickness of the active region of the p-ch TFT. The cell desigh concept for a SRAM with low standby-current and high noise immunity is that leakage-current and on/off ratio of the p-ch TFT are low and high, respectively.

In order to satisfy these requirements, it is important to enlarge the grain size of the polysilicon film for the p-ch TFT. For this purpose, we have developed a novel solid phase growth (SPG) technique.

The grain size of the polysilicon film after SPG process is strongly dependent on the initial nucleation rate in the amorphous silicon film. In order to decrease the nucleation rate in the amorphous silicon film, Si_2H_6 source gas was used so as to decrease the deposition temperature. The density of grains as a function of the annealing time is shown in Fig.2, where three kinds of deposition temperature are compared. As shown in this figure, the density of grains is reduced with decrease of the deposition temperature. The properties of the deposited films are summarized in Table 1. The nucleation rate is calculated[4] with aids of the experimental result shown in Fig.2. It is seen that the nucleation rate of the grains is reduced with decrease of the deposition temperature although the growth rate of the grains is the same. As a result, the grain size of the polysilicon film after SPG process is enlarged with decrease of the deposition temperature. The TEM photograph of the polysilicon film after SPG process, which is deposited at a temperature of 485 °C, is shown in Fig.3. It is noted that the grain size as large as 5 μm is seen.

Another point to be considered for enlarging the grain size of the polysilicon film through the SPG process is the reduction of the surface roughness of the gate oxide of the p-ch TFT. The reduction of the surface roughness is effective in suppressing the stress-induced nucleation in the amorphous silicon film during the course of the SPG process. The surface roughness is mainly caused by silicon migration during thermal diffusion of phosphorus into the gate polysilicon. Therefore, we used the ion-implantation method for forming the gate for the p-ch TFT instead of the thermal diffusion. The surface roughness of the gate oxide as a function of P^+ concentration is shown in Fig.4 for the cases of P^+-diffused and P^+-implanted gates. It is clearly shown that the surface roughness of the gate oxide formed thermally on the P^+-implanted gate is smaller than that on the P^+-diffused gate. The formation of the grains in the amorphous silicon film is shown in Fig.5, where the cases of P^+-implanted gate and P^+-diffused gate are compared. As shown in the photographs, the density of grains is decreased in the case of P^+-implanted gate.

3. Cell Characteristics

The subthreshold characteristics of the polysilicon p-ch TFT load are shown in Fig.6, where the characteristics of the polysilicon-TFT, the SPG polysilicon-TFT on P^+-diffused gate, and the SPG polysilicon-TFT on P^+-implanted gate are compared. The thicknesses of the active region and gate oxide are 50nm and 60nm, respectively. The SPG polysilicon-TFT on P^+-implanted gate shows an excellent performance such as leakage current of 0.07pA/μm and on/off ratio of 10^5 at the logic swing of 3V. This result shows that the present cell is usefull as a 4Mbit SRAM with a standby-current of about 0.3 μA and high noise immunity at the supply voltage of 3V.

4. Conclusion

We have developed a high-performance stacked-CMOS SRAM cell with remarkably improved polysilicon p-ch TFT load-characteristics ; leakage current of 0.07 pA/μm and on/off ratio of 10^5 at the logic swing of 3V. This high-performance is due to the successful use of a novel SPG technique which features the reductions of the initial nucleation rate in the amorphous silicon film and of the surface roughness of the gate oxide for the p-ch TFT. The developed cell is promising for a 4Mbit SRAM with standby-current of 0.3 μA and high noise immunity at the supply voltage of 3V.

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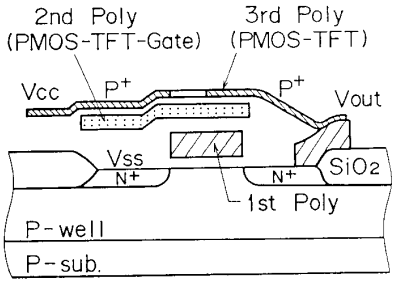

Fig. 1 Cross-sectional view of inverter in stacked-CMOS SRAM cell.

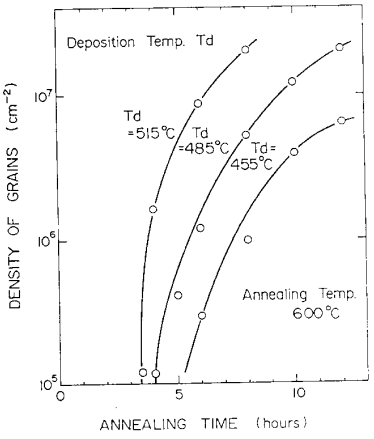

Fig. 2 Density of grains as a function of annealing time.

Table 1 Properties of amorphous silicon films deposited by LPCVD using Si_2H_6 source gas.

Deposition Temperature (°C)	Nucleation Rate (/cm².sec)	Growth Rate (nm/sec)	Maximum Grain Size (μm)
455	280	0.13	7
485	810	0.14	5
515	1100	0.13	3.5

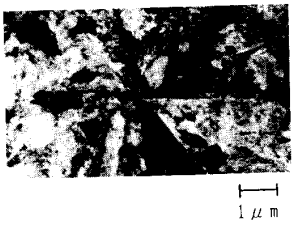

Fig. 3 TEM photograph of polysilicon film after SPG process.

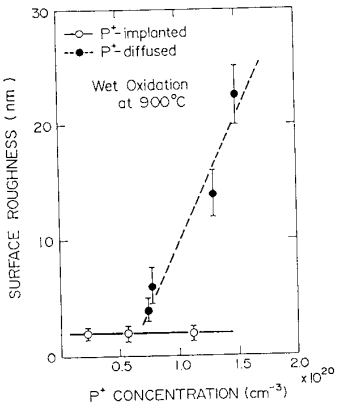

Fig. 4 Surface roughness of gate oxide as a function of P⁺concentration.

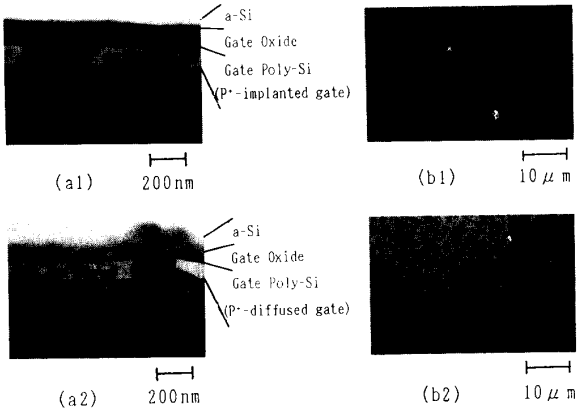

Fig. 5 Comparison of two kinds of grain formation in amorphous silicon films.
(a)Cross-sectional TEM photographs of surface roughness.
(b)Optical micrographs of grain formation after 4h annealing.

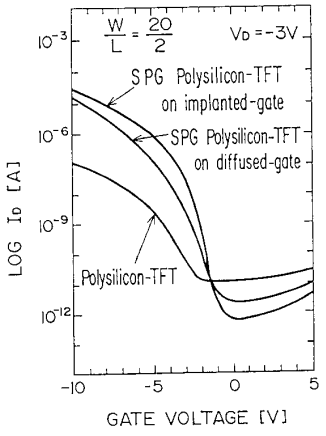

Fig. 6 Subthreshold characteristics of fabricated p-ch TFTs.