SON (Silicon-On-Nothing) P-MOSFETs with totally silicided ($CoSi_2$) Polysilicon on 5nm-thick Si-films: The simplest way to integration of Metal Gates on thin FD channels

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Abstract

In this paper, the first SON (Silicon On Nothing) devices with metal gate are presented. Extremely thin fully depleted Si- films are recognized to be integrable with single-metal gate (mid-gap) due to their intrinsically low threshold voltage. In this work, we present mid-gap $CoSi_2$ metal gate by total gate silicidation on SON transistors with Si-conduction channel thickness down to 5nm. Due to its architecture and to the continuity between SD areas and the bulk, SON transistors allow deep silicidation process down to the gate oxide, meaning that no more polysilicon is left. SON PMOS devices were performed with 55nm $CoSi_2$ gate length with 5nm of Si-channel thickness, and show excellent performances (350μA/μm I_{on} with only 0.1nA I_{off} @-1.4V with T_{ox}=20Å). The polydepletion is of course suppressed and the gate resistance (<2Ω/□) is very competitive for RF applications.

Introduction: thin FD-films and metal gates

Rapid acceleration in gate-length scaling for end-of-roadmap devices is needed [1-3]. Therefore, extremely thin film SOI and DG devices are extensively studied for their potential to suppress SCE [4-9]down to very short channels. However, SCE control for such aggressive gate length as 20nm needs extremely thin and controlled Si-channel thickness down to 5nm (fig. 1).

As presented in this figure, V_{th} decreases with the film thickness, leading to intolerably high off current. One solution is to increase the channel doping in the range of 6 to $8x10^{18}cm^{-3}$ (fig. 2), that however degrades mobility.

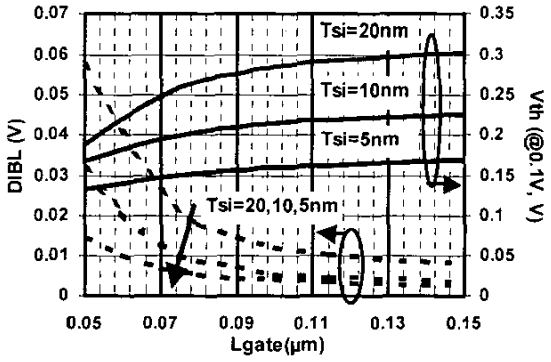

Fig.1: Influence of the Si-channel thickness (T_{Si}) of simulated SON devices on the subthreshold voltage (@Vdd=0.1V) and on the DIBL for downscaling gate length. SCE is reduced with decreasing T_{Si}. As shown in the graph, the threshold voltage value decreases with T_{Si}. Simulation parameters: N_{ch}=3.5x10^{18}cm^{-3}, T_{ox}=12Å.

Such high doping offsets the intrinsic advantages of FDSOI devices that are capable to suppress SCE with undoped channels. The use of mid-gap gates is thus required for V_{th} adjustment with lowly-doped channels, and may be also useful for polydepletion and gate-resistance reduction. In this paper, we performed for the first time totally silicided gates on SON devices, with very well controlled and reproducible 5nm thin Si-conduction channel.

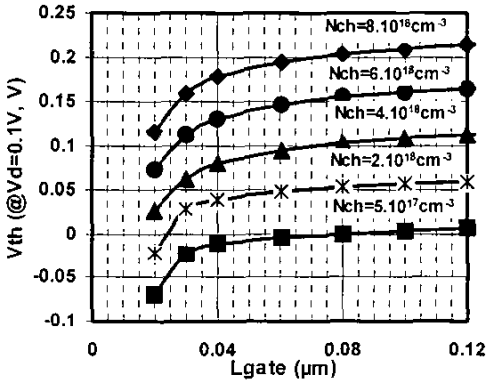

Fig.2: Influence of the Si-channel doping (N_{ch}) on simulated SON devices. Vth adjust needs high channel doping (above 6-8x10^{18}cm^{-3}) than can impact on the mobility of the devices, while SCE are controlled by T_{Si} and T_{box}.Simulation parameters: T_{Si}=5nm , T_{ox}=10Å.

Totally silicided gates without CMP: application to SON devices

As shown in figure 3, SON devices were fabricated in the way described in [10-11], were the empty tunnel is fulfilled with the RTO(20Å)/HTO(50Å)/Si_3N_4(300Å) stack.

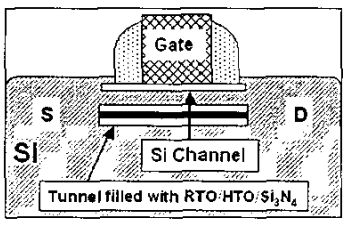

Fig.3: Structure of the SON transistor. The tunnel is fulfilled with the RTO(20Å)/HTO(50Å)/Si3N4(300Å) stack. The continuity between S/D areas and the bulk allows comfortable silicidation process.

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As the thin Si-film was defined with highly-controlled epitaxy process, conduction-channel thickness could be downscaled to 5nm. While voids are created on thin FDSOI devices during the standard silicidation process (fig. 4), SON architecture allows comfortable silicidation thanks to the metallurgical contact between S/D and the bulk (fig. 5).

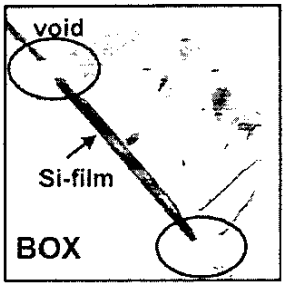

Fig.4: Voids formation during silicidation $CoSi_2$ of thin FDSOI films

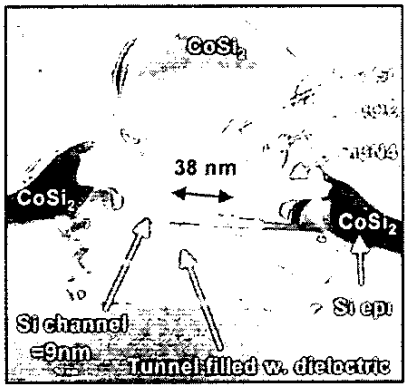

Fig.5: Example of short SON MOSFET (Lgate=38nm) after silicidation. Co layer reacts with the mono-Si without lateral extend thanks to metallurgical contact with body-Si. Measured Tsi=9nm.

Thanks to that, the deposited Co reacts with the mono-Si without creating voids. Figure 6 describes the process of the total gate silicidation: (a) the structure is covered with Co+TiN capping and (b) RTP is performed for $CoSi_2$ formation down to the gate oxide. TEM pictures were performed on morphological bulk 0.1µm structures, and show that the oxide integrity was perfectly ensured [12] but some non-transformed poly-Si residues were present in large capacitances.

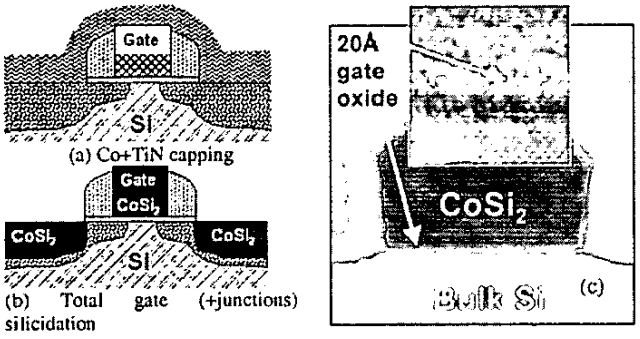

Fig.6: Total gate silicidation steps. Standard process is realized and the devices are covered by Co+TiN capping layers. RTP is then performed for $CoSi_2$ formation down to the gate oxide. TEM picture (c) shows an example of 0.1µm totally silicided gate on a bulk wafer. The insert in (c) shows that the gate oxide integrity is conserved.

In this paper, we have optimised the Co capping that has allowed elimination of non-transformed poly-Si residues (fig.7).

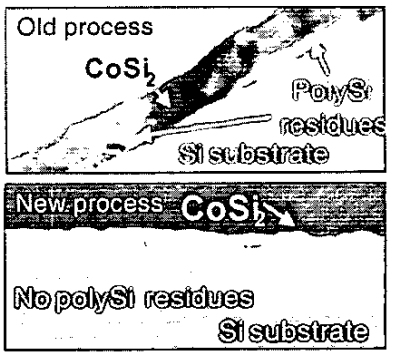

Fig.7: Optimization of Co+TiN capping has allowed elimination of non-transform poly-Si residues.

Figure 8 shows the implementation of this process to SON devices, with reduced gate height (800Å) in order to limit silicidation depth in the junctions. SON transistors were performed with this new process and figure 9 shows that the 800Å gates were totally transformed into $CoSi_2$.

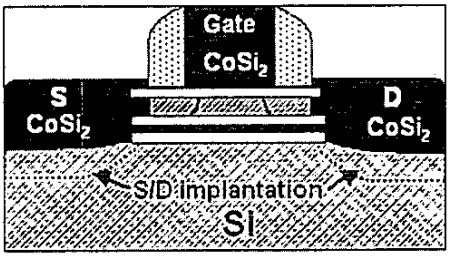

Fig.8: Implementation of the total gate silicidation process to SON devices. SON architecture allows total gate silicidation process without creating voids in the Si-film. This is thank to the metallurgical contact between S/D and bulk. Gate height was equal to 800Å.

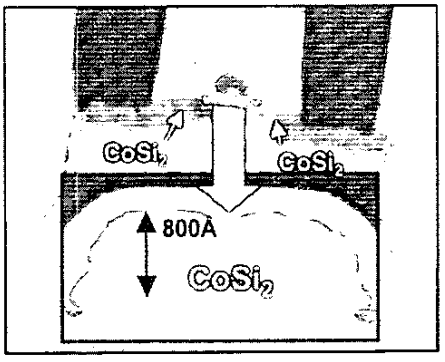

Fig.9: Example of SON transistor with metal gate integration. Silicidation process induces deep junctions (800Å depth) that can be included in deliberately deepened SD implantation (Double implant, see fig.11). Gate height=800Å and T_{ox}=20Å.

Figure 10 shows the 5nm-thick Si-channel. Note in particular that top and bottom interfaces are both of similar quality that demonstrates that the SON tunnel etching is a high quality and a highly selective process.

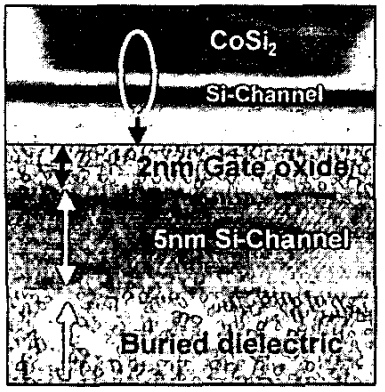

Fig.10: Plasmon and HRTEM pictures showing the thickness of the Si-channel. Measured T_{Si}=5nm, with perfect top and bottom interfaces.

Finally, to prevent I_{diode} leakage, a double S/D implantation was performed: a shallow one after S/D etching and a conventional one (determined by the requirements of gate doping) after S/D epitaxy, see fig.11. It is worth noting that only the SON architecture enables the total silicidation process. On bulk it leads to too deep silicide and thus to diode leakage, and on FDSOI it leads to voids under spacers (unless elevated S/D are used).

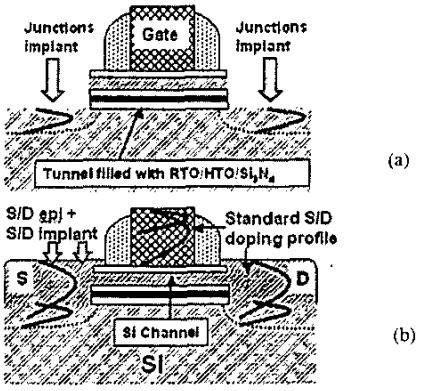

Fig.11: (a) Shallow implantation after the S/D areas etching. (b) Standard S/D implant after S/D epitaxy. Thank to deeper hard junctions, this process suppresses diode leakage between $CoSi_2$ and the bulk.

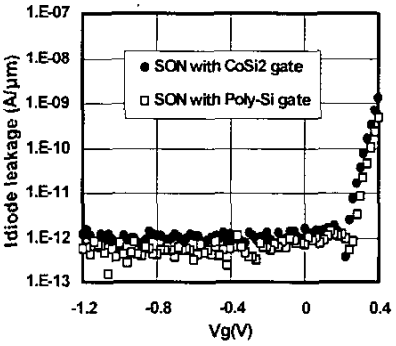

Fig.12: Ibulk leakage of midgap gates SON devices compared to Poly-Si SON transistors. The leakage current is the same, showing that the diode current is not degraded by the deep silicidation process (thanks to double S/D implantation -Fig.11).

Electrical results down to 55nm gates

Thanks to the double S/D implantation, I_{diode} leakage of midgap gates SON devices is the same compared to poly-Si gate SON transistors (fig.12). C(V) measurements confirm that the CoSi2 gate has suppressed the polydepletion effects (fig. 13).

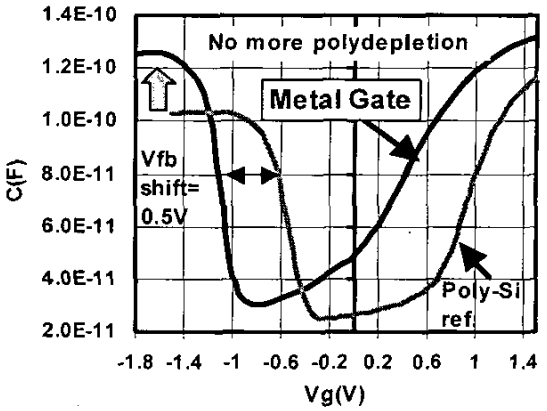

Fig.13: C(V) curves of PMOS transistors with W/L=100µm/100µm. $CoSi_2$ gate suppresses the polydepletion and induces a 0.5V V_{FB} shift.

Electrical performances are presented on 55nm PMOS transistor with 5nm of conduction-channel thickness.

Figure 14 shows highly SCE-immune devices (only 60mV of DIBL and a subthreshold slope of 73mV/dec). Thank to the V_{th} adjustment with midgap gate (V_{th}=-0.47V @-0.1V, Figure 15), I_{off} was reduced to 0.1nA/µm for 350µA/µm of drive current @-1.4V (see fig. 16).

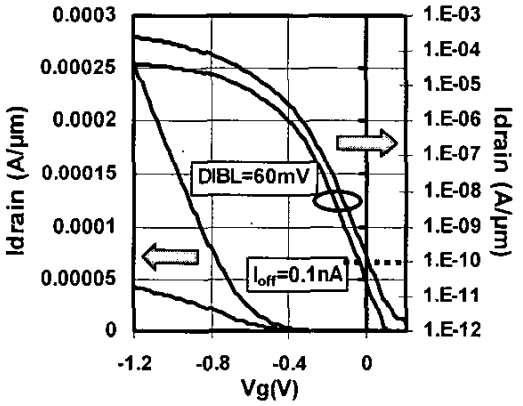

Fig.14: Lin-Id(Vg) and Log-Id(Vg) of a 55nm SON transistor with $CoSi_2$ gate. Data shows high SCE-resistive devices (DIBL=60mV) and thank to the Vth shift induced by the mid-gap gate, I_{off} is around 0.1nA/µm. The drive current is over 250µA/µm @-1.2V with T_{ox}=20Å and over 350µA/µm @-1.4V.

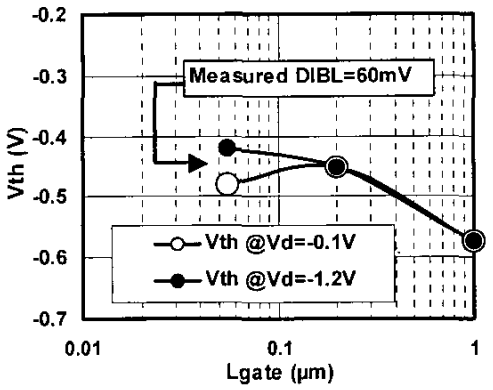

Fig.15: Measured Vth (@-0.1V&-1.2V) on SON devices with $CoSi_2$ gates. Roll-up occurs on the shortests devices due to pockets implantations that locally increase the Si-channel doping.

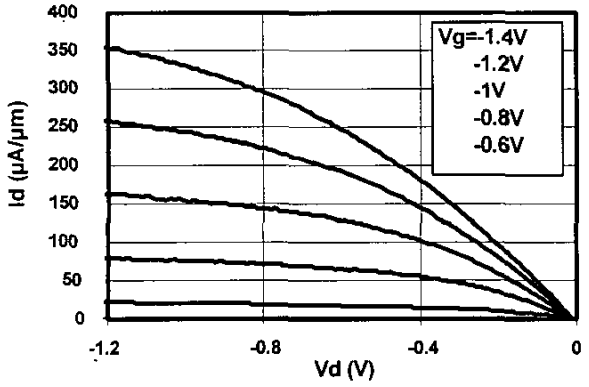

Fig.16: Lin-Id(Vd) of the 55nm SON transistor with $CoSi_2$ gate. Drive current as high as 350μA/μm is measured @Vg=-1.4V. Vdd=-1.4V is consistent with T_{ox}=20Å.

On figure 17, we made a comparison of SON devices with poly-Si and $CoSi_2$ gates, permitting us to conclude that the use of a midgap gate for V_{th} adjustement on extremely thin Si-film leads to more than 4 decades of I_{off} reduction, maintaining very good Ion≈250μA/μm @-1.2V or 350μA/μm @ -1.4V.

Alternative strategy consisting in equivalent I_{off} reduction due to strong channel doping (with poly gate) leads to very degraded mobility and to a loss of 25% in drive current (Ion=195μA/μm @-1.2V as shown by 2D simulations calibrated on the electrical data, fig.18).

Conclusions

Totally $CoSi_2$ silicided gates were successfully integrated on SON MOSFETs for the first time, with extremely thin (5nm) Si-conduction channel. Advantages of the midgap gates integration have been presented (V_{th} adjustment for thin FD films, polydepletion reduction) and demonstrated on highly performant SON PMOS devices (350μA/μm I_{on} with only 0.1nA I_{off} @-1.4V with T_{ox}=20Å). This technique can be a solution for the integration of very thin SON films for the ULSI area, and may be interesting for low leakage and highly performant devices. Note that total gate silicidation can also be performed on FD-SOI devices with elevated SD.

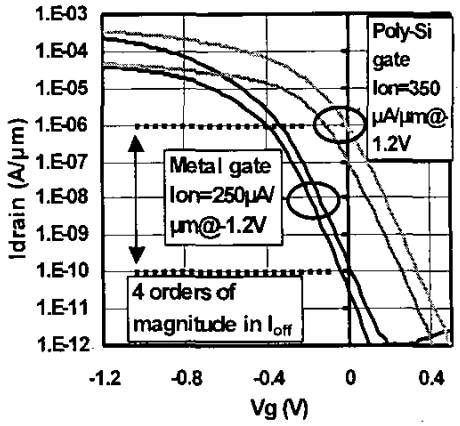

Fig.17: Comparison of Log-Id(Vg) curves of 55nm SON devices with poly-Si gate and $CoSi_2$ gate. Due to the very thin depletion depth (T_{Si}=5nm), the low threshold voltage of the transistor with poly-Si gate leads to high I_{off} that can be reduced by 4 orders by adjusting V_{th} with the mid-gap gate.

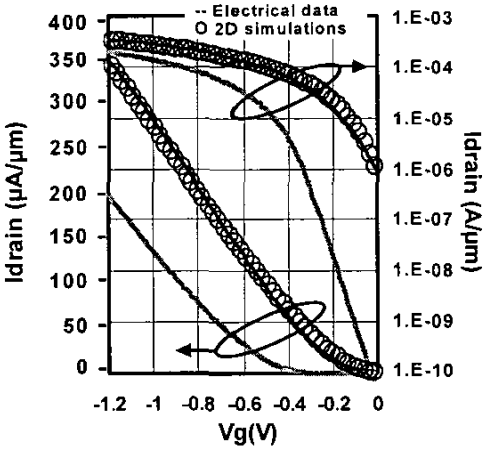

Fig.18: Calibration of 2D simulations (SON with poly-Si gate, open circles) on our electrical data(black lines). Next the simulations have been extended to the case of poly gate (gray lines) with adjusted I_{off}=0.1nA/μm by means of increased doping (Nch=6.5x$10^{18}$$cm^{-3}$). The corresponding Ion=195μA/μm is 25% lower than the 250μA/μm obtained with $CoSi_2$ gate (@-1.2V).

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