## 26.1 A 90nm 1.8V 512Mb Diode-Switch PRAM with 266MB/s Read Throughput

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Phase change random access memory (PRAM) is one of the most promising candidates that can overcome the performance and scalability limits of currently dominant flash memories [1-3]. The cell size of the MOS-switch PRAM is limited by a large amount of write current to melt the phase-change storage material ($Ge_2Sb_2Te_5$). To reduce the cell size without loss of current driving capability, a diode-switch PRAM has been presented [4]. The vertical diode switch using selective-epitaxial-growth (SEG) technology makes it possible to achieve not only minimum cell size but also disturbance-free operation. Figure 26.1.1 shows the diode-switch PRAM cell using SEG. In terms of cell size, the diode-switch PRAM is the smallest PRAM cell developed in recent years [1-3]. Even though the diode-switch PRAM makes it possible to achieve higher density, careful approach is necessary in designing cell array and corresponding periphery circuitry in a way that minimizes any parasitic effect such as vertical and lateral bipolar junction transistor (BJT) formations, and thermal crosstalk disturbance [4]. This paper presents a diode-switch PRAM with an optimized core structure and write/read control techniques for the diode-switch cells.

The 512Mb PRAM is configured as 16 banks of 32Mb, with each bank consisting of 8 blocks. Each block is built with 1024 wordlines and 4096 bitlines. Through global bitlines (GBL) using metal 3, local bitlines (LBL) of all blocks are connected, which helps the PRAM to have higher chip efficiency. Each block is divided into 4 I/O-blocks for write operation. Each I/O-block is built with 1024 wordlines and 1024 bitlines, and one I/O-block is subdivided into 8 sub-blocks for burst read operation. Each sub-block is composed of 1024 wordlines and 128 bitlines. To minimize ground bounce along the wordline during write operation, data of maximum four bits are written within an I/O-block. The number of the simultaneously activated I/O-blocks is adjusted corresponding to the division-write modes of ×2, ×4, ×8, and ×16. During burst read operation, the 32 sub-blocks in a block are activated simultaneously to pre-fetch 8 word data from cell arrays. By pre-fetching 8-word simultaneously, 266MB/s data rates are achieved.

Since the diode-switch PRAM cells are 2-terminal devices, unlike MOS-switch PRAM cells, they have higher operation voltage for write and read than the MOS-switch PRAM due to built-in potential of a diode switch, as shown in Fig. 26.1.1. They also have more parasitic effects such as vertical and lateral leakage current formations. Fig. 26.1.2 shows the optimal core configuration used to overcome these problems for the diode-switch PRAM. Unselected wordlines are set to a $V_{DD}$ + 1V or $V_{DD}$ + 2V level according to the operation mode to turn off unselected diodes. Floating bitlines (FBL) are used on unselected bitlines, which reduces leakage current and parasitic effects in the normal write and read operation mode. To develop selected cell data with enough voltage margin, section datalines (SDL) are precharged up to $V_{PPSA}$ level, a boosted voltage level from the $V_{DD}$ power-supply level. The precharge process of SDLs is performed through a two-step precharge method that makes eliminates the need for charge pumps. In the first step, SDLs are precharged to $V_{DD}$, and then they are precharged to the $V_{PPSA}$ level. After finishing the precharge of SDL nodes, cell data are developed through a PMOS transistor with nPBIAS signal activated, which provides read cell current to guarantee read disturbance. Write drivers provide optimum current values and pulse shape for SET or RESET data per cell through a write verify scheme which improves distribution and reliability of cell data.

Arbitrary slow-quench (ASQ) waveforms for better SET data distribution are generated through a slow-quench (SQ) pulse shaper, as shown in Fig. 26.1.3. Since it has wide operating range of almost $V_{DD}$, it provides versatile ASQ waveforms with maximum and minimum current values specified. This scheme is used to improve distributions and reliability of cell data through write verify process. Single pulse sequences are provided for the RESET data, and multiple step-down pulse sequence are provided for the SET data during the write verify loops.

Figure 26.1.4 shows a charge pump system to cope with higher operating voltage than the MOS-switch PRAM [1]. The $V_{PPSA}$ voltage level is the basic voltage for write and read operations. In case of the MOS-switch PRAM, the $V_{DD}$ voltage level is basic voltage for write and read operations [1]. The $V_{PPSA}$ voltage level is higher than the $V_{DD}$ power supply by about 1V to account for the built-in potential of the diode switch, as previously mentioned. Although the charge pump supplies the $V_{PPSA}$ voltage level during standby mode, the oscillation period of charge pump circuits is enlarged so much as to meet target of standby current. In read operation modes, the voltage levels of $V_{PPX}$ for X-decoders, $V_{PPY}$ for Y-decoders, $V_{PPWD}$ for write drivers, and $V_{PPSA}$ for sense amplifiers are all boosted up to $V_{PPSA}$ level of $V_{DD}$ + 1. In write operation modes, $V_{PPX}$, $V_{PPY}$, $V_{PPWD}$, and $V_{PPSA}$ levels are boosted to $V_{DD}$ + 2V, $V_{DD}$ + 3V, $V_{DD}$ + 3V, and $V_{DD}$ + 1V, respectively, as detaled in Fig. 26.1.4. Current consumption of the charge pump system is about 40 mA the worst case condition of a RWW operation.

The diode-switch PRAM provides write operation modes such as ×2, ×4, and ×8 division-write for low power mobile systems [1]. The write modes are selected according to required maximum current specifications. The PRAM draws about 25mA current in the ×2 division-write mode, where the write current value for RESET data is from 0.6 to 1mA and the pump efficiency during write operation is about 20%. Since the division-write modes lead to increase write time [1], our PRAM provides a ×16 accelerated write mode to increase write throughput. This mode increases write throughput without increasing current consumption because the write current is supplied by an external pin instead of internal pump circuits. Figure 16.1.5 plots measured data showing the effect of write pulse width on the distributions of SET and RESET resistances. To discriminate between SET data and RESET data during a read operation, at least a 400ns SET pulse width of SQ is required and a 50ns RESET pulse width is also necessary. The throughput of the write operation is 0.58 MB/sec when operated in ×2 division-write mode, and increases to 4.64 MB/sec in ×16 accelerated write mode.

Shmoo plots in Fig. 26.1.6 show test results from a 512Mb prototype chip. The initial access time, $t_{IAA}$, is 78ns and the burst access time, valid-clock-to-output-delay, $t_{BA}$, is 8ns at 1.8V, room temperature, and 133MHz synchronous burst read mode. Figure. 26.1.7 shows a chip micrograph of the 512Mb diode-switch PRAM, fabricated in a 3M 90nm CMOS process. The chip size is 91.5mm$^2$ with a unit cell size of 0.0467μm$^2$.

*References:*

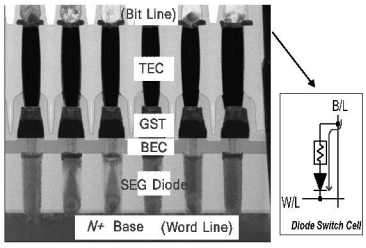
[1] S. Kang, W. Cho, B.-H. Cho, et al., "A 0.1μm 1.8V 256Mb 66MHz Synchronous Burst PRAM", *ISSCC, Dig. Tech. Papers*, pp. 140-141, Feb., 2006.

[2] H.-R. Oh, B.-H. Cho, W.-Y. Cho, et al., "Enhanced Write Performance of a 64Mb Phase-Change Random Access Memory", *ISSCC, Dig. Tech. Papers*, pp. 48-49, Feb., 2005.

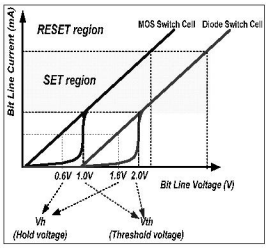
[3] F. Pellizzer, A. Benvenuti, B. Gleixner, et al., "A 90nm Phase Change Memory Technology for Stand-Alone Non-Volatile Memory Application", *Symp. VLSI Technology*, pp. 150-151, Jun., 2006.

[4] J.H. Oh, J.H. Park, Y.S. Lim, et al, "Full Integration of Highly Manufacturable 512Mb PRAM based on 90nm Technology", to appear in *IEDM Tech. Dig.*, Dec., 2006.




Vertical view of PRAM cells.




I-V characteristic curve of PRAM cells.

Figure 26.1.1: Diode-switch PRAM cell.

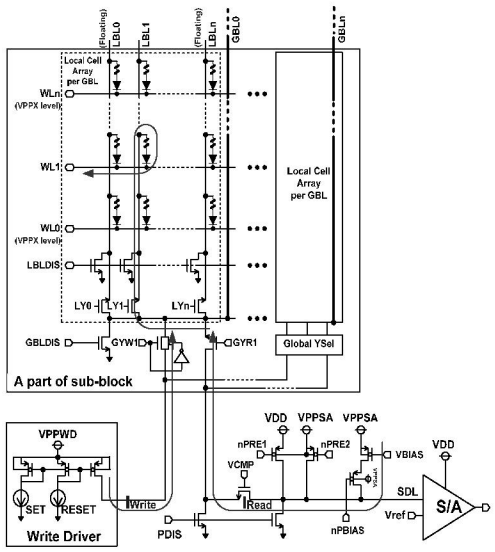
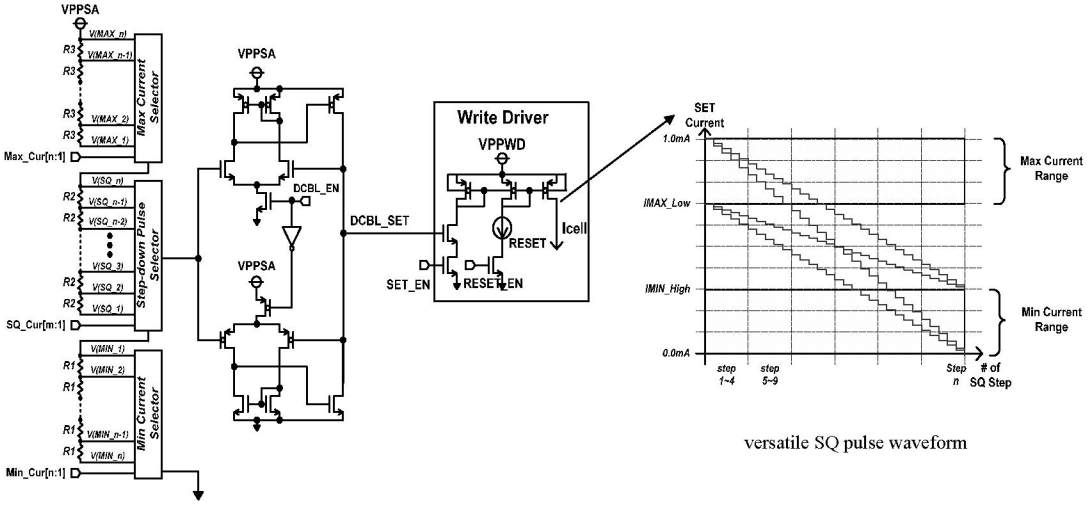


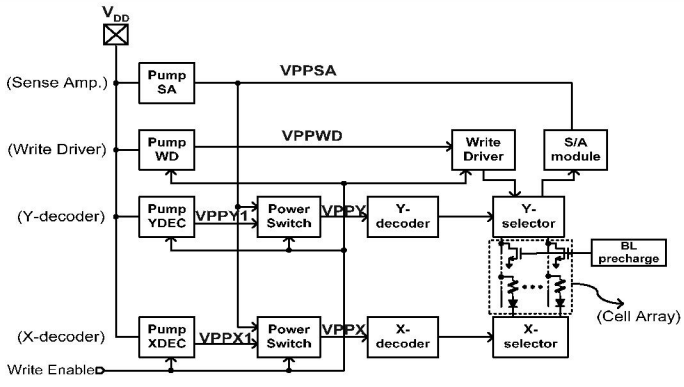

Figure 26.1.2: Core configuration with diode-switch PRAM cells.




Slow Quench pulse shaper circuit

versatile SQ pulse waveform

Figure 26.1.3: Slow quench pulse shaper.




| | Stand-by mode | Read mode | Write mode |
|---|---|---|---|
| VPPSA | VDD+1V | VDD+1V | VDD+1V |
| VPPWD | VPPSA | VPPSA | VDD+3V |
| VPPY1 | VPPSA | VPPSA | VDD+3V |
| VPPY | VPPSA | VPPSA | VDD+3V |
| VPPX1 | VPPSA | VPPSA | VDD+2V |
| VPPX | VPPSA | VPPSA | VDD+2V |

Figure 26.1.4: Charge-pump system for the diode-switch PRAM.

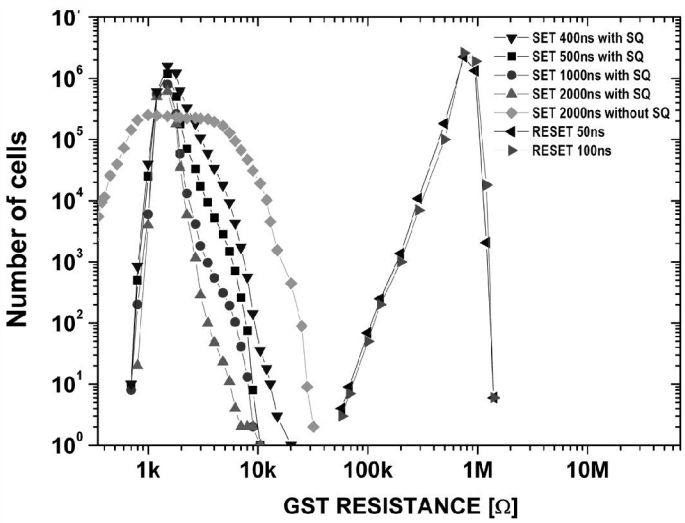



Figure 26.1.5: Distributions of GST cell resistances with varied duration of RESET/SET pulses, obtained with 4Mb sampled data.

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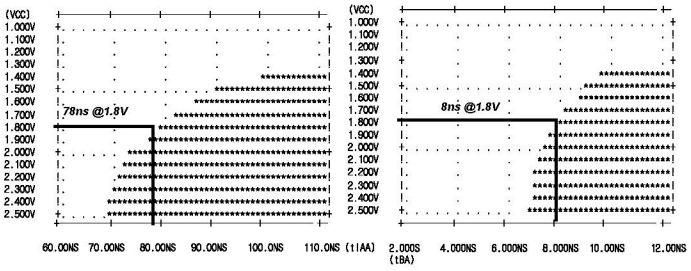


Figure 26.1.6: Shmoo plots for inital access time ($t_{IAA}$) and burst access time ($t_{BA}$).

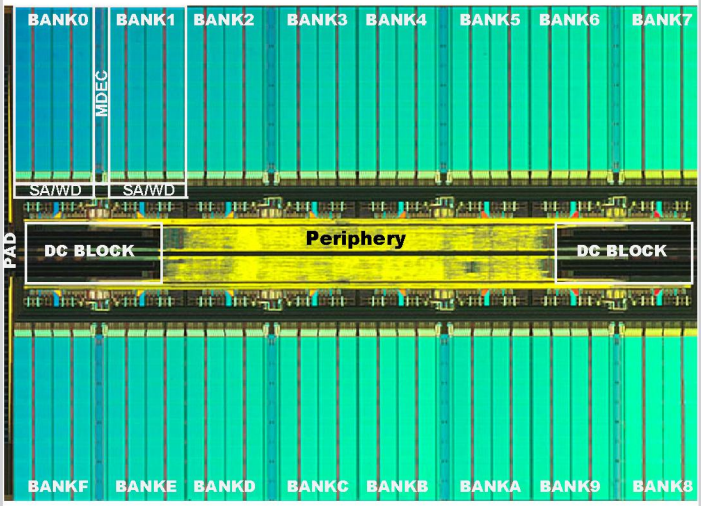


Figure 26.1.7: Micrograph of the fabricated 512Mb PRAM chip.

 