Dual work function phase controlled Ni-FUSI CMOS (NiSi NMOS, Ni_2Si or $Ni_{31}Si_{12}$ PMOS): Manufacturability, Reliability & Process Window Improvement by Sacrificial SiGe cap

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Abstract

This work presents the first comprehensive evaluation of the manufacturability and reliability of dual WF phase controlled Ni-FUSI/HfSiON CMOS (NMOS: NiSi; PMOS: Ni_2Si and $Ni_{31}Si_{12}$ evaluated) for the 45 nm node. RTP1 and poly/spacer height were identified as the most critical process control parameters in our flow. We demonstrate that a novel sacrificial SiGe cap addition to the flow (improved poly-Si/spacer height control) opens the RTP1 process window from ~5°C to ~20°C for gate lengths down to 45nm, making scalable dual WF CMOS Ni-FUSI manufacturable. We demonstrate Vt control with σ~19mV (including wafer to wafer variation, N=1000, 45 nm devices) for NMOS (NiSi), and σ~21mV for PMOS. TDDB and NBTI reliability evaluation of NiSi and, for the first time, of Ni_2Si and $Ni_{31}Si_{12}$ was done. ~1V or larger operating voltages (V_{op}) were extrapolated for a 10 years lifetime. Using a higher back-end thermal budget showed no reliability degradation.

Introduction

Ni FUSI/HfSiON gates are one of the main metal gate candidates for scaled CMOS technologies [1-7]. In our previous work [6] we presented a simple, CMP-based, dual WF CMOS integration scheme (NMOS: NiSi; PMOS: Ni-rich silicide) with simultaneous full silicidation of NMOS and PMOS gates and poly etch-back on PMOS. For implementation into manufacturing, process control, process window (PW) and reliability become key decision criteria. This work presents a comprehensive evaluation of the manufacturability and reliability of this integration scheme and a novel method to improve the PW by the use of a sacrificial SiGe cap.

Process integration

MOSFET devices with Ni FUSI/HfSiON gates were fabricated using a CMP based, 2-step RTP FUSI CMOS flow [6] that achieves NiSi on NMOS and Ni-rich silicide on PMOS by selective poly-etch back on PMOS (Fig. 1). In the standard flow, poly-Si and spacer heights are not well controlled before FUSI due to non-uniformity in the CMP process and the need for over etch at oxide etch-back (Figs. 1, 2). This is eliminated by a novel SiGe cap process (Fig. 1). A sacrificial SiGe cap is deposited on the poly-Si film, in order to absorb the process variability that only affects the SiGe cap thickness, leaving the thickness of the poly-Si (t_{Si})below intact. The SiGe layer is then removed selectively to poly-Si and spacers, leaving a well controlled poly-Si and spacer height (no spacer recess with respect to poly-Si). This is critical for linewidth independent phase and Vt control (control of effective Ni/Si ratio) [5] and for manufacturability as shown in the next section. Poly-Si etch-back was then performed selectively on PMOS to reduce poly-Si height to 50 and 30 nm for devices targeting Ni_2Si and $Ni_{31}Si_{12}$, respectively. The SiGe cap process resulted in significant expansion of the RTP1 PW (Fig. 3) and re-centering of the RTP1 temperature to slightly higher values making the process compatible with both Ni_2Si (50 nm poly-Si) and $Ni_{31}Si_{12}$ (30 nm poly-Si) on PMOS (Fig. 4). Processing was completed with one level metal (PMD at 400°C or 550°C) and sinter (420°C 20 min).

Results and discussion

To assess manufacturability and process window for dual WF CMOS, the sensitivity throughout the flow to process variables was studied systematically. The main issue limiting process window was found to be linewidth independent NiSi FUSI phase formation on NMOS devices. Poly-Si/spacer height and RTP1 conditions were found to be the most critical variables, controlling the effective Ni-Si ratio and silicide phase on NMOS devices: At low RTP1 temperatures (T), not enough Ni is reacted and the gates remain under-silicided (poly-Si gates). For high RTP1 temperatures, Ni diffuses from areas surrounding the gates, too much Ni is reacted on small devices, and the growing Ni-rich silicide can reach the dielectric interface resulting in a Ni-rich (over-silicided) FUSI gate [5]. Uniformity of poly-Si and spacer height is critical to ensure uniform Ni-Si reacted ratios. Recessed spacers or lower poly-Si height can result in Ni-rich FUSI gates at lower RTP1 temperatures, for which taller gates (or spacers) may end up under-silicided, reducing or eliminating the PW for NiSi FUSI. Figs. 5 and 6 show the RTP1 T PW (30s) obtained for Lgate down to ~40 nm, and the deposited t_{Si} PW. The novel SiGe cap flow leads to a PW increase from ~5°C to ~20°C. At low RTP1 T, gates are under-silicided (poly-Si gate behavior) showing larger CET and ~1 order of magnitude lower gate leakage in accumulation. For increasing RTP1 T, NiSi FUSI gates are obtained. At higher T, over-silicidation of small devices results in bimodal Vt distribution (NiSi and Ni-rich FUSI, the later with higher Vt). The t_{Si} PW of ~10nm for NiSi FUSI was obtained at fixed RTP1 $T=T_0$, with the standard process. SiGe cap layer flows should not significantly suffer from process fluctuations due to Δt_{Si} variations, since t_{Si} before FUSI = t_{Si} as-deposited. In a standard flow, however, as shown in Fig. 2, up to $\Delta t_{Si} \approx 14\%$ can occur within wafer, before Ni deposition for FUSI. Vt uniformity within wafer for ≈50nm devices is show in Fig. 7 for 2 RTP1 temperatures (Δ=10°C). SiGe cap devices have tight distributions (σ~15-18 mV); for the standard flow, the 10°C increase is enough to cause Vt splitting at these gate lengths (bimodal distribution) (see also Fig. 8). Fig. 9 shows a well behaved NMOS ITP characteristics at RTP1 $T=T_0$ (standard flow). For other RTP1 Ts, if under or over-silicidation occurs, there is considerable drive loss. Interestingly, FUSI devices showed improved performance with rising RTP1 T (Fig.9, right).

On the PMOS side, Fig. 10 shows well-behaved ITP characteristics for $Ni_{31}Si_{12}$ FUSI devices at RTP1 $T=T_0$. Tight Vt distributions were obtained for Ni_2Si and for $Ni_{31}Si_{12}$ FUSI phases (σ~16-21mV). ΔVt~60mV at ~50nm gate lengths between the 2 phases is in agreement with measured WF (Fig. 3).

NBTI was evaluated on Ni FUSI/HfSiON (CET~1.6 nm) devices for NiSi, and for Ni_2Si and $Ni_{31}Si_{12}$ (Fig. 11). Increasing the Ni content in Ni_xSi FUSI leads to a small V_{op} decrease for ΔV_T = 30 mV. For a 10 years lifetime, values ~0.9-1V were extrapolated. No impact of a higher PMD temperature (550°C *vs.* 400°C) was found for NBTI of Ni_2Si FUSI devices. TDDB was also evaluated (Fig. 12), using a 1 μA abrupt current increase as criterion for breakdown detection. For NMOS, V_{op}~1.0V was obtained for a 10 years lifetime, with also no degradation for 550°C *vs.* 400°C PMD devices. For PMOS, V_{op} >1.2 V was extrapolated for $Ni_{31}Si_{12}$ FUSI, with no degradation compared to poly-Si devices (same deposited HfSiON, resulting in ~3Å thinner EOT for FUSI devices).

Conclusions

A comprehensive manufacturability and reliability assessment of Ni FUSI gates was presented. NiSi FUSI RTP1 T process window (PW) can be improved from ~ 5 to 20 °C, for down to 45nm gate lengths, using a new integration process with a SiGe sacrificial cap layer. From NBTI and TDDB, for a 10 years lifetime, V_{op} near or > 1.0V was extrapolated for NMOS and PMOS devices with controlled NiSi and $Ni_{31}Si_{12}$ or Ni_2Si FUSI gates, respectively.

References

[1] B. Tavel *et al.*, IEDM Tech. Dig., 825 (2001); [2] J. Kedzierski *et al.*, IEDM Tech. Dig., 247 (2002); [3] A. Veloso *et al.*, IEDM Tech. Dig., 855 (2004); [4] K. Takahashi *et al.*, IEDM Tech. Dig., 91 (2004); [5] J. A. Kittl *et al.*, Symp. VLSI Tech., 72 (2005); [6] A. Lauwers *et al.*, IEDM Tech. Dig., 661 (2005); [7] P. Ranade *et al.*, IEDM Tech. Dig., 227 (2005).

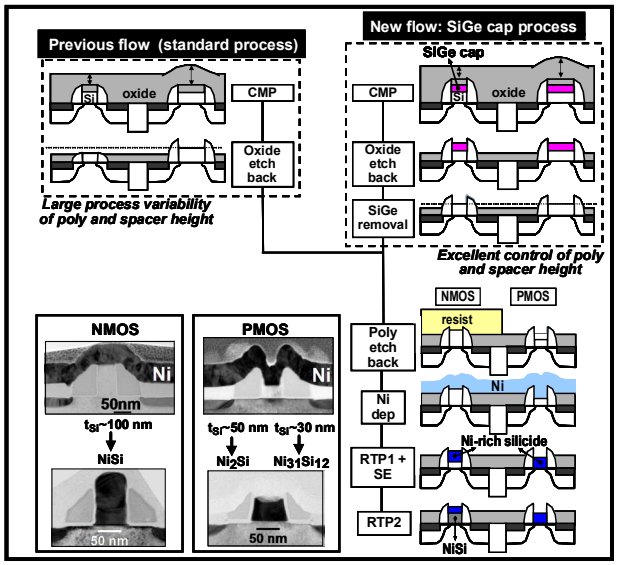

Fig.1 – Schematics of the CMOS integration flows of this work. A new process with SiGe sacrificial cap layer gives excellent control of the poly-Si and spacers height, key parameters for the NiSi FUSI process window (PW). $Ni_{31}Si_{12}$ and Ni_2Si FUSI were evaluated for PMOS.

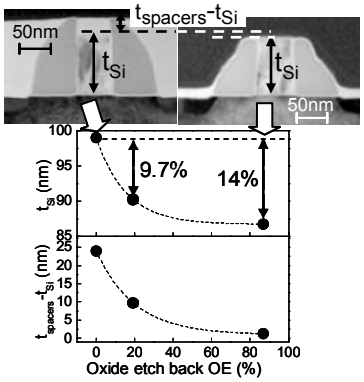

Fig.2 – Impact on the poly and spacers of the over-etch (OE) used in the oxide etch back before FUSI.

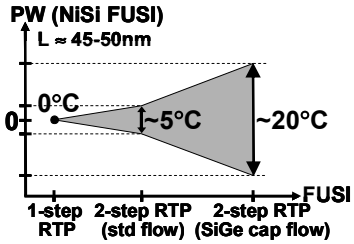

Fig.3 – NMOS RTP1 T PW for NiSi-FUSI for ~45nm devices. From no PW for a 1-step RTP process, PW is increased to ~5°C with a 2-step RTP and to ~20°C with SiGe cap flow.

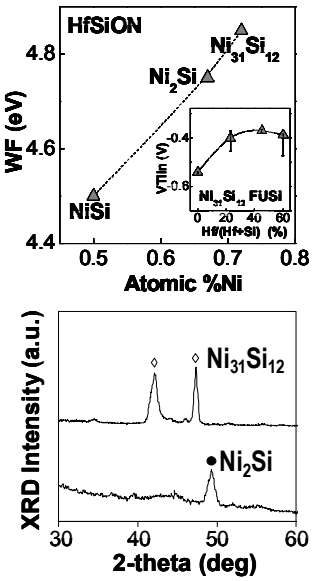

Fig.4 – WF for the main Ni silicide phases on Hf_xSiON (top). XRD analysis showed that Ni_2Si or $Ni_{31}Si_{12}$ can be obtained for 60nm Ni by adjusting the poly thickness or RTP1 conditions (bottom).

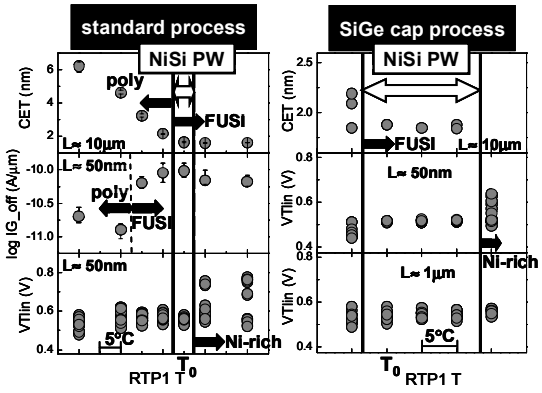

Fig.5 – Evaluation of NiSi FUSI RTP1 T PW. PW limits are defined by: incomplete silicidation < NiSi FUSI < over-silicidation (Ni-rich) of the gates. The use of SiGe cap increases the PW from ~5 to 20°C.

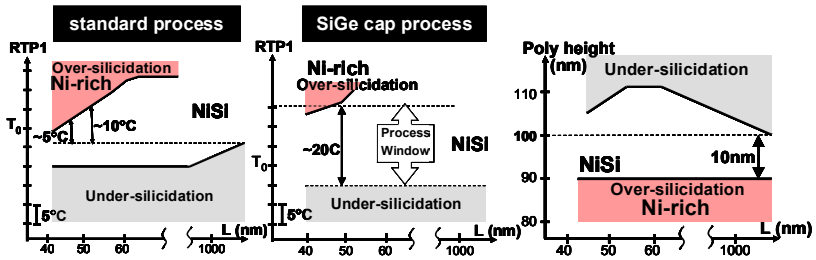

Fig.6 – NMOS RTP1 temperature PW for NiSi-FUSI for devices down to ~40nm gate lengths with the standard integration flow (left) and with SiGe cap flow (center). On the right plot, at RTP1 T=T_0, the NiSi FUSI t_{Si} PW is ~10nm poly height.

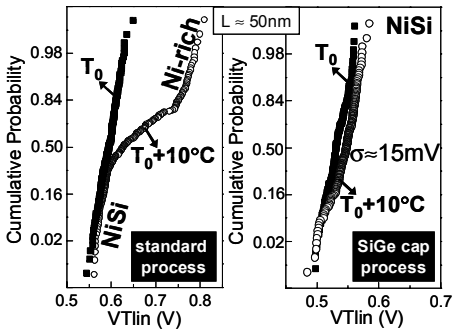

Fig.7 – NMOS Vt distributions for 2 RTP1 Ts using the standard flow (left) or the novel SiGe cap flow (right).

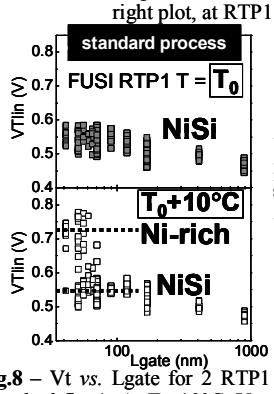

Fig.8 – Vt *vs.* Lgate for 2 RTP1 Ts (standard flow). At T_0+10°C, Vt split occurs for smaller NMOS devices.

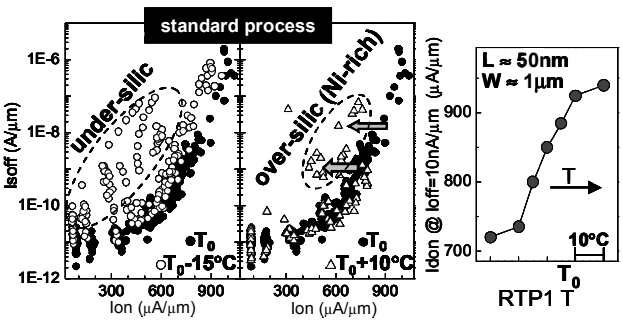

Fig.9 – NMOS ITP plots (standard flow). Incomplete silicidation/ over-silicidation of the gates ⇒ drive current (Ion) loss. For NiSi-FUSI devices,↑ FUSI RTP1 T ⇒ ↑Ion (right plot).

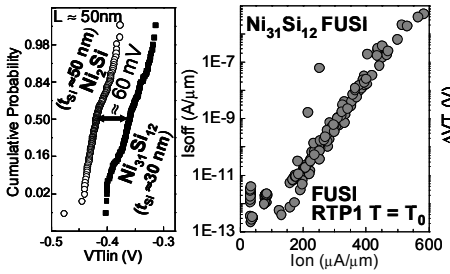

Fig.10 – Vt distributions for Ni_xSi FUSI. ITP characteristics of $Ni_{31}Si_{12}$ FUSI PMOS devices.

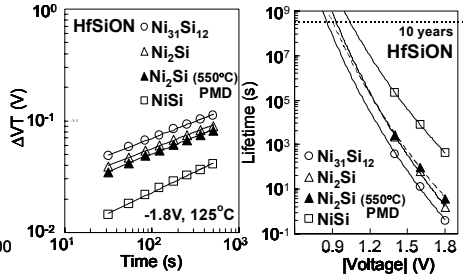

Fig.11 – NBTI comparing devices with different Ni FUSI phases.

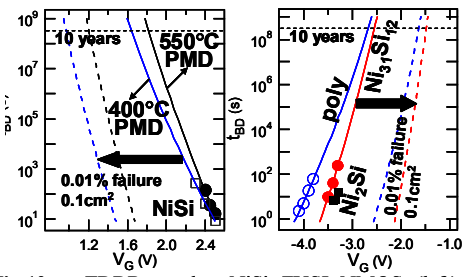

Fig.12 – TDDB results: NiSi FUSI NMOS (left); $Ni_{31}Si_{12}$ FUSI *vs.* poly gate PMOS (right).