A 65nm-node LSTP (Low Standby Power) Poly-Si/a-Si/HfSiON Transistor with High I_{on}-$I_{standby}$ Ratio and Reliability

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Abstract

We have newly developed poly-Si/a-Si/HfSiON (EOT=1.6nm) transistor that features high I_{on}-$I_{standby}$ ratio and reliability for 65nm-node LSTP (Low Standby Power) application.

By carefully optimizing halo implant condition, excellent I_{on}-$I_{standby}$ ($=I_g+I_{off}$) characteristics of I_{on}=520μA/$I_{standby}$=17pA (I_g=1.6pA, I_{off}= 15pA) at V_{dd}=1.2V are obtained, which is the highest ratio ever reported. In addition, we have newly introduced thin amorphous-Si layer between HfSiON and phosphorous-doped poly-Si gate -electrode for reliability enhancement, and confirmed that PBTI (positive bias temperature instability) lifetime improves by two orders of magnitude with no performance degradation. We believe this technology enables further device scaling of poly-Si/HfSiON structure.

Introduction

Low standby power (LSTP) devices are now indispensable for various mobile applications. Fig.1 shows the relation between I_g, GIDL and I_{on} as a function of EOT. In conventional LSTP using SiON gate dielectric, thick gate dielectrics and high channel doping are required for standby leakage ($I_{standby}$) suppression, which inevita -bly results in performance degradation as well as GIDL increase. Compared to SiON, high-K gate dielectric can achieve not only I_g reduction but also GIDL suppression because high threshold voltage (V_{th}) can be obtained with lower channel doping thanks to Fermi -pinning effect. High-K device is well-suited for LSTP because of these features. On the other hand, high-K gate dielectric is known to induce many issues such as V_{th} shift of P-MOSFET, mobility degradation, and reliability degradation. Up till now, V_{th} adjustment of P-MOSFET [1] and mobility improvement [2] have been reported. However, poly-Si /high-K detailed device level study has not yet been reported.

In this paper, we show the excellent I_{on}-$I_{standby}$ transistor characteristics obtained through process parameter optimization not only on high-K film formation, but also on other parameters involved in total transistor formation, namely, gate-electrode and halo implant. In addition, we propose the new method for reliability enhancement by means of "amorphous-Si (a-Si) layer insertion" between poly-Si gate-electrode and HfSiON and show the detailed device level study on this new structure.

Device performance

In order to investigate the superiority of HfSiON over SiON for LSTP, we prepared HfSiON (EOT=1.6nm) device and two SiON devices : SiON-1 (EOT=2.2nm) with sufficiently thick dielectric so that I_g is suppressed to comparable value as I_{off}, SiON-2 (EOT=1.6nm) with the same EOT as HfSiON. Fig.2 shows I_d-V_g characteristics of both SiON and HfSiON devices. In the case of SiON-1, thicker dielectric degrades on-current. On the other hand, in SiON-2, thinner dielectric drastically increases I_g. Moreover, GIDL significantly increases due to higher channel doping and vertical electric field. Compared to SiON devices, HfSiON device can achieve not only I_g reduction, but also GIDL suppression due to low channel doping resulting from Fermi-pinning effect. Fig.3 shows the comparisons of GIDL dependence on halo dosage between SiON and HfSiON devices. GIDL of HfSiON device is one order of magnitude smaller than that of SiON device. Higher halo dosage can be applied for HfSiON device because of low GIDL, and this can be exploited for short-channel effect suppression and device scaling.

Mobility is an important parameter for high I_{on}. Fig.4 shows the comparison of effective electron mobility between SiON and HfSiON devices. HfSiON device in this work achieved high effective electron mobility comparable to SiON device. Fig.5 shows I_{on}-I_{off} characteristics of HfSiON and SiON devices. Because of reduced I_g and GIDL, HfSiON device exhibits excellent I_{on}-I_{off} characteristic compared with SiON device. Table.1 shows the summary of device performances. We have achieved I_{on}=520μA with $I_{standby}$=17pA at V_{dd}=1.2V, which is the highest $I_{on}/I_{standby}$ ratio ever reported for poly-Si/high-K device.

HfSiON device reliability improvement

Phosphorus (P) doping into gate-electrode is required for suppressing gate depletion effect and increasing inversion-mode capacitance. However, in the case of high-K dielectrics, many researchers have reported concerns on reliability degradation caused by the impurities diffusion from gate-electrode and the reaction at poly-Si/high-K interface [4,5]. Fig.6 shows the influence of phosphorus diffusion from poly-Si gate-electrode. I_g drastically increases with higher phosphorus concentration in poly-Si gate -electrode. This is because phosphorus forms trap-sites in HfSiON, and degrades the film integrity. In conventional poly-Si/HfSiON structure, it has been a trade-off between performance (increased inversion capacitance) and poor dielectric film reliability.

We have devised a new process flow with which high reliability can be achieved without performance degradation. Fig.7:B) shows the process flow and proposed gate-electrode structure, which features thin amorphous-Si layer deposition on HfSiON prior to poly-Si deposition. Fig.7:A) shows the conventional flow. Test samples were fabricated for both A) poly-Si/HfSiON and B) poly-Si/a-Si/HfSiON and evaluated. Although gate depletion effect was of concern in case of poly-Si/a-Si/HfSiON, we have confirmed that optimizing a-Si layer thickness can effectively prevent the degradation of inversion-mode capacitance (Fig.8). Large area capacitor I_g distribution, an index for the dielectric film reliability, is shown in Fig.9. Poly-Si/a-Si gate-electrode tightens I_g distribution spread. V_{th} dependence on phosphorus dosage is shown in Fig.10. Although V_{th} is generally known to increase by phosphorus induced fixed-charge [5], no V_{th} increase was observed in poly-Si/a-Si/HfSiON. Also, compared with poly-Si/HfSiON, 40% reduction in hysteresis is achieved (Fig.11). From these experimental results, we infer that thin amorphous-Si layer effectively suppresses the formation of phosphorus induced fixed-charge and trap-site.

The result of TDDB measurement is shown in Fig.12. Poly-Si/a-Si gate-electrode improves TDDB lifetime. PBTI lifetime, which is one of the greatest issues of high-K gate dielectric devices, is shown in Fig.13. Due to phosphorus induced trap-sites suppression, poly-Si/a-Si gate-electrode improves PBTI lifetime by two orders of magnitude. These results show that highly reliable device can be obtained by using optimized a-Si layer without performance degradation.

Conclusion

We have newly developed poly-Si/a-Si/HfSiON transistor for 65nm-node LSTP application. By carefully optimizing halo implant condition and using poly-Si/a-Si gate-electrode, we have obtained excellent I_{on}-$I_{standby}$ characteristics with high reliability.

References

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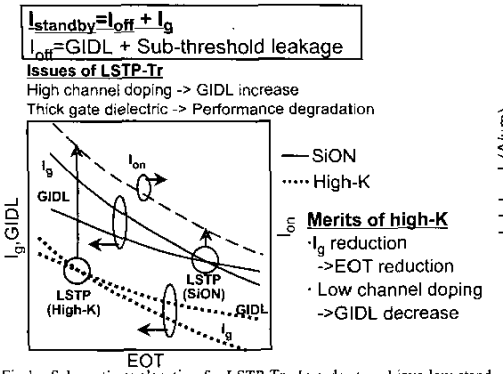

Fig.1 Schematic explanation for LSTP-Tr.. In order to achieve low stand-by leakage, it is necessary to suppress I_g and GIDL simultaneously. Compared to conventional SiON gate dielectric, both I_g and GIDL can be suppressed by using high-K gate dielectric.

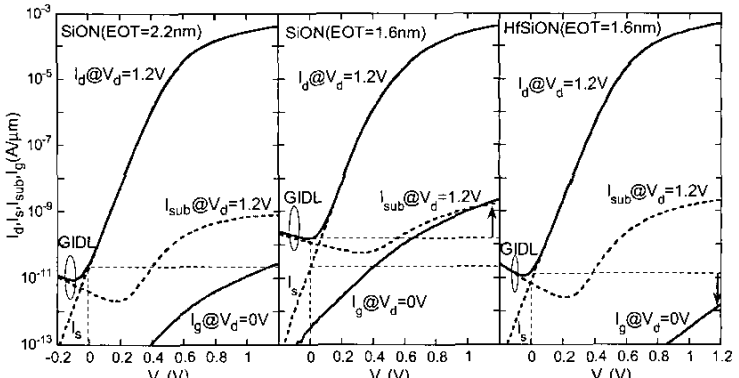

Fig.2 Sub-threshold and I_g characteristics with SiON(EOT=2.2nm,1.6nm) and HfSiON (EOT=1.6nm) gate dielectrics for 70nm(EOT=1.6nm) and 85nm(EOT=2.2nm) gate length.

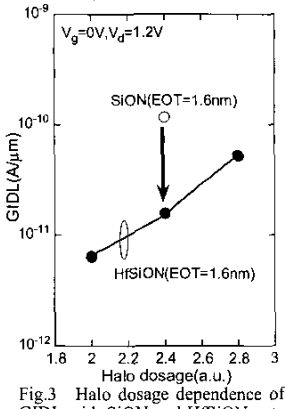

Fig.3 Halo dosage dependence of GIDL with SiON and HfSiON gate dielectrics.

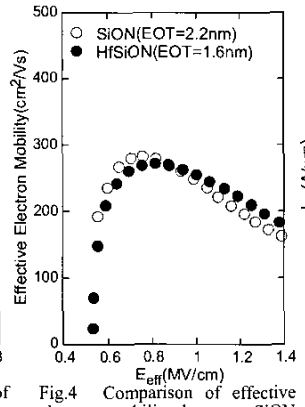

Fig.4 Comparison of effective electron mobility between SiON and HfSiON gate dielectrics.

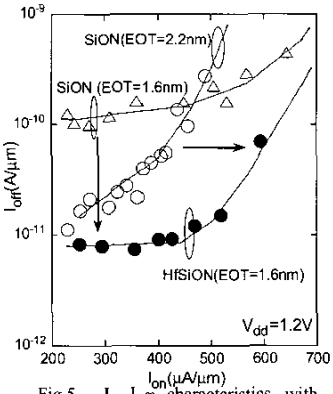

Fig.5 I_{on}-I_{off} characteristics with SiON and HfSiON gate dielectrics at V_{dd}=1.2V.

Table1 Summary of device performances with SiON and HfSiON gate dielectrics.

	SiON		This Work HfSiON	HfSiO Ref[1]	HfO_2 -Al_2O_3 Ref[6]
EOT (nm)	2.2	1.6	1.6	1.8	1.56
L_g (nm)	85	70	70	85	100
V_{dd} (V)	1.2	1.2	1.2	1.2	1.2
I_g (A/μm)	2.9E-11	2.4E-9	1.6E-12	4E-11	---
I_{on} (μA/μm)	361	448	520	469	470
I_{off} (A/μm)	2E-11	1.6E-10	1.5E-11	4.8E-12	1.0E-10
$I_{standby}$ (A/μm)	4.9E-11	2.6E-9	1.7E-11	4.5E-11	---

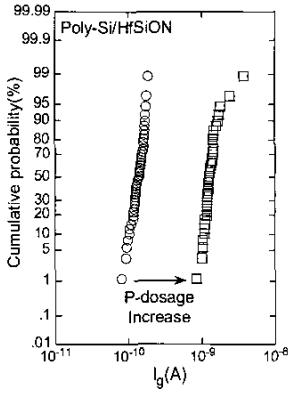

Fig.6 Phosphorus dosage dependence of gate leakage current with poly-Si gate-electrode at V_g=1V.

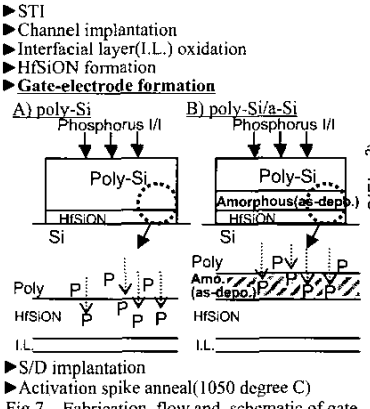

Fig.7 Fabrication flow and schematic of gate -electrode structure. As-deposited amorphous-Si layer suppresses phosphorus diffusion.

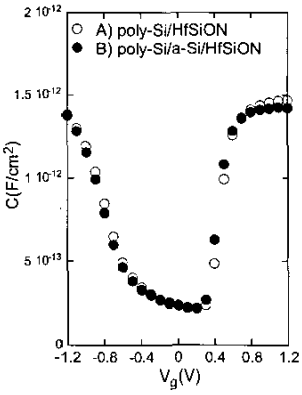

Fig.8 Comparison of C-V character -istics between A)poly-Si/HfSiON and B)poly-Si/a-Si.

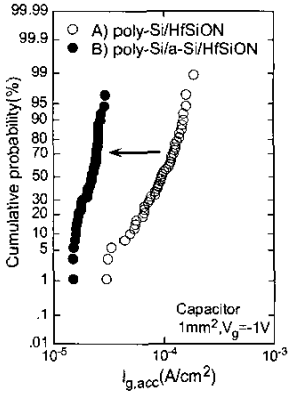

Fig.9 Accumulation gate leakage ($I_{g,acc}$) distributions of capacitor.

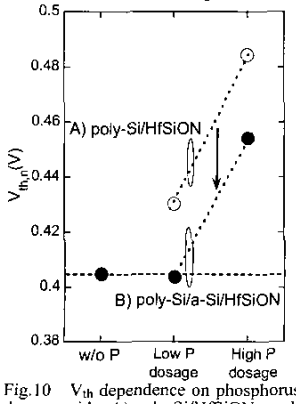

Fig.10 V_{th} dependence on phosphorus dosage with A) poly-Si/HfSiON and B) poly-Si/a-Si/HfSiON.

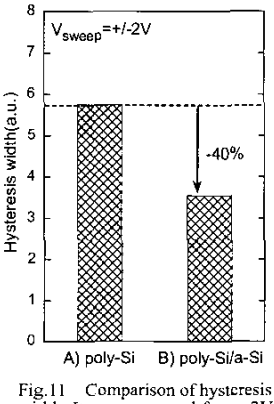

Fig.11 Comparison of hysteresis width. It was measured from -2V to 2V.

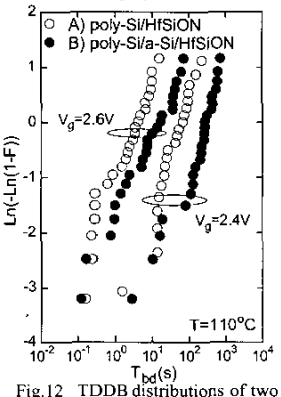

Fig.12 TDDB distributions of two different gate-electrode samples.

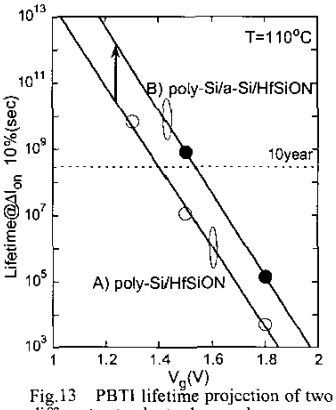

Fig.13 PBTI lifetime projection of two different gate-electrode samples.