Investigation of Gate Oxide Short in FinFETs and the Test Methods for FinFET SRAMs

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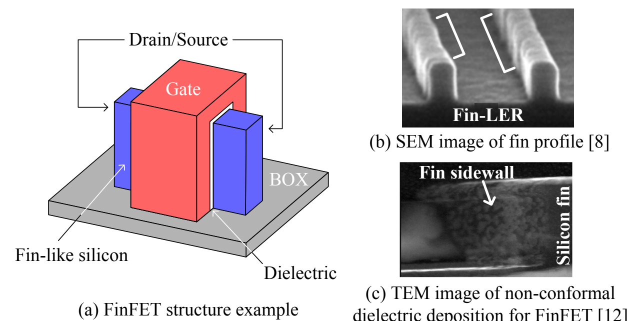
Abstract

When CMOS technologies enter nanometer scale, FinFET has become one of the most promising devices because of the superior electrical characteristics. Nonetheless, due to the scaling of dielectric thickness and the occurring of line-edge roughness, FinFETs may suffer the gate oxide short. Gate oxide short is a defect that has been widely discussed in planar bulk MOSFETs. But for FinFETs, the defect characteristics have not been studied yet. In this paper, we investigate the fault behaviors of the gate oxide short in FinFETs. The investigation includes both tied-gate and independent-gate FinFETs. Based on the TCAD mixed-mode simulations, we discover that the gate oxide short in the two types of FinFETs causes different fault behaviors from each other. Compared to planar bulk MOSFETs, the fault behaviors are even more complex. In addition to the discussion at device level, we also discuss the corresponding SRAM testing. For detecting gate oxide short in FinFET SRAMs, we propose two new test methods. By using TCAD transient simulations, we prove the two methods' test efficacy of detecting the gate oxide shorts uncovered by traditional test methods.

I. Introduction

As CMOS technology enters post-22nm era, FinFET becomes the promising device. This is because FinFET possesses the superior electrical characteristics such as reduced short channel effect, good sub-threshold slope, reduced random dopant fluctuation [1] [2], and high-speed performance [3]. The reason FinFET performs differently from the traditional planar bulk MOSFETs is that it utilizes a specific physical structure. As shown in Figure 1(a), an upright fin-like silicon with fin width of nanometer-scale forms the channel. While source and drain locate at the fin's alternative edges, the gate with its dielectric cover the fin sidewalls to control the channel's conductivity. In 2012, Intel has demonstrated the 22nm FinFET logics and SRAMs [4] [5], which almost claims the ready-to-deliver technology.

For FinFETs, one of the major-concerned issues is the fin line-edge roughness (Fin-LER) [6] [7] [8]. This phenomenon depicts the fin sidewalls of the device would be rough after process due to the limitation of lithography and etching. Figure 1(b) shows the SEM image of the silicon fin profile with Fin-LER. As a result, device's characteristics and performance would vary from each other. To mitigate the Fin-LER caused device variation, several solutions have been proposed [7] [9]. The techniques include adjusting devices' number of fins, controlling gate bias voltage, and considering sidewall surface (conducting channel) orientation. However, when the dielectric thickness of FinFETs is scaled to 1∼5nm [10] [11], and the non-conformal deposition of the dielectric layer is reported [12], the FinFET with Fin-LER suffers the poor insulator coverage at the sidewalls as shown in Figure 1(c). The gate oxide short defects may consequently occur [13] [14].



(a) FinFET structure example

(b) SEM image of fin profile [8]

(c) TEM image of non-conformal dielectric deposition for FinFET [12]

Fig. 1. **FinFET structure and images of the manufacture defects.**

Gate oxide short (GOS) is a defect that has been widely discussed in planar bulk MOSFETs. In addition to the defect mechanism mentioned in the previous paragraph, the GOS defect can also be induced by voltage stress, lithographic particles, or unexpectedly large gate tunneling leakage [13] [15]. The GOS used to be classified into two types: gate-to-source/drain short and gate-to-channel short. The first type depicts the shorting between gate and source/drain and was usually modeled by a resistive short between them. We do not include this type into our discussion for two reasons. Firstly, for FinFETs, only the devices with overlapped gate-source/drain have chance to suffer the defect. In the devices with underlapped gate-source/drain, the defect rarely appears. Secondly, even for the overlap-type FinFETs, the gate-to-source/drain GOS modeled by a resistance short actually behaves the same as a simple node-to-node short. Since previous works [16] [17] have already studied the node-to-node shorts for FinFET logics, the corresponding fault behaviors can be quickly referred and hence need no more discussion. We focus on the second type of GOS: gate-to-channel short. The gate-to-channel GOS causes a low impedance from gate to the silicon channel. The corresponding fault behavior is more complex. In planar bulk MOSFETs, many works of defect modeling [18] [19] and testing [14] [20] [21] have been published. But for FinFETs, the related research paper has not been seen yet to the best of our knowledge.

In this paper, we investigate the gate-to-channel GOS (will be abbreviated to only GOS in the following contents) in FinFETs by using the TCAD mixed-mode simulations. Firstly, we build defect-free FinFETs in the TCAD 3D environment. Based on the built devices, we inject the GOS defect and extract the corresponding faulty characteristics. By comparing the electrical I-V curves of the defective FinFETs and the defect-free ones, we show how the GOS affects the FinFETs. In addition, we also illustrate and explain the fault behavior difference between FinFETs and planar bulk MOSFETs. Finally, following the above studies, we discuss the corresponding SRAM testing. For detecting GOS in FinFET SRAMs, we introduce

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two new test methods. One is for tied-gate FinFET based SRAM, and the other is for independent-gate FinFET based one. The test efficacy of both the methods is proved by applying TCAD transient simulations.

II. GOS Fault Behaviors in Planar Bulk MOSFETs

In this section, we briefly review the fault behaviors when GOS occurs in the planar bulk MOSFETs. As reported [13] [22], GOS affects the devices in three aspects. The first one is decreasing the saturation drain current. Due to the defect, the channel inversion becomes weak and the drive ability of the device is accordingly reduced. Secondly, when the drain voltage is low, there will be a negative drain current. The current comes from the gate leakage current flowing through the GOS to the drain. As to the last, the total gate leakage current increases exponentially with the increasing of gate voltage. Below are their summarizations.

- Decreased saturation drain current ($I_{D(SAT)}$)
- Negative drain current at low drain voltage
- Gate voltage dependent gate leakage current

The three fault behaviors are usually demonstrated by the device's IDVD figure. Figure 2 shows the example. Figure 2(a) is the IDVD of a defect-free planar bulk nMOS with VDD=1.2 volt. Figure 2(b) belongs to the same device but with GOS on the contrary. When comparing the right hand sides of the two figures, firstly the "Decreased $I_{D(SAT)}$" occurs obviously. As to the "Negative $I_{D(low\,V_D)}$", it appears at the left hand side of Figure 2(b) when being compared to Figure 2(a). The third fault behavior "Leakage I_G" is not directly shown in the figures. However, it can be implied by the negative $I_{D(V_D=0)}$ which increases exponentially with V_G.

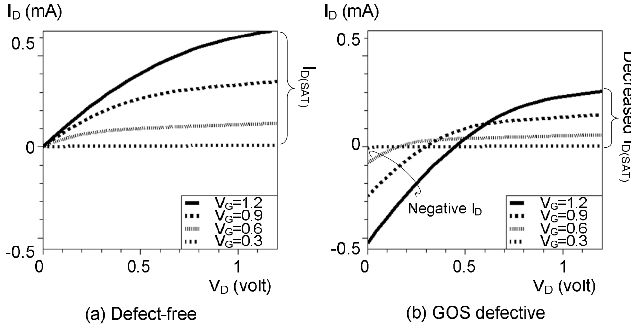

Fig. 2. **IDVD curves of a planar bulk n-type MOSFET (a) without and (b) with a gate-to-channel GOS.**

III. Experiment Setup

For experiments, we build four 25nm FinFET devices in the Synopsys Sentaurus TCAD environment. The devices are n/p-type FinFETs with tied-gate (TG) and independent-gate (IG) structures as shown in Figure 3. The TG FinFET in Figure 3(a) uses only one gate to control the channel. On the other hand, the IG FinFET in Figure 3(b) has two gates: front gate and back gate. The front gate usually works to turn-on/off the device while the back gate adjusts the V_{th} of the device. The parameters of all the FinFETs follow the previous work [23]: N_a=1x10$^{17}cm^{-3}$, L_{eff}=25nm, W_{fin}=7nm, H_{fin}=20nm, effective oxide thickness (EOT)=0.65nm, and work function of gate metal=4.55eV.

Based on the above setup, we further inject the GOS into the built devices to simulate defective FinFETs. The GOS injection in this paper utilizes the representation of pinhole [24] [25]. The following steps are consequently applied. Firstly, choose one sidewall of the FinFETs as the defect location. For the chosen sidewall, remove a tiny cubic of the dielectric layer and leave a pinhole in the center. Then,

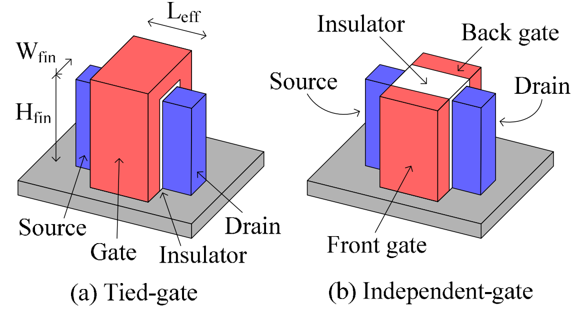

Fig. 3. **Perspective view of the built FinFETs.**

fill the pinhole with gate material. As a result, the gate contacts the channel via a small pinhole, and the GOS injection thereby completes. In our experiments, we apply the pinhole with diameter 5nm as example.

IV. GOS Fault Behaviors in FinFETs

A. Tied-Gate FinFET

For TG FinFET shown as Figure 3(a), GOS occurring at either sidewall of the device causes equivalent fault behavior. It's because the unique gate terminal controls both the sidewall channels in the same manner. Accordingly, we only need to inject the GOS once for the TG-FinFET unlike the twice injections for IG-FinFET, which will be discussed in the next sub-section. Figure 4 shows the experiment results of using an n-type TG-FinFET as example. The supply VDD is 1 volt. In the figure, two sets of IDVD curves are shown. The black-square IDVD curves represent the defect-free FinFET, and red ones represent the defective one. As shown in the figure, GOS causes $I_{D(SAT)}$ decreased as in the planar bulk MOSFETs but just less obviously. As to "Negative $I_{D(low\,V_D)}$" and "Leakage I_G", the defective FinFET also suffers the two fault behaviors similarly.

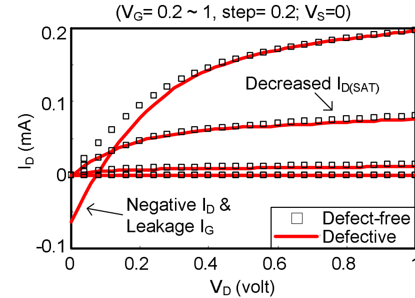

Fig. 4. **IDVD behaviors of TG FinFETs without/with GOS.**

B. Independent-Gate FinFET

For IG FinFET shown in Figure 3(b), GOS occurring at the dielectric layers of front gate and back gate causes different I-V characteristics. It's because the control voltage on the front/back gates was usually set separately for the sake of either performance or low power. For performance, [26] [27] set the voltage of FinFETs' back gates varied depending on the circuit's status to improve the operating speed. For low power, [2] [16] on the contrary fix the back gate voltage to GND/VDD to minimize the leakage current. In our discussion, we apply the low-power mode IG-FinFET design since the device status can be defined more clearly. Accordingly, the back gates of n-type IG FinFETs will be connected to GND. For p-type IG FinFETs, the back gates will be connected to VDD.

Figure 5 shows the simulation results of an n-type IG FinFET without/with GOS at front gate's dielectric. In the figure, the black-square curves belong to the defect-free FinFET. Red curves are of the defective one. As shown in the figure, when V_D is at low voltage, the defective IG FinFET suffers the "Negative $I_{D(low\,V_D)}$" and "Leakage I_G" fault behaviors as well as the previous TG FinFET does. However, when V_D is at high voltage, GOS causes the saturation drain current increased, which is opposite to the decreased $I_{D(SAT)}$ of planar bulk MOSFETs and TG FinFETs.

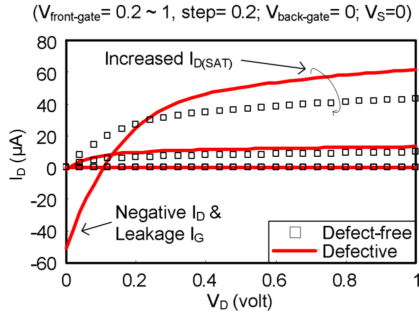

Fig. 5. **IDVD behaviors of IG FinFETs without/with GOS at the front-gate dielectric.**

For analyzing the specific fault behavior, we extract the carrier density of the device under saturation region from the TCAD simulations. We discover the GOS causes much higher carrier density in the channel. The channel thereby becomes more conductive. Figure 6 shows the part of electron density distribution of the IG FinFET. For the defect-free FinFET, the electron density is shown as above. For the defective one, the electron density is shown as below. Comparing the two density distributions, GOS causes thicker channel and higher electron density (from 8.4E+20 cm^{-3} to 1.9E+21 cm^{-3}). As to hole, the carrier density is even more tremendously increased at the back-gate side from 1.1E+8 cm^{-3} to 1.4E+21 cm^{-3}. The reasons for the high carrier density in the silicon fin are two: 1) Holes are injected into the silicon fin through GOS from the front gate with positive bias and continuously accumulate in the back-gate side. 2) The holes change the electrons density in the channel and enhance the electrons injection from source, which leads to the V_{th} shifting. The two phenomenons increase the drain current and are similar to the floating body effect (kink effect) for SOI devices [28] [29].

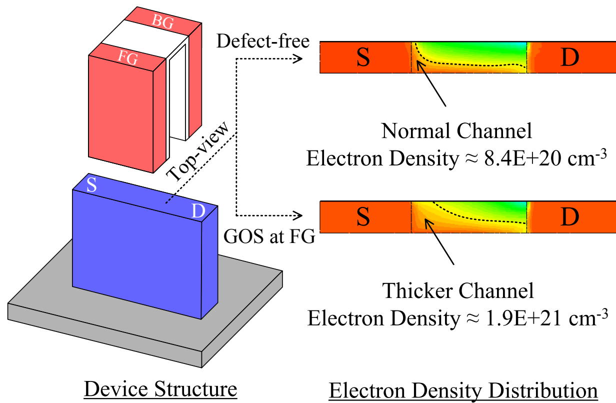

Fig. 6. **Electron density distribution of an n-type IG FinFET with/without GOS at front-gate dielectric.**

As to GOS occurring at the back-gate dielectric, Figure 7 shows the simulation results. The results indicate that the defective IG-FinFET only suffers the "Decreased $I_{D(SAT)}$" but neither "Negative $I_{D(low\,V_D)}$" nor "Leakage I_G". The saturation drain current decreases because the GOS has the back gate turn off more region of the silicon fin, which consequently increases the device's V_{th}. As to the "Negative $I_{D(low\,V_D)}$" and "Leakage I_G", there is no gate leakage occurring because the back gate connected to GND always turns off the back-channel. Since the back channel cannot conduct the carriers, the back-gate leakage current remains very low as of defect-free FinFETs.

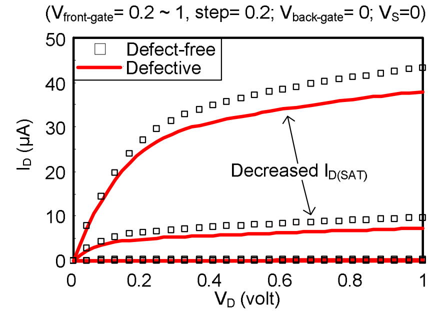

Fig. 7. **IDVD behaviors of IG FinFETs without/with GOS at the back-gate dielectric.**

C. Short Summary

Table I summarizes the GOS fault behaviors of different MOSFETs. For the planar bulk MOSFET, the fault behaviors include the "Decreased $I_{D(SAT)}$", "Negative $I_{D(low\,V_D)}$", and "Leakage I_G" as reviewed in section II. For TG FinFET, the fault behaviors are almost the same as the planar bulk MOSFET, but the fault behavior of "Decreased $I_{D(SAT)}$" is not obvious. As a result, to detect the GOS in TG FinFET, only the test method detecting leakage current can be applied. The test method which intends to detect the reduction of drive ability may be unable to trigger and capture the fault. For IG FinFET, when the GOS occurs at the front-gate dielectric, one of the fault behaviors is different from the two previous cases. The $I_{D(SAT)}$ no longer decreases but increases on the contrary. As to GOS occurring at the back gate, the defective IG FinFET only suffer "Decreased $I_{D(SAT)}$" but no other fault behaviors related to the gate leakage current. To detect the GOS in IG-FinFET is much more complex. For the GOS at front-gate, only the test method detecting leakage current can be applied. For the GOS at back-gate, however, only the test method detecting the reducing of drive ability is applicable.

TABLE I
COMPARISON OF GOS FAULT BEHAVIORS OF DIFFERENT TRANSISTORS

Transistor type & defect location (for IG FinFET)		Fault behaviors		
		$I_{D(SAT)}$ variation	Negative I_D (at low V_D)	Leakage I_G
Planar bulk MOSFET		Decreased	Yes	Yes
TG FinFET		Decreased (not obvious)	Yes	Yes
IG FinFET	Front-gate	Increased	Yes	Yes
	Back-gate	Decreased	No	No

V. Testing of GOS in FinFET SRAMs

Based on the above investigations of GOS in single FinFETs, in this section, we further discuss the corresponding SRAM testing. Figure 8 shows the SRAMs applied in experiments. Figure 8(a) is the typical TG-FinFET based SRAM [30] [31]. Figure 8(b) is the low-power mode IG-FinFET based SRAM [2] [32]. For detecting GOS in the SRAMs, we firstly apply traditional methods including March test and

IDDQ test. The experiment results show that the traditional methods are limited when testing the defect. Hence, we introduce two new test methods. The two proposed methods are for the TG/IG-FinFET based SRAMs respectively and can detect the undetectable GOSs of previous methods.

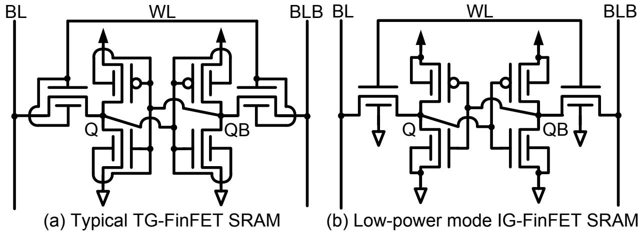

Fig. 8. **FinFET SRAM designs applied for experiments.**

All the related experiments in this section are run under the TCAD transient simulation. To the SRAMs, the setup is as following. The FinFETs are with minimum size (L_{eff}=25nm, W_{fin}=7nm, H_{fin}=20nm) for simplicity [26] [30]. The operation frequency is determined by using the period length which is 20% more than the minimum operatable one.

A. Traditional Tests: March Test and IDDQ Test

To test SRAM, March algorithm is the most commonly used method. By applying organized normal operations to the SRAM, the fault is detected if the read output is different from the expected one. In our experiments, we have difficulty to run a complete March for the SRAM. It's because the TCAD transient simulation requires extremely-long computation period. Thus, we apply parallel operation pairs instead to test the SRAM. The operation pairs include Write-Hold, Write-Read, Hold-Read, Hold-Write, Read-Hold, and Read-Write. And the data covers both 0 and 1. If any one of the operations fails due to the GOS, the defect will be deemed as detected. To distinguish the pass/fail of hold and write, we inspect if Q and QB flip. For read, we examine the BL-BLB voltage difference at the end of the operation. We do not use sense amplifier to judge the read pass/fail because the TCAD limits the number of included FinFETs for each simulation. In our case, only 7∼8 FinFETs at most can be applied each time. Referring to [33], the sense amplifier with VDD = 1 volt can achieve 99.8% yield if the input voltage difference reaches 55mV. Therefore, we judge the read success if BL-BLB's voltage difference is larger than 55mV. For BL-BLB voltage difference less than 55mV, the read is considerred failed.

Table II shows the results of applying operation pairs to detect the GOS. The first two columns are the SRAM type and the possible GOS location. The third column shows if any operation fails due to the GOS at the designated location. If yes, the fourth column shows the detecting operation. As shown in the table, for TG-FinFET based SRAM, only the GOS at the pass-gate nFinFET is detected. The detecting operation is read. For GOS locating at other FinFETs, the TG-FinFET SRAM functions correctly. For IG-FinFET based SRAM, three GOSs are detected. The detected GOSs locate at the front-gate/back-gate of the pass-gate nFinFET and the front-gate of the pull-down nFinFET. The detecting operations are also read.

Apparently, the GOS only affects the FinFET SRAMs' read operations. For hold/write operations, no fault is found. However, according to our experiments, the undetected GOS at the cross-couple inverters actually affects the storing nodes Q/QB of the SRAM. As a result, the cell's reliability is reduced. For those undetected GOS, we further apply the IDDQ test secondly since it has been commonly recommended for detecting GOS in planar bulk MOSFETs [20] [21]. Table III shows the IDDQ sensitivity of each defective case. For calculating the sensitivities, we apply the SRAM with array size 163Mb [5]. Besides, we also apply write operations for the IDDQ test [21] in addition to the hold operation. According to the results, the largest IDDQ sensitivity for the two SRAMs both occur when GOS locates at pull-up pFinFETs. However, the largest IDDQ sensitivity is only 8.6x10^{-4}% and 6.2x10^{-4}% respectively which still limits the test efficacy of IDDQ.

TABLE II
EXPERIMENT RESULTS OF APPLYING OPERATION PAIRS TO DETECT GOS IN FINFET SRAMS

SRAM type	GOS location		Failure occurs	Failed operation
TG-FinFET based	pass-gate nFinFET		yes	read
	pull-down nFinFET		no	-
	pull-up pFinFET		no	-
IG-FinFET based	pass-gate nFinFET	front-gate	yes	read
		back-gate	yes	read
	pull-down nFinFET	front-gate	yes	read
		back-gate	no	-
	pull-up pFinFET	front-gate	no	-
		back-gate	no	-

TABLE III
IDDQ SENSITIVITY OF FINFET SRAMS WITH GOS (ARRAY SIZE IS 162MB [5])

SRAM type	GOS location		IDDQ sensitivity (%) Hold	IDDQ sensitivity (%) Write
TG-FinFET based	pull-down nFinFET		7.8x10^{-4}	6.5x10^{-4}
	pull-up pFinFET		8.6x10^{-4}	4.6x10^{-4}
IG-FinFET based	pull-down nFinFET	BG	9.7x10^{-7}	1.5x10^{-4}
	pull-up pFinFET	FG	6.2x10^{-4}	6.8x10^{-5}
		BG	3.9x10^{-8}	9.7x10^{-6}

FG: front gate BG: back gate

B. Proposed Test method for TG-FinFET based SRAM

In previous sub-section, the traditional methods are shown limited in testing the GOS at the cross-couple inverters. To detect the GOS in TG-FinFET based SRAM, we propose a new test method notated Proposed_TG. The Proposed_TG applies a write operation to the targeted cell with both BL and BLB floating during the period. The voltage on BL/BLB is set specifically to adjust the test efficacy. Figure 9 illustrates the configuration of the Proposed_TG. In the figure, we assume M_a and M_b are the two FinFETs suffering GOS. To detect the GOSs, the floating BL and BLB are with capacitance C_T. And the voltage on them is set to (GND-ΔV) and (VDD+ΔV) respectively to execute a write-0 operation. The original data inside the cell is assumed Q/QB=1/0.

When the SRAM is defect-free, the BLB with voltage (VDD+ΔV) pulls up QB by I_2. BL with voltage (GND-ΔV) pulls down Q by I_1. In this situation, only I_1 and I_2 exist in the figure. However, when the GOS in M_a occurs, I_3 will appear to share I_2 and consume the stored charge on BLB more rapidly. On the other hand, if the GOS in M_b occurs, I_4 will appear to share the I_1 which intends to pull down Q. As a result, the voltage difference of BL-BLB will decrease much more quickly due to the GOS induced I_3 or I_4. The write-0 operation will consequently fail. While the write-0 fails, the following read will output the original 1/0 instead of the expected 0/1. The GOS is then detected. If M_c or M_d is the FinFET suffering GOS, the Proposed_TG can also detect the defect as long as the voltage on BL/BLB and Q/QB exchanges respectively to execute a write-1 instead.

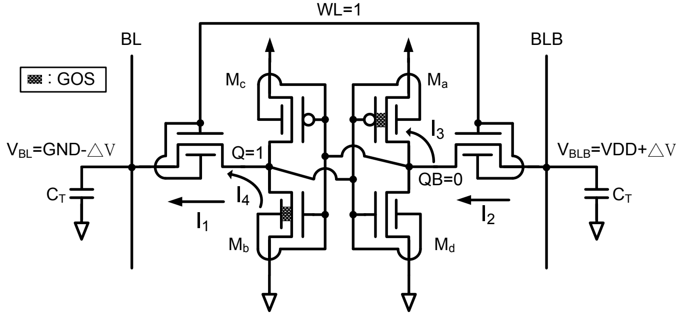

Fig. 9. **Configuration of the Proposed_TG test method for detecting GOS in TG-FinFET SRAM.**

The test efficacy of the Proposed_TG depends on the setup of ΔV and C_T. In Figure 10, we show the corresponding experimental results to help find the valid ΔV-C_T for test. In the figure, the three curves represent the minimum operatable ΔV-C_T for each SRAM. The black-square curve is of the defect-free SRAM, and the other two curves belong to the defective SRAMs with different GOS location. For each curve in the figure, the ΔV-C_T below will fail the corresponding SRAM under the Proposed_TG. On the contrary, the ΔV-C_T above allows the corresponding SRAM pass the test write operation. According to the results, there are three regions in the figure. The lowest one causes not only the defective SRAMs but also the defect-free SRAM failed. The highest region on the contrary has all the SRAMs pass the Proposed_TG. Finally, the ΔV-C_T in the middle region fails the defective SRAMs but has the defect-free SRAM pass the Proposed_TG. The ΔV-C_T in the region is thus the valid one for test.

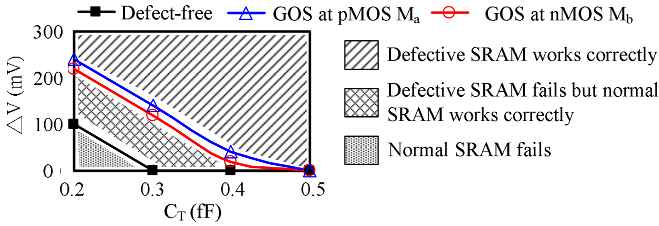

Fig. 10. **Minimum operatable ΔV-C_T for SRAMs passing the Proposed_TG.**

C. Proposed Test method for IG-FinFET based SRAM

To detect the GOS in the IG-FinFET based SRAM, we propose a test method notated Proposed_IG. The Proposed_IG is actually modified from the Proposed_TG in the previous sub-section. Before introducing the Proposed_IG, we firstly illustrate how and why the Proposed_TG is insufficient for the test here. We repeat the experiment in Figure 10, but the tested SRAM is changed to the IG-FinFET based one. Figure 11 shows the results. Figure 11(a) is with GOS at the front gate of the IG FinFETs. Figure 11(b) is with GOS at the back gate on the other hand. According to the results, the Proposed_TG has valid ΔV-C_T for detecting the front-gate GOS as shown in Figure 11(a). But for back-gate GOS, the results in Figure 11(b) show no valid ΔV-C_T exists. The Proposed_TG detects the front-gate GOS because it triggers the gate leakage current in IG-FinFETs as in the TG-FinFETs. However, while the back-gate GOS causes no fault behavior related to gate leakage current as mentioned in section IV-B, the test method has no way to detect the defect.

To detect the back-gate GOS, we include the testing of decreased $I_{D(SAT)}$ into the Proposed_IG. Besides, by being modified from Proposed_TG, the Proposed_IG also inherits the advantage of de-

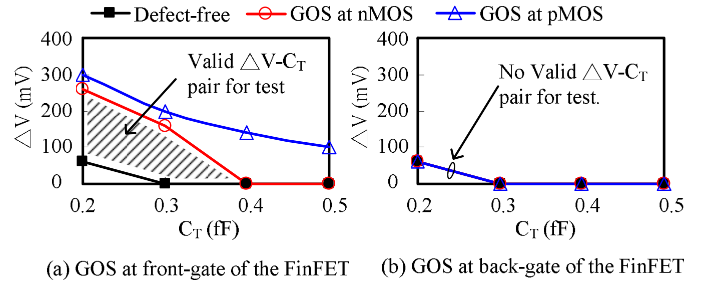

Fig. 11. **Test results of applying Proposed_TG for detecting GOS in the IG-FinFET SRAM.**

tecting gate leakage current. The Proposed_IG can detect both the front-gate/back-gate GOS at the same time. Figure 12 shows the configuration of the Proposed_IG. In the figure, M_a is assumed the IG FinFET of which the front gate and the back gate may suffer GOS. To test the GOSs, Proposed_IG sets the BL and BLB floating similar to Proposed_TG. The voltage on BL is also (GND-ΔV). But the voltage on BLB is modified from the original (VDD+ΔV) to 0. Note that the test write operation here is still a write-0. For the front-gate GOS, since the BL/BLB remain floating, the GOS induced current I_3 will affect the SRAM in the same manner as for the TG-FinFET SRAM. The Proposed_IG can detect the front-gate defect. As to back-gate GOS, the modification of BLB voltage makes the pulling up of QB rely on I_2 only without the driving current from BLB. If the back-gate GOS in M_a decreases the drain current I_2 too much to succeed the pulling up QB, the test write operation would fail. And the back-gate GOS is hence detected.

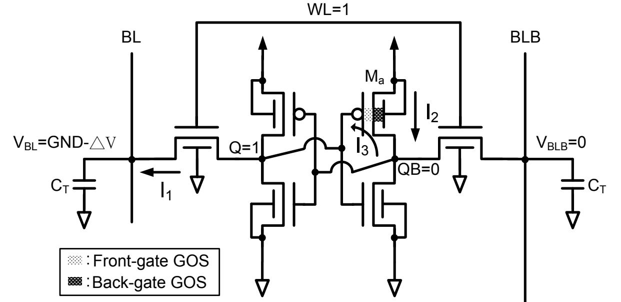

Fig. 12. **Configuration of the Proposed_IG test method for detecting GOS in IG-FinFET SRAM.**

Figure 13 shows the simulation details of the Proposed_IG detecting both the front-gate and back-gate GOS at the same time. For the simulations, we apply C_T=0.2fF and ΔV=0.62V as example. In the Figure 13, the IG-FinFET SRAM is under three conditions: (a) defect-free, (b) GOS at front gate, and (c) GOS at back gate. For each case, we show the the voltage of Q/QB and V_{BL}/V_{BLB} during the test write-0 period. Firstly, for the defect-free SRAM, Figure 13(a) shows the Q and QB successfully flip, and V_{BLB} is always higher than V_{BL}. When GOS occurs at front gate, the Figure 13(b) shows the Q is pulled down and reaches QB. But the Q remains higher than QB at the end. The write-0 thus fails. For GOS occurring at back gate, Figure 13(c) shows the Q/QB flip at time=2ps. But while V_{BL}/V_{BLB} also flip later on, the driving force of the write-0 disappears. The Q/QB then flip again at time=4ps. The test write operation fails as well, and the back-gate GOS is detected.

Table IV summarizes the test efficacy of the methods for detecting GOS in the IG-FinFET SRAM. Firstly, Proposed_TG detects the front-gate GOSs for pull-down and pull-up IG-FinFETs. But for back-gate GOSs, the test method cannot detect the defects. Proposed_IG

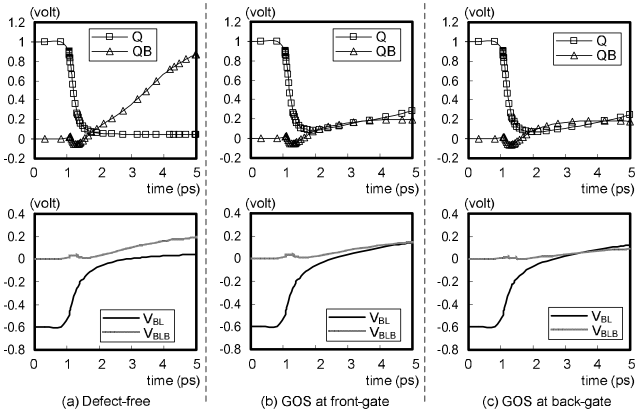

Fig. 13. **Simulation details of the Proposed_IG detecting front-gate/back-gate GOS at the same time (C_T=0.2fF, $\triangle$V=0.62V).**

on the other hand detects all the GOSs including front-gate/back-gate GOSs in both pull-down and the pull-up IG-FinFETs. For comparison, we also include the severe write test method [34] in experiments. The method is included because the decreased $I_{D(SAT)}$ caused by back-gate GOSs is similar to the fault behavior of open defects. And the severe write method has been shown useful for detecting the open defects in SRAMs. According to the results, the severe write method does not detect any back-gate GOSs. After improvement, the modified severe write can detect the back-gate GOS, but only the one in the pull-down IG FinFET.

TABLE IV
TEST EFFICACY COMPARISON OF THE METHODS TO DETECT THE GOSS IN IG-FINFET SRAM

Test method	Detecting the GOS in IG-FinFET SRAM			
	pull-down n-FinFET		pull-up p-FinFET	
	FG	BG	FG	BG
Proposed-TG	yes	no	yes	no
Proposed-IG	yes	yes	yes	yes
Severe write [34]	no	no	no	no
Modified severe write	no	yes	no	no

FG: front gate BG: back gate

VI. CONCLUSION

In this paper, we investigate the gate oxide short (GOS) in FinFETs by using the TCAD mixed-mode simulation. According to the results, we discover the GOS fault behaviors in FinFETs are more complex than those in planar bulk MOSFETs. For tied-gate FinFETs, the fault behavior of saturation drain current decreasing becomes much less obvious. This leads the test method, which intends to detect the reducing of device's drive ability, to be unable to detect the defect. For independent-gate FinFETs, the fault behaviors of the GOS at front gate and back gate completely differ from each other. When locating at the front gate, the GOS increases the saturation drain current and induces the gate leakage current. But when locating at the back gate, the GOS decreases the saturation drain current on the contrary and causes no fault behavior related to gate leakage current. Based on the investigation for single FinFETs, we also discuss the corresponding SRAM testing. For detecting GOS in the SRAMs, we propose two new test methods. One is for tied-gate FinFET based SRAM, and the other is for independent-gate FinFET based one. Both the methods can detect the undetectable GOSs of traditional methods and are verified by using the TCAD transient simulations.

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