11.2 A SiP Tuner with Integrated LC Tracking Filter for both Cable and Terrestrial TV Reception

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Many countries around the world currently operate a simultaneous broadcast service where both analog and digital TV are made available for the viewers at the same time. The presented chip is called a hybrid silicon tuner, as it is able to receive both all analog (PAL, NTSC, SECAM) and all digital (DVB-T/H, ISDB-T, ATSC, DVB-C) TV standards.

This hybrid silicon tuner is a system-in-package (SiP) module consisting of a 40GHz f_t 0.25µm BiCMOS die and 19 SMDs (coils, capacitors, resistors, and varicaps) on laminate (see Fig. 11.2.7). All these SMDs are used for implementing the RF LC-tracking filter.

The hybrid silicon tuner is based on a Low-IF architecture with an integrated splitter and a loop-through (LT) function as shown in Fig. 11.2.1. The intermediate frequency (IF) can be set in the 3.5–to-5MHz range according to the desired standard. Compared to an upconversion concept, the used Low-IF architecture has the advantage of avoiding the use of any SAW filter. In addition, the splitter and LT integration drastically reduces the number of components needed for multi-tuner/multi-stream applications. The added RF LC-tracking filters enable achieving weighted SNR performances equivalent to that of conventional tuner cans, even in loaded spectrum conditions. Only a single LC-VCO is used to generate the total LO frequency range, which significantly reduced the silicon area.

30V varicaps are used for large tuning range and high dynamic range handling. This voltage is generated on chip using a Dickson DC-DC converter. Despite their low density, fringe capacitors are used because they can tolerate very high voltages. In addition, their leakage current is negligible and their stray capacitance is reduced becasue of the shielding done by a poly layer connected either at the top or bottom side of the capacitor. The 0.25µm BiCMOS process can withstand high voltages due to the high breakdown voltage of the collector substrate junction (B_{VCS0}≈80V). The discharge system of the DC-DC converter, depicted in Fig. 11.2.2, enables decreasing the output voltage (if needed) by pumping the output charge towards a low impedance point (e.g., the ground). This is done using a DC-DC down converter [1]. The V_{low} ground enables the use of N diodes as an ESD protection that will help discharging process during the positive voltage stress at the output pin. When the DC-DC up converter is switched on, the DC-DC down converter is switched off and vice versa. This is done by using *Ck Up* and *Ck Down* signals.

The tuning of the RF LC-tracking filters is updated at every channel selection by injecting a test signal at the filter inputs. As shown in Fig 11.2.1, a dedicated VCO and PLL (also used for the image-rejection calibration) generate this test signal. The frequency and peak level of the test signal are carefully chosen to minimize any leakages through the splitter and the LT. The tracking system tunes the varicaps biasing of the RF filters to properly adjust its resonance frequency. The peak level *P* of the test signal is measured on-chip at the IF low-pass filter output. *P* does not contain accurate information on the varicap biasing. Consequently, the tuning is performed in two phases. First, the varicap is biased at its minimum value (1V) such that the filter resonance frequency is at its minimum frequency and *P* is measured. Then the biasing of the varicap *Vb* is continuously increased which results in an increase of *P*. When the varicap biasing Vb_{up} is just above its optimal value Vb_{opt}, the corresponding P_{up} *is* lower than its maximum value P_{max}. Since the RF filter frequency response is symmetrical around the resonant frequency, in the second phase of the tuning procedure, stepping backward from Vb_{up} first increases P_{up} to its maximum value P_{opt}. Then, stepping down further *Vb*, *P* starts to decrease again. When *P* is 1dB lower than P_{up} the corresponding varicap biasing Vb_{down} is latched and the optimal varicap biasing Vb_{opt} is equal to the average value of Vb_{up} and Vb_{down}. The measured RF selectivity is illustrated in Fig. 11.2.3.

The image suppression of double-quadrature mixers followed by a polyphase filter is slightly better than 50dB [4]. This is 10dB less than the target of more than 60dB of image rejection. To increase the image-rejection (IR) an auto calibration of the amplitude and phase correction [5] is implemented. The amplitude error between I and Q branches is adjusted with controllable resistors R2I/Q (see Fig. 11.2.4). The phase error between I and Q is minimized by subtracting a small part of the I signal from the Q signal or vice versa by using resistors R3I/Q. During the IR calibration, an on-chip PLL generates a single test-tone signal that is fed at the input of the RF polyphase filter. After downconversion, its peak level is measured at the output of the IF low-pass filter and it is stored in a register. Then, the calibration PLL generates a signal frequency that corresponds to the image of the RF signal. The level of this image signal is 38dB higher than the RF signal to compensate for the negative frequency attenuation in the double quadrature mixer and the polyphase filters. As illustrated in Fig. 11.2.5, the peak level of the image signal is measured and the IR is 58dB (38+20). Based on this IR value, R2I, R2Q, R3I, and R3Q are successively increased and the IR is measured. At the end of the calibration, R2I/Q and R3I/Q are set with values that enable to get the best measured IR (68dB) which is more than the 60dB target. At the power-up, this procedure is repeated three times for an RF signal at 100MHz, 400MHz, and 800MHz. It guarantees that the IR is more than 60dB in the 48-862MHz range.

The fractional-N synthesizer continuously tunes a single low-noise fully integrated LC-VCO in the range of 7.1 to 8GHz, corresponding to a tuning range of 12.5%, with small frequency steps (<1kHz) [3]. The tuning range of the single VCO is extended to 100% using the 8-15 prescaler R, thus creating 8 sub-bands. Since the quadrature of the LO signal is generated by a divider by 2, the LO signal has to be multiplied by 2 after division by R. A duty-cycle correction is required to compensate the duty-cycle error (up to 25%) introduced by the R prescaler. Four additional post divide-by-2s are added to extend the LO range to the desired 48 to 862MHz. The measured phase noise at the tuner output is better than –90dBc/Hz at 10kHz offset for an RF signal at 862MHz.

The hybrid silicon tuner is designed to meet NorDig specification for DVB-T and A74 recommendations for ATSC. Noise figure at maximum gain is 5dB. The die size is 5.7mm and the SiP module measures 9×9×1.6mm^3 (Figure 11.2.7). The power consumption is 750mW at 3.3V. When it is used in combination with an IF demodulator, it achieves a weighted SNR of 55dB. As illustrated in Fig. 11.2.6, this hybrid silicon tuner performs similar to classical can tuners.

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[2] F. Behbahani, Y. Kishigami, J. Leete, and A.A. Abidi, "CMOS Mixers and Polyphase Filters for Large Image Rejection," *IEEE J. Solid-State Circuits*, vol. 36, pp. 873-887, June 2001.
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[5] M. Notten, M. Bernard, V. Rambeau, and J. van Sinderen, "A CMOS Quadrature Down-Conversion Mixer with I/Q Correction Obtaining 55dB of Image Rejection for TV on Mobile Applications", *IEEE RFIC Symp. Dig. Papers*, June, 2006.

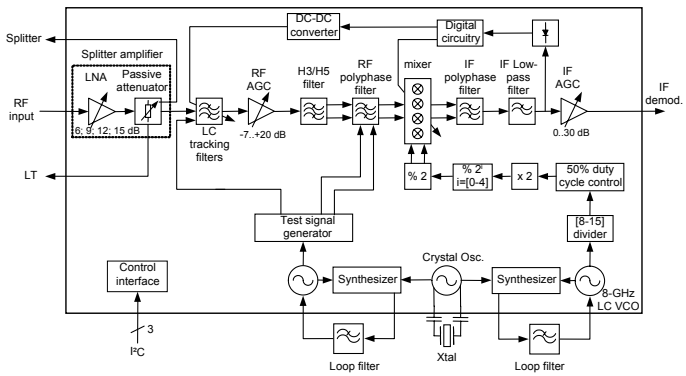

Figure 11.2.1: The hybrid silicon tuner block diagram.

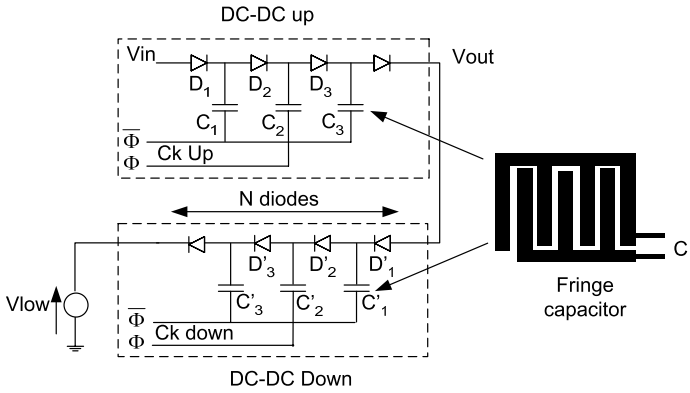

Figure 11.2.2: DC-DC Converter with its discharge circuitry.

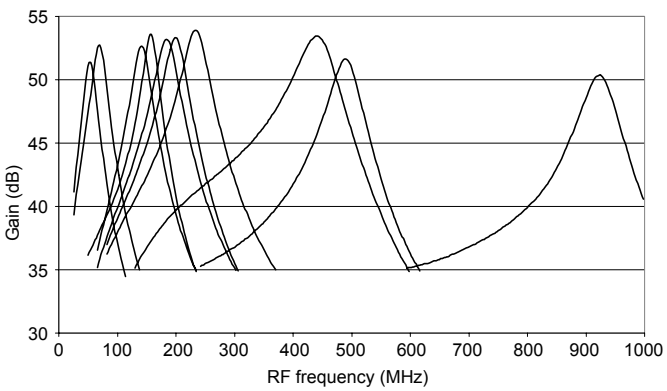

Figure 11.2.3: Measured RF LC-tracking filter selectivity.

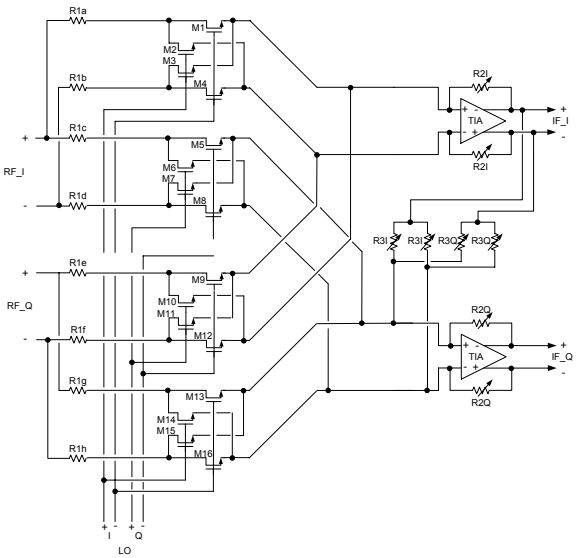

Figure 11.2.4: Passive MOS mixer with amplitude and phase error correction.

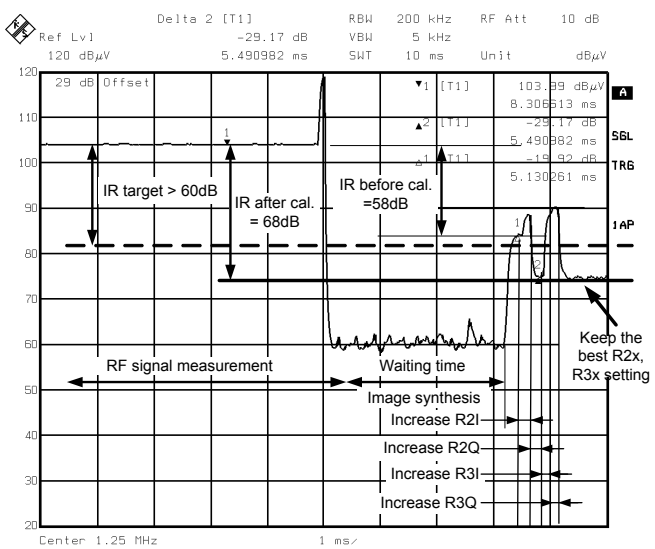

Figure 11.2.5: Measured IR during calibration.

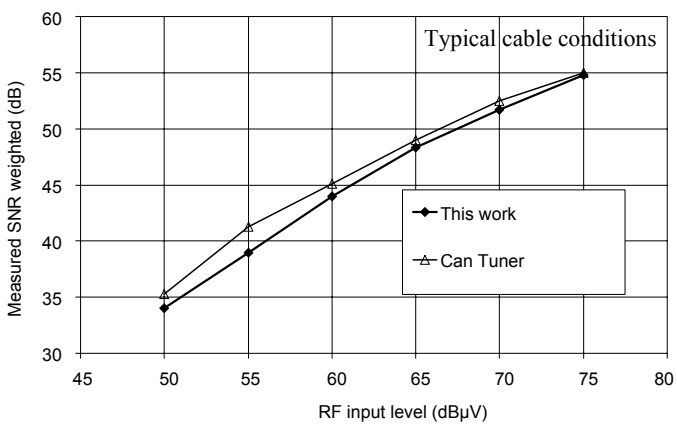

Figure 11.2.6: Weighted video SNR for analog PAL B TV reception.

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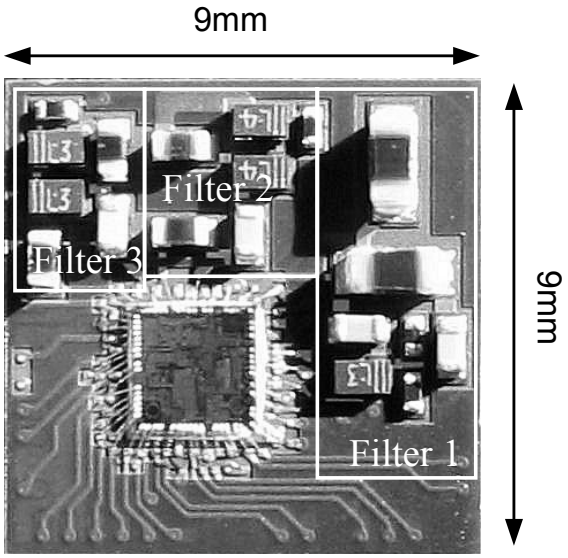

Figure 11.2.7: Micrograph of the un-molded SiP hybrid silicon tuner.

