TSV Technology and Challenges for 3D Stacked DRAM

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Abstract

A successful integration of Via-middle TSV process in DRAM technology with major process issues is introduced. Fast TSV open/short detection and how to trade-off in choice repair scheme is discussed. Process development for TSV volume shrink required to reduce dynamic power for driving TSV. Fast Cu leak monitor method is essential to sustaining good quality and Fab process control.

Introduction

3D memory stacking using by fine-pitched TSV array has been developed last two decades as highly promising technology to overcome density scaling limitation as well as to enable high data bandwidth. Commercial sample release of its major applications (HBM and HMC) are being expected in near future, technology hurdles still remains before grand opening of TSV era; cost-effective DRAM compatible Via-middle TSV process should be developed. Wafer thinning and stacking process should guarantee sufficient mechanical stiffness without deteriorating DRAM data retention characteristic. Fast and sensitive Cu leak/migration, Cu Void, and TSV-to-TSV open/short detection method should be developed. This paper may provide an answer the question and shows the right way to go. An example of DRAM compatible TSV process and key factor in process optimization are introduced in next section. Cost effective TSV open/short detection method is shown in subsequent section. A list of subjects to develop for mass production is proposed in last part.

TSV Process Integration

Fig.1 shows the VIA middle TSV process integrated in triple metal DRAM technology. After M1C tungsten plug CMP, TSV pillar formation is following. M1C plug and TSV pillar are connected in same M1 level by single damascene Cu wire. High aspect ratio vertical profile and small scallop control are essential factors for Bosch TSV etch scheme. Less than 30nm of scallop diameter is required to guarantee barrier metal and seed Cu coverage. Careful choice of barrier metal species and its thickness are essential to prevent Cu eruption. Fig.2 shows an example of Cu eruption failure caused by poor process control of barrier metal structure and insufficient degassing during dielectric film deposition. Cu protrusion over the top side of Cu pillar is known due to high thermal expansion mismatch between Copper and Silicon[1], which can be reduced by Cu anneal temperature control. TSV void formation and its migration is another key issue. Poor deposition coverage or impurity introduced during Cu deposition may causes mid-void in the pillar. Existence of mid-TSV void itself may not cause an electrical failure, but it tends to move toward surface under subsequent thermal and/or mechanical stress which cause contact failure[2]. Fig.3 shows experimental results whether and how much contact failure occurs in intentional fabricated mid-void TSVs during baking process. Comparing with control wafer, mid-void wafer shows incremental contact failures caused by surface-gathered void during baking stress. Optimal process control not to introduce void during Cu deposition subsequent stress control is important.

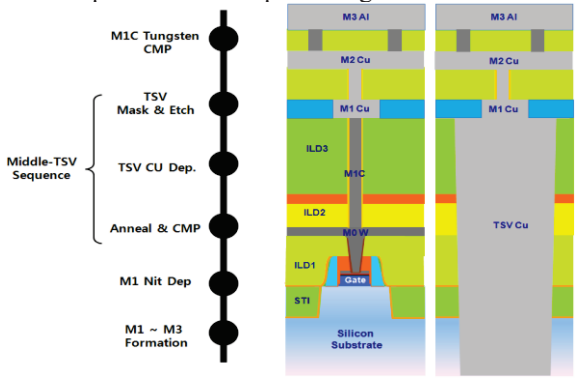

Fig.1 VIA-middle TSV process sequence and its cross-section.

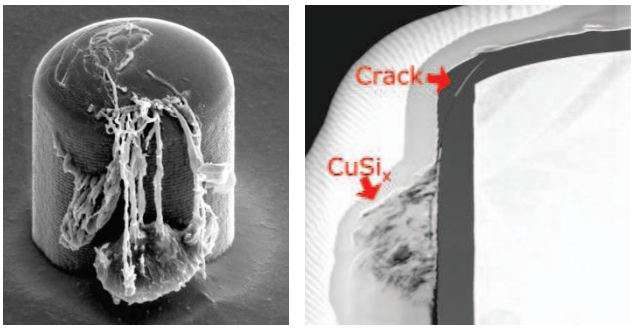

Fig. 2 Cu eruption Failure occurred from un-optimized barrier metal and dielectric deposition condition. Failure detected during TSV revealing wafer back-side thinning process.

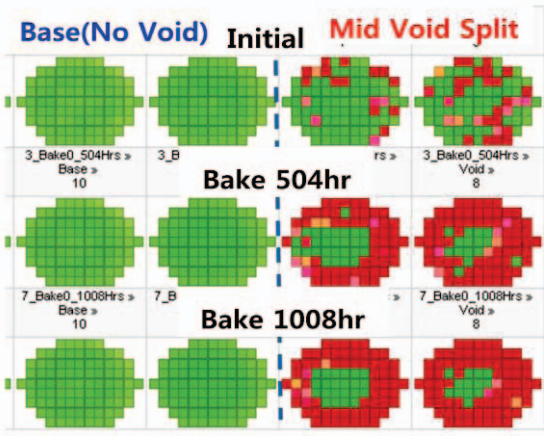

Fig.3. Wafer Map comparison between control and Mid-Void split: Fail die(red dot) is increasing as bake proceed.

Micro Bumping and Stacking

Fig.4 depicts stacked die cross-section schematic and key elements during bumping and stacking process. Fig.5 shows a partial picture of four-stacking memory die on the carrier wafer before the KGSD (Known Good Stacked Die) Test.

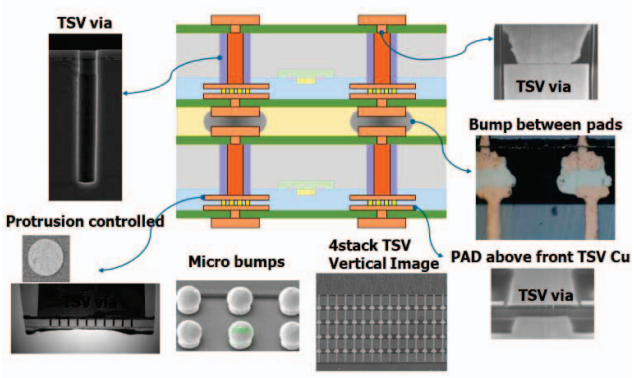

Fig.4 Stacked Die cross-section and key process control aspects.

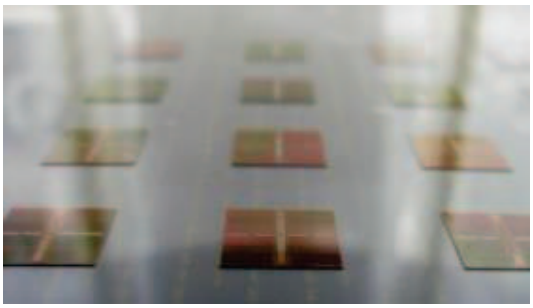

Fig.5 Four-stacked KGSD sample mounted on carrier wafer

DFT for TSV Testing

For the efficient testing of TSV, proper DFT (Design-for-Testability) techniques need to be implemented. Fig.6 shows an approach to use probe pad monitoring the current through TSV's. After collecting the current distribution for good TSV paths, we can detect the open TSV or short TSV as an outlier in the current distribution. Another DFT approach is to use boundary scan based technique. Fig 7 shows the JEDEC JESD229 (Wide-IO) boundary scan implementation. Each IO has boundary scan cell (BSC) assigned. The control signals, SDO

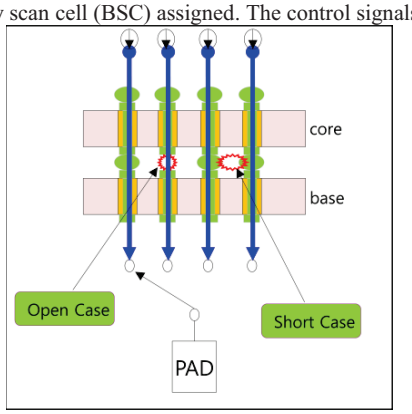

Fig.6 TSV Open-Short Test

and SDI can be integrated with the IEEE Std. 1149.1 interface. Since the standard is a well-know standard, the boundary scan based technique can utilize the existing infra structure of design, pattern generation, and debugging. HBM adopted IEEE Std. 1500 for the u-bump and interposer testing. IEEE P1839 is underdevelopment to define a standard test interface for 3D IC based on TSV technology.

TSV Scaling and TSV Yield

TSV scaling technology is also a key factor for achieving higher performance and reducing area. TSV diameter and TSV pitch plays an important role in Wide-IO TSV structures, such as HBM(High Bandwidth Memory) and WIO2. It directly relates to TSV capacitance hence determines the TSV dynamic current. Fig.8 shows the simulation result of the ratio of TSV current over IDD4R/W mode as a function of TSV diameter and height in 8-high HBM stack. Reducing height may change mechanical property of substrate Silicon and seriously deteriorate data retention time of DRAM. Diameter reducing increases VIA aspect ratio which causes difficulty in Cu gap fill capability.

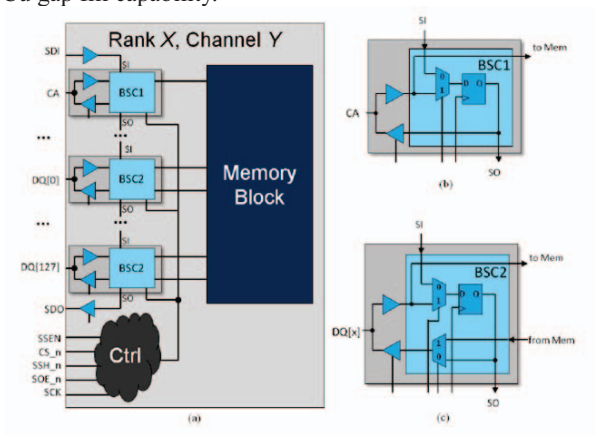

Fig.7 JEDEC Wide-IO DRAM boundary scan implementation

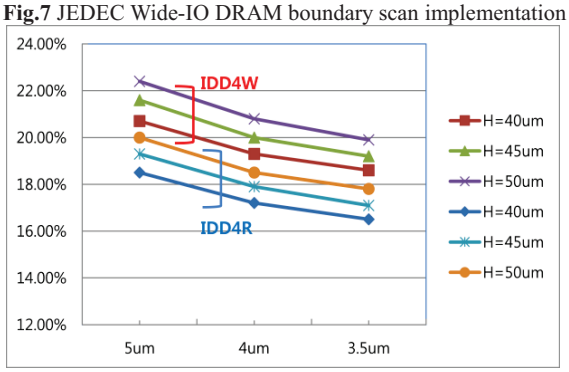

Fig.8 The ratio of TSV current over IDD4R/W mode as a function of TSV diameter and height.

One another interest is what TSV repair scheme should be selected in the stack memory. In case of n:1 scheme for a group of TSV, assuming the yield of single TSV is p, Group Yield=$p_{gr\_n:1}=p^{n+1}+{}_{n+1}C_1p^n(1-p)$. If we assume the number of n:1 group as m, Die Yield=$p_{d\_n:1}=p_{gr\_n:1}{}^m$. On the other hand, in case of 2n:2 scheme for a group of TSV, Group Yield=$P_{gr\_2n:2}=p^{2n+2}+{}_{2n+2}C_1p^{2n+1}(1-p)+{}_{2n+2}C_2p^{2n}(1-p)^2$, and the Die Yield=$P_{d\_2n:2}=P_{gr\_2n:2}{}^{m/2}$. It shows that 2n:2 scheme is beneficial to get yield more effectively. However it also requires 2 redundant TSVs per group resulting in more area for most cases. Since the redundant TSVs cause area increase and performance degradation, it will be the best if there need no redundant TSVs, the best alternative plan will be to get enough die yield using the n:1 repair scheme. To generalize the use of n:1 repair scheme, very high yield of single TSV should be guaranteed.

Further Works

To sustain good yield and quality in mass production of TSV memory, fast (not exceed 15sec/site[3]) Cu leak monitor should be developed. Plasma discharging technique to prevent arching in fabrication process for passive interposer and ESD protection for micro-bump are also crucial tasks.

References

[1] Lee K., et.eal., Reliability Physics Symposium(IRPS), 2012, page. 5F.2.1-5F.2.4.

[2] E.T.Ogawa, et.al., 40th Annual Int'l Reliability Physics Symposium, 2002, page.312-321.

[3] *For examples*, P.Tiwari,et.al., Solid-State Electronics Vol.26, No.7, pp.695-698, 1983.