Fully Integrated Distributed Power Amplifier in CMOS Technology, optimized for UWB Transmitters

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Abstract — **A power amplifier (PA) in distributed amplifier technique for the Ultra Wide Band (UWB) standard is presented. The amplifier was fabricated in a standard 0.13 µm CMOS technology and comes with an on-chip biasing circuitry and a non-distributed input stage. Measurement results are given for a chip-on-board module to take any influence of a product assembly into account. It achieves a transmission coefficient S_{21} = 17 dB, a corner frequency of f_c = 8 GHz and a 1dB compression point of A_{1dB} = 3.5 dBm. The output impedance is matched to 50 Ω so that external matching circuitry can be omitted. With these features it is customized to be integrated with the other building blocks to a fully integrated CMOS UWB transmitter product.**

Index Terms — **Distributed amplifiers, CMOS power amplifiers, broadband amplifiers, data communication, indoor radio communication, Ultra Wide Band.**

I. Introduction

All building blocks required for state of the art communication IC's were recently investigated in standard CMOS technologies to go down in size and costs. Nevertheless, the high speed interfaces of the IC on the board seem to be the bottleneck in this development. Especially in CMOS technology the necessary bandwidth and the required output performance can only be achieved with carefully tailored circuit design. The often used method of inductive peaking [1] is only suitable for narrowband applications. For a fully integrated transmitter a 50 Ω matched power amplifier is desirable. In standards with narrow bandwidth like GSM, DECT or Bluetooth the impedance can be tuned by means of a transformer, which can either be on board or integrated on chip [2].

The UWB standard, in contrast, requires a wideband system, that can use the frequency band from f_{low} = 3.1 GHz up to f_{high} = 10.6 GHz. Even if a future standard in a first step does not employ the whole bandwidth the use of baluns or transformers appears to be more than critical.

For that reasons the distributed amplifier technique which is intrinsically suited for broadband circuits and widely used for high speed communication systems [3], seems to be the key to a 50 Ω matched power amplifier with appropriate linearity. In a distributed amplifier the active transistor is divided into several stages connected by tailored transmission lines to combine the transfer functions to the desired frequency behavior. The overall transfer function can be shaped for higher bandwidth by the ratio and number of its stages and the impedance and length of the transmission lines.

The internal interface of the PA in an UWB transmitter will be realized by a non-distributed preamplifier stage to drive the PA, so that the input impedance of the distributed amplifier has to be optimized with respect to the preamplifier. For product requirements external bias voltages are not desirable, so that a complete integrated biasing circuitry is necessary. To drive the antenna without additional power amplifiers an appropriate linearity is needed. This contrasts with the imperative to go down in power supply voltage to a level that is sufficient for the other building blocks of the transmitter.

This paper presents a power amplifier design which exhibits all this features. The focus of this paper is to show that a PA suitable for a UWB system can be integrated in a CMOS transmitter. First, the design of the PA and the measurement setup are discussed. Second, the measurement results are presented and compared with the simulation results.

II. Circuit Design

The presented PA was designed as a four stage distributed amplifier. Its active transistor is used in a resistively loaded common source configuration which is biased to provide appropriate linearity. The PA comes with a single ended 50 Ω matched output to avoid an external balun. Therefore a separate supply voltage pin is preferable to decouple the PA from other sensitive building blocks of the transmitter like bandgap references and voltage controlled oscillators.

The number of stages is a trade off between the desired bandwidth and the die size, the stability of the circuit and the possibility to optimize the design parameters.

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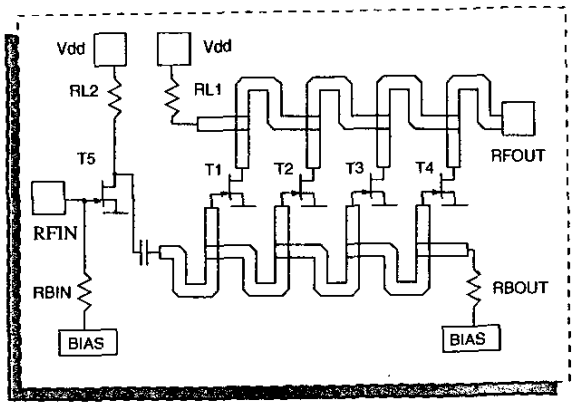

Fig. 1. Block diagram of the four stage distributed amplifier and the non-distributed input stage.

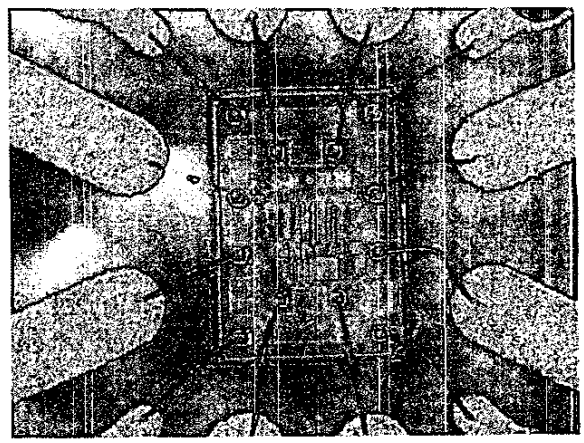

Fig. 2. Photograph of the power amplifier mounted on the measurement board.

Figure 1 shows a block diagram of the entire chip. The distributed amplifier comes with microstrip transmission lines using the top metal layers as a signal conductor and the bottom layer as the ground plane. The ground plane additionally prevents substrate coupling of the PA and other sensitive blocks. The disadvantage of microstrip lines compared to coplanar wave guide lines due to the skin effect reported in [4] is negligible, because the conductor dimensions are in the order of magnitude of the skin depth by frequencies up to $f = 10$ GHz.

The feed lines of the stages to the gates and drains, respectively, were simulated using the microstrip line models of the Advanced Design System (ADS) simulation tool of Agilent. The Simulator uses the Kirshning model of a microstrip transmission line. The impedance and length of each transmission line were evaluated using ADS to tailor the scattering parameters of the PA and the input buffer to a predefined frequency behavior. The input reflection coefficient of the input PA is therefore customized to the characteristics of the output impedance of the input buffer to avoid any insertion losses. The resulting dimensions show a non uniform distribution of both the transistor width values and the parameters of the transmission lines.

Fig. 2 exhibits a photograph of the mounted chip with a view on the transmission lines that form the distributed amplifier.

The input buffer is designed in a single ended common source configuration, too. The input is matched to 50 Ω for measurements. In a transmitter the input impedance is to be fitted to the previous circuitry. It is internally biased and a capacitor is used to decouple the biasing of the buffers. The parasitic capacitance of this capacitor has a severe influence on the frequency behavior of the circuit, so that it is necessary to take it into account while the PA. In this design a vertical finger capacitance is used which shows a large parasitic capacitance. In a redesign this capacitance was replaced by a more suitable metal insulator metal (MIM) capacitance to improve the performance of the PA.

III. Measurements

The chip was measured on a chip-on-board assembly technique. The signal lines of the measurement board were designed as a microstrip line to provide an impedance of 50 Ω and the bond wires are about 0.5 mm in length. This would represent any parasitic influences of a product assembly on a application board, so that the measurement results give an appropriate insight to the behavior of the fully integrated PA of an UWB transmitter. The output of the PA was biased by means of a bias tee to achieve maximum linearity. The reference of the biasing can be adjusted by an external resistance. The chip uses $I_{supply} = 50$ mA from $V_{DD} = 2$V power supply. To evaluate the measurement results the SMA contacts were modeled in ADS by a T equivalent circuit consisting of a parallel parasitic capacitance, an series inductor and a wire line representing the electrical length. The bonding wire is represented by a lumped inductivity. The board model was evaluated by measuring a 50 Ω terminated input pad on chip.

As key parameters for the PA the scattering parameters were measured to investigate the gain and bandwidth and the 1dB compression point A_{1dB}.

The model of the measurement board and SMA connector were used to simulate the scattering parameters of the measurement setup. The forward transmission

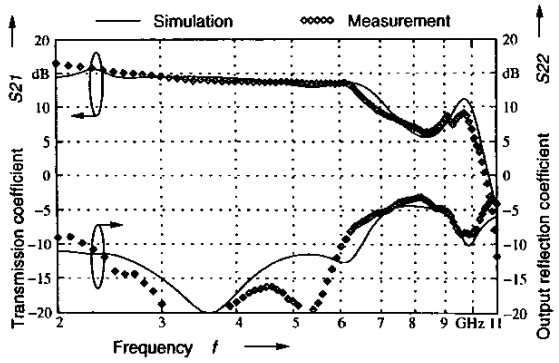

Fig. 3. Transmission coefficient S_{21} and output reflection coefficient S_{22} of the PA including the measurement board.

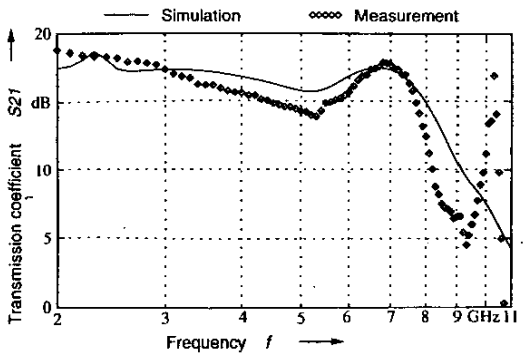

Fig. 4. Transmission coefficient S_{21} of the PA including the bond wire of the output pad.

coefficient of the chip, including the bond wire of the output pad was then evaluated by deembedding the results of the measurement using ADS.

IV. Results

The scattering parameters were measured from $f = 2$ GHz up to $f = 11$ GHz and compared to the simulation results of the chip including the board modeling. Fig. 4 shows the transmission coefficient S_{21} and the output reflection coefficient S_{22} of the chip on the measurement board, respectively. The measurement results show excellent matching to the simulation results. The output reflection coefficient S_{22} is lower than -5dB.

Fig. 4 shows the transmission factor of the deembedded scattering parameters. As stated before this includes the wire bond of the output pad and shows therefore the performance of an integrated PA including the assembly parasitics.

The simulation result of the PA with the bond wire inductivity shown in Fig. 4 exhibits again good matching to the deembedded results. The maximum transmission coefficient is $S_{21max} = 17$ dB and the 3dB corner frequency is $f_{3dB} = 8$ GHz.

Another key parameter of the PA is the linearity to avoid signal distortions in the transmit path. The maximum average output power of an UWB transmitter is limited to $P = -41.3$ dBm [5]. Nevertheless the required linearity of the transmitter is far higher because peak power values are calculated to be about $P = +2$ dBm. Because of the expected losses of the antenna the linearity of the PA should exceed this value.

Fig. 5 shows the measurement results for the PA. The input power of the measurement board is sweeped for the frequencies $f = 3,4,5,6,7$ GHz, respectively. It can be seen that the 1 dB compression point is $A_{1dB} = 3.5$ dBm, and therefore meets the requirements. In Fig. 6 the results of the simulation are shown, they exhibit the same 1 dB compression point.

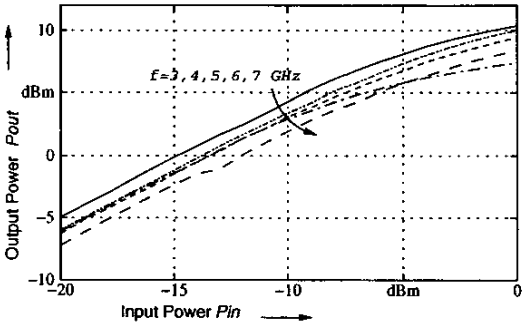

Fig. 5. Measurement results of the linearity of the PA.

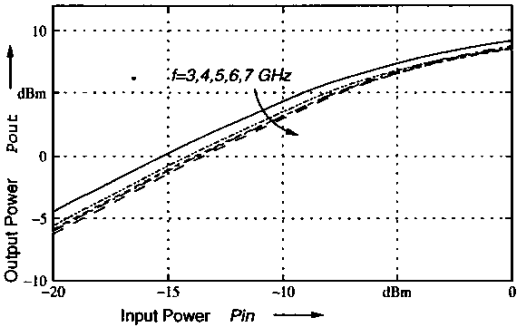

Fig. 6. Simulation results of the linearity of the PA.

TABLE I
SUMMARY OF MEASUREMENT RESULTS

Parameter	Value
3 dB corner frequency f_{3dB}	8 GHz
Maximum transm. coeff. S_{21}	17 dB
1 dB compression point A_{1dB}	3.5 dBm

V. CONCLUSION

The distributed amplifier technique is suitable to overcome the bandwidth limitations at the assembly interface of a fully integrated CMOS application like an UWB transceiver. The key figures of the measurement results are listed in Table I.

The 50 Ω matched single ended output requires no external or internal balun, the output reflection coefficient is lower than S_{22} = -5 dB up to the f_{3dB}, so that an impedance transformation can be omitted, and up to f = 6 GHz it is lower than S_{22} = -10 dB. With its features it is well suited for a highly integrated low cost solution for UWB.

Appropriate biasing and a customized driving stage ensures that the circuit can be integrated on a CMOS transmitter without degradation of its performance. The parasitic influences of a product package have been taken into account by measurements of a chip-on-board assembly.

The demonstrated scattering parameters show the required bandwidth for UWB application. Due to the high gain of the PA any further amplification by preamplifiers can be omitted and thereby the power consumption of the overall transmitter decreased. The measured linearity of the PA demonstrates that it is perfectly qualified to drive an antenna with the required peak output power of the UWB standard.

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