180Vpp Output Voltage, 24MHz Bandwidth, low power Class AB Current-Feedback High Voltage Amplifier for Ultrasound Transmitters

Davide Ghisu, Andrea Gambero, Marco Terenzi, Giulio Ricotti, Anna Moroni, Sandro Rossi
STMicroelectronics
Cornaredo, Milan (MI), Italy
davide.ghisu@st.com; andrea.gambero@st.com; marco.terenzi@st.com;
giulio.ricotti@st.com; anna.moroni@st.com; sandro.rossi@st.com

***Abstract*— A novel integrated high-voltage high bandwidth linear amplifier for medical ultrasonic transmitter applications is presented in this brief. Compared to digital high voltage pulsers, linear amplifiers have many advantages, such as lower harmonic distortion and the capability of generating complex arbitrary waveforms for coded-excitation mode. The amplifier employs a current-feedback technique that overcomes the gain–bandwidth product limitation of a conventional voltage feedback amplifier, capable of generating a high output signal swing with a wide closed-loop bandwidth. The output stage is a mixed emitter follower and open drain architectures. The amplifier is designed and implemented using a 0.18-µm CMOS silicon-on-insulator process with 200 V components. When driving a load of 50 pF in parallel with 100 Ω, it's capable of transmitting a sine-wave signal at a frequency of up to 20 MHz, a maximum signal swing of 180 Vpp, a second-order harmonic distortion (HD2) lower than −43 dB and a maximum slew rate of 12 V/ns with only 20 mW average power dissipation with 0.1 % duty cycle.**

Keywords*— *BCD technology, high-voltage ICs, Current-feedback amplifier (CFA), high-voltage (HV) power amplifier, ultrasound transmitter, linear amplifier, ultrasound.

I. INTRODUCTION AND STATE OF THE ART

Today echography imaging is widely used as diagnostic in biomedical applications and its usage is increasing. A typical ultrasound system is composed by a transmission portion (TX) that excites transducers with high voltage signals up to 200 Vpp, in order to guarantee a good penetration depth of the ultrasonic beams, and a receiving chain (RX) which has to acquire, process and convert echo-signals. The transducers are placed inside the probe and connected by coaxial cables. In the state of the art of high-level high-performances systems, a TX linear driver is usually adopted by the main players of the market, because it ensures the best excitation of the elements, amplitude apodization, high harmonic performances, and full flexibility to generate and tune complex arbitrary waveforms. Discrete solutions often using bulky transformers are the most-used architectures [1][2]. Reliability, high manufacturing cost and area, limit this approach. Moreover, to enhance image quality, new techniques, such as tissue harmonic imaging (THI), have been developed to produce images of better quality and contrast as compared with conventional ultrasound techniques [3]. In THI, the ultrasonic energy is transmitted in a fundamental frequency to the transducers, and an image is realized by using the second-order harmonic distortion (HD2) content of the received signal, which is generated by the inherent nonlinearity of the body tissue. Usually, the B-mode THI ultrasound technique requires an output voltage swing up to 180 V_{pp} with a frequency from a few megahertz up to 12 MHz and a signal HD2 of less than −40 dB. The main problem of using pulser driver transmitters is the high harmonic components generated, that produces and HD2 between −30 to −40 dB [4]. For this reason, the design of an integrated HV linear power amplifier as transmitter for enhanced ultrasonic imaging is needed. Their use is today rather limited because of the high manufacturing costs, power dissipation and space constraints. The possibility of integration in a single chip solution fitting ultrasound system performances can change this market segment, renewing the interest to study full integrated linear drivers, also for portable application [5]. In this work a solution using HV-SOI-BCD technology has been studied and realized to overcome the main limitations of the state of art [6][7]. The first challenge in the design of an integrated HV linear amplifier is to ensure wide bandwidth and low HD2 at the same time, without exceeding the power limitation of a single chip device. A large signal swing can be obtained by using HV power MOSFET technologies. To push for higher bandwidth, some published works such as [6] use lower voltage rating processes to trade the voltage swing of the transmitters (90 V_{pp}) in exchange of a shorter transistor gate length that can improve the bandwidth of the operational amplifier, but reducing the penetration depth. In order to run over this drawbacks, some commercial products such as Supertex MD2130 [8] are integrated in a single chip. The proposed fully integrated HV linear operational amplifier uses a current feedback technique that can overcome the gain-bandwidth product (GBW) of the voltage feedback topologies. It can reach 180 Vpp output signal swing without using an external transformer, a bandwidth up to 20 MHz that is more than twice the one presented in [1], and an HD2 of less than −40 dB without pre distortion on input signal. The paper is organized as follows: Section II describes the adopted BCD technology and presents the circuit topology of the integrated amplifier. Measurements setup and results are analyzed in Sections III. Section IV draws conclusions.

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II. CURRENT FEEDBACK AMPLIFIER IN BCD-SOI TECHNOLOGY

The implemented architecture is shown in Fig.1. The input stage works as a buffer between inputs in_p and in_m, which is a low impedance input with an equivalent resistor R_i. The current flowing on R_i is composed by a DC current I_{err} and the AC feedback current I_{fb}. This current is multiplied by a factor N and it's carried to the high voltage gain node G, where it is converted into a voltage by the resistance R_G that creates, with the total capacitance C_C of node G, the dominant pole of the single stage amplifier

$$f_0 = 1/(2\pi R_G C_C). \quad (1)$$

All mosfets connected to G node have low current capability, so an efficient output buffer is necessary to drive the load. To reach high linearity, the feedback loop is realized by HV poly resistors on top of a second poly layer to shield against the substrate voltage modulation. If $R_i \ll R_1 \parallel R_2$, the closed loop bandwidth tends to

$$f_C \approx 1/(2\pi R_2 C_C). \quad (2)$$

The loop gain G_{loop} can be calculated as

$$G_{loop} = - (NR_G/R_2)\cdot\{1/[1+R_i(R_1||R_2)]\} \quad (3)$$

and the closed loop ideal gain G_{id} is

$$G_{id}=1+(R_2/R_1) \quad (4)$$

with R_2 fixed to 20 KΩ and R_1 digitally selectable between 225 Ω and 1.43 KΩ in case of high gain (HG, 90) or low gain (LG, 15) respectively. The possibility to change the gain setting can relax the input DAC resolution when low output signals are generated.

The adopted BCD-SOI technology embeds 0.18 µm CMOS transistors and 200V complementary power DMOS with Vgs=|3.3| V.

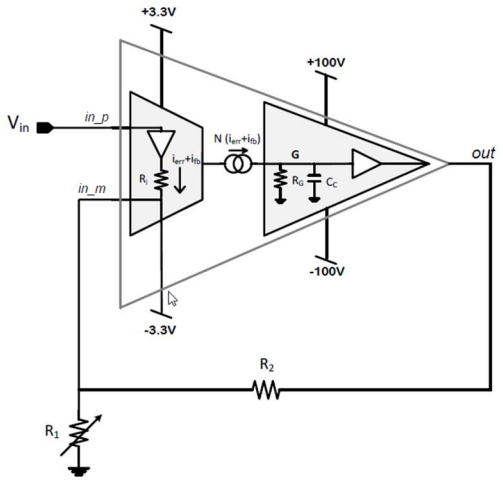

Fig. 1. Functional description of the linear amplifier architecture.

A. Input stage

Fig. 2 shows the schematic details of input stage. This stage is designed with 1.8V CMOS transistors. Mosfets M_2 an M_3 are designed to create a very low in_m input impedance

$$R_i=1/gm_2 \parallel 1/gm_3 \quad (2)$$

while keeping low the parasitic capacitance. The input structure consists in two LV branches biased by an high current I_1 able to optimize trans-conductance values and the dynamic range, plus a third branch biased by a current I_2 that feeds the HV stage. Both the quiescent currents are digitally selectable. This biasing solution makes I_1 independent from I_2, allowing the possibility to choose the gain of the stage while keeping low the power consumption by the HV supplies. To further minimize the power consumption, this opamp is biased just few microseconds before the pulse generation and turned-off during the long receive period, closing all the grey switches shown in fig.2.

Another design challenge is to minimize the output voltage glitches, mainly caused by the input offset during the turn-on/off phase and by the switches charge injection, that can produce unwanted artifacts in the image. For this reason, a digital state machine controls the turn-on/off phases, pushing out of transducer bandwidth the glitch energy. The measured input offset is 10 mV at 3-σ over a statistical Gaussian distribution (200 samples measured on two different lots).

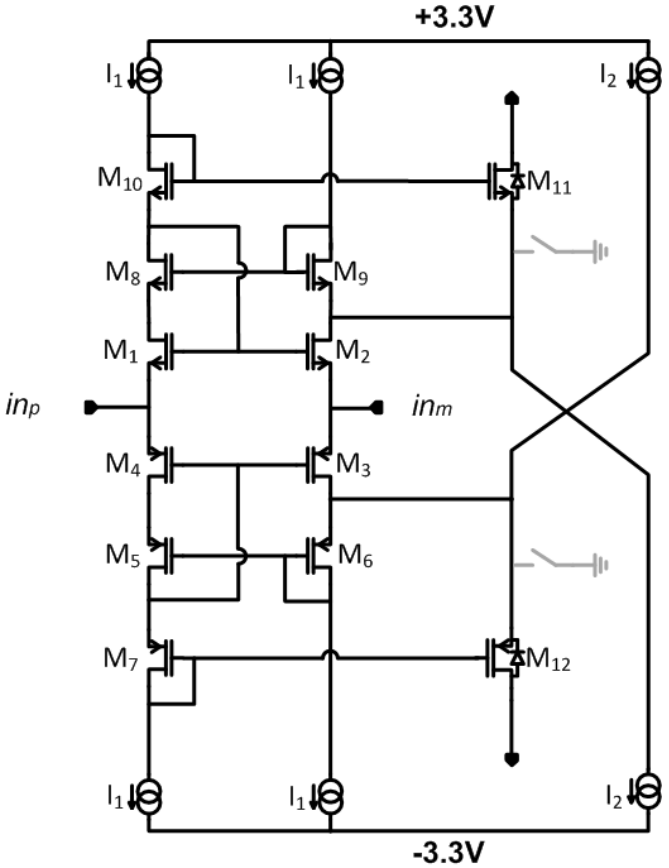

Fig. 2. Schematic of the linear amplifier input stage.

B. *HV trans-impedance stage*

Fig. 3 shows the details of the HV trans-impedance stage. The current coming from the input stage is mirrored by a Wilson topology that increases the output impedance of this mirror and determines the trans-resistance R_G. A mirror factor of 2 is chosen to drive the total capacitance C_C of node G at frequencies higher than 20 MHz. The parasitic capacitances on this node must be negligible compared to the 250 fF metal-over-metal (MOM) capacitor (the best solution in terms of linearity) placed to compensate the structure, so M_{18}-M_{20} and M_{25}-M_{26} have low size and low current capability. Additional mirrors M_{21}-M_{22} and M_{23}-M_{24} allow to decouple the parasitic capacitances C_{p1} and C_{p2} to the critical signal path.

The G node drives the output buffer in a double source follower configuration polarized in class-AB. This buffer is able to drive up to 50 pF as load with 12 V/ns slew-rate (SR). To increase the output current capability up to 3 A, a current multiplier is used in common drain configuration (M_{29} M_{30}) driven directly by the source follower current. Mirrors M_{31}-M_{32} and M_{33}-M_{34} stole exactly the current of the source follower stage, limiting the DC power consumption in the output branch. The current signal flowing on R_3 and R_4 resistors increases the current of mosfets M_{29} M_{30} till their saturation. This structure introduces a loop compensated by C_3 and C_4. When the linear amplifier is active, the total quiescent current from HV supply is $50 \cdot I_2$. Best performances are measured with I_1= 2 mA and I_2= 100 µA where power consumption is 20 mW at ±100V HV supplies. It goes to zero during the receiving phase when the linear opamp is fully turned-off.

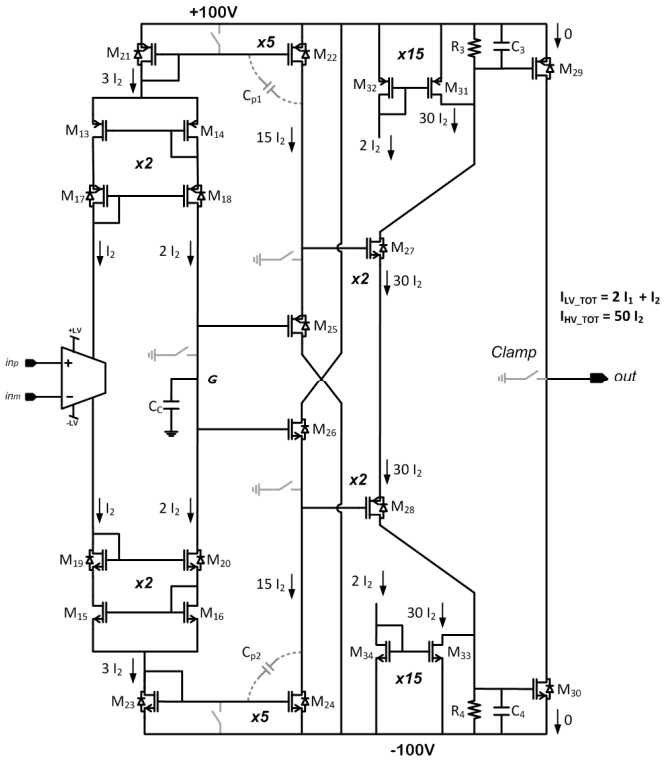

Fig. 3. Schematic of the linear amplifier HV trans-impedance stage.

III. MEASUREMENT RESULTS

The proposed operational amplifier has been fabricated by STMicroelectronics. Realized prototypes have been tested in a 48-pin quad-flat no-leads (QFN) plastic package. The whole op-amp occupies an area of about 6 mm² (Fig.4) and it is completely integrated, including also a high-voltage transmission switch to isolate the LV chain during TX and a clamp circuit.

The off-chip load impedance used for characterization comprises a 100 Ω resistor and a 300 pF capacitor. The input signal is provided through a National Instrument PXI-5421 16 bit 100 MS/s signal source while the output is probed on an 8 bit Rohde&Schwarz RTO-1024 Oscilloscope (2 GHz, 10 GS/s). The high and low voltage supplies are set to |100| V and |3.3| V respectively.

To avoid excessive self-heating, all the measurements have been carried out with a pulsed input signal having a duty cycle of 0.1 %. High gain configuration output transient is shown in fig.5: an output peak to peak voltage amplitude between 50 V and 180 V is able to guarantee the best performances at maximum gain condition. We also compared the performance of our HV power amplifier IC to an existing commercial product Supertex MD2130 [8] when both are driving a 0.1 % duty-cycle signal. The performance comparison between our amplifier, Supertex MD2130, and other states of the art is listed in Table I. This solution is the best for BW, area, integration, power consumption and slew rate, while it is comparable for all other parameters.

The closed loop frequency responses for typical output voltage swings at LG and HG configurations are shown in Fig.6. Simulations are also reported for comparison, showing a very good agreement. The measured -3dB bandwidths are 22 MHz and 20 MHz for LG and HG configurations, respectively. All stability analysis has been done both with small signal simulations superimposed to the large driving signal and step response transient analysis. In the worst operative condition, the phase margin is 36º.

Linearity performances have been analyzed through second harmonic distortion measurements. A six periods Gaussian enveloped input, typical in ultrasound systems, is been used for testing. HD2 measurements results vs frequency are reported in. Fig.7 for an output voltage of 180 Vpp in HG configuration and of 5 Vpp for LG configuration. HD2 values are below −42 dB with input frequencies up to 6 MHz.

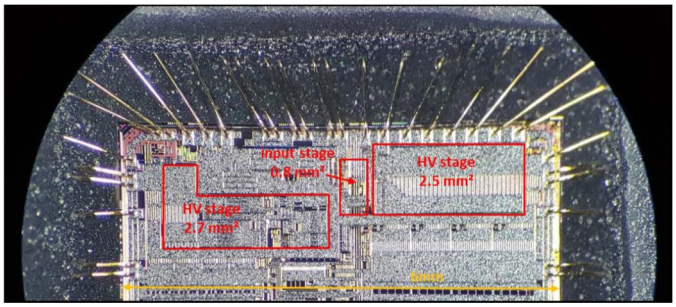

Fig. 4. Chip photograph

TABLE I. PERFORMANCE COMPARISON BETWEEN THE PRESENTED INTEGRATED LINEAR AMPLIFIER AND PUBLISHED WORKS

	This work		[1]	[8]	[6]	[7]
Linear Gain	15	90	45	NA	110.9	90
Output load	300pF || 100Ω		220pF || 1kΩ	220pF || 1kΩ	150pF || 100Ω	300pF || 100Ω
HD2	-48 dBc	-43 dBc	-63 dBc	-46 dBc	-43 dBc	-50 dBc
Bandwidth	22 MHz	20 MHz	8.7 MHz	15 MHz	6.5 MHz	8.6 MHz
Voltage swing	25 Vpp	180 Vpp	180 Vpp	180 Vpp	90 Vpp	180 Vpp
Power supplies	2		2	1	2	2
Output transformer	No		Yes	Yes	No	No
External DAC	Yes		Yes	No	Yes	Yes
Power consumption while ON	4 mW	20 mW	62 mW	152.5 mW (including digital circuits and DAC)	37 mW	NA
Slew rate	12 V/ns	12 V/ns	NA	NA	+ 2 V/ns -2.2 V/ns	4 V/ns
Silicon area	6 mm^2		13.8 mm^2	25 mm^2 (PKG)	1 mm^2	NA
Technology	BCD8 - SOI 0.18µm 200V process		0.7 µm CMOS – SOI process	NA	0.35 µm 200 V process	1 µm 200 V process
Current capability	3 A	3 A	NA	3 A	0.7A	NA

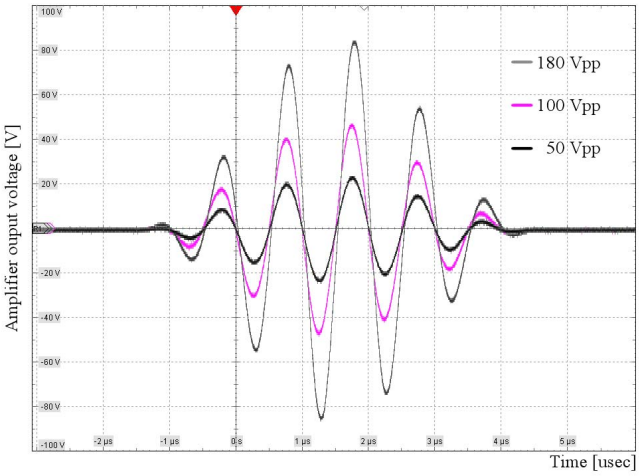

Fig. 5. Output voltage signal acquisitions at High gain, changing the amplitude of the 6 periods hanning windowed input voltage signal at 1 Mhz, load 300 pF || 100 Ω.

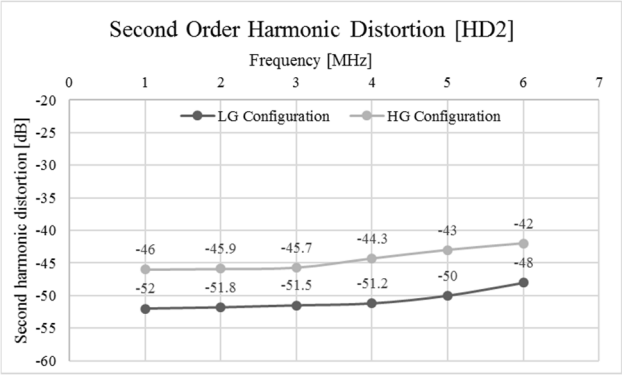

Fig. 6. Second Harmonic performances of the linear amplifier ouput voltage at High gain (180 Vpp) and Low gain (5 Vpp) settings, 6 periods hanning windowed input signal, load 300 pF || 100 Ω.

IV. Conclusion

This work shall cover the design of a fully integrated high voltage linear amplifier able to satisfy the main specification of a high-end TX channel for medical echography. It can generate an output voltage signal up to 180 peak-to-peak while driving a 300 pF || 100 Ω load (Fig.4). The measured closed-loop bandwidth is 20 MHz in HG corresponding to a GBW > 2 GHz and 22 MHz in LG. Five patents are filled to protect the novel solutions. The cost reduction given by the full silicon topology in a reduced area can address a wide range of applications in addition to the traditional High-End platform using linear approach.

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