aBCD18 - an advanced 0.18um BCD Technology for PMIC Application

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Abstract—**We present a new advanced 0.18um BCD(Bipolar-CMOS-DMOS) technology with the key features being a 40V HV-MOS and an SSTC(Sidewall Selective Transistor Cell) type EEPROM as well as complimentary available analog devices such as a high gain BJT, 4fF/um^2 MIM capacitor, and 10k Ω/sq. poly resistor. To reduce device area and enhance latch up immunity, a 15um depth deep trench isolation process has been developed, which will help to significantly reduce the chip size.**

I. INTRODUCTION

BCD processes are widely used in the variety of areas such as in large displays (TV and monitor), small displays (hand-held and mobile devices), POE (Power of Ethernet), and storage controller chips. Recently, many companies have made an effort to combine a power management, logic, audio and communication functions in a single chip. Therefore, more and larger logic contents have been integrated with a BCD technology [1-3]. Furthermore, to reduce the high voltage blocking area some companies are developing the DTI (Deep Trench Isolation) process which is an elegant alternative to junction isolation [4-7]. This paper presents the a(advanced)BCD1840 process technology based on 0.18um logic platforms with high density EEPROM and the DTI process.

The aBCD1840 for 0.18um smart power SOC (Systems On a Chip) process architecture presented here was developed mainly for purpose of foundry services. Key features of this process are:

a. Industry compatible, shallow trench isolation (STI) for 0.18um CMOS baseline process, metal and oxide CMP (Chemical Mechanical Polishing), dual work function poly gate with cobalt silicide, up to six metal layers, 1.8V and 5.0V CMOS transistors, high resistance poly silicon resistors and high capacitance MIM (Metal-Insulator-Metal) capacitors.

b. Substrate-isolated n-type high voltage LDMOS (Lateral Double diffused drain MOS) transistors for 12V ~ 40V operation and low specific on-resistance (Rsp) of 15~50 [mΩ*mm^2] which makes use of a multi-RESURF technique based on optimized device structures.

c. Asymmetrical high voltage CMOS transistors with gate and drain voltages, Vgs=5.0V and Vds =12~40V for use in HV analogue circuitry and NVM (Nonvolatile Memory) periphery for instance.

d. By adding only 4 photo process steps, high density EEPROM (Electrically Erasable and Programmable Read Only Memory which utilizes the SSTC (Sidewall Selective Transistor Cell) structure with FN (Fowler-Nordheim) tunneling mechanism for programming and erasing operations.) is embedded.

II. PROCESS ARCHITECTURE

Starting material is a p-type silicon wafer with resistivity of 10 ohm-cm. NBL (N$^+$ Buried Layer) is formed on it using antimony implants. NBL is used for high voltage device isolation to the p-type substrate. Then, a p-type epitaxial layer is grown on the NBL to achieve a high breakdown voltage up to 60V. In this process, there are high voltage twin well

Fig. 1. Key Process Flow of aBCD1840

formations for the HV devices. HV wells are designed to

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achieve high breakdown voltage by proper ion implant condition and additional well drive-in anneal. To get lateral isolation of each device, DTI is processed. Its minimum width and typical depth are 1.6um and 15um respectively, followed by a field stop implant at the bottom of the trench to stop the field transistor from turning on. Then gap-fill is performed with a thin liner oxide plus un-doped poly silicon is processed. Then Poly CMP is processed to get flat topology for the next photo lithograph processes. STI is consecutively processed after DTI process. After the trench isolation process, P-Body is formed to make the n-type LDMOS transistor. The EEPROM cell formation is processed after the low voltage twin well formation. Fig.1. shows the aBCD1840 schematic process flow tailored for the key features described above. The process offers up to six levels of metal with a top metal of 4.0um thickness using aluminum. Electrical parameters for 1.8V/5.0V CMOS, BJT, diode, resistor, capacitor, and EEPROM are summarized in Table 1. 1.8V/5.0V CMOS is fully compatible with an industry standard 0.18um logic process.

LV_CMOS	VT [V]	IDSAT [±uA/um]	Ioff [±pA/um]
1.8V NMOS	0.43	600	< 10
1.8V PMOS	-0.51	260	< 10
5.0V NMOS	0.76	574	< 10
5.0V PMOS	-0.79	263	< 10
BJT	**Hfe**	**BVCEO [V]**	
Verticle NPN	54	22	
Substrate PNP	44	50	
DIODE	**VF [V]**	**VR [V]**	
Bulk Zener	0.74	6.5	
Schottky	0.25	17	
RESISTOR	**Res. [Ω/sq.]**		
High-R	10K / 1K		
Low TCR	310		
CAPACITOR	**Cap. [fF/um²]**	**BV [V]@1fA/um²**	
High-K MIM	4	12	
SiN MIM	1	27	
EEPROM	**VT_PGM [V]**	**VT_ERS [V]**	**ID_ERS [uA/cell]**
SSTC type	5.0	1.2	20

Table 1. Electric Parameters for LV_CMOS, BJT, Diode, Resistor, Capacitor, and EEPROM

III. Key Device Characteristics

A. HVMOS Transistors

Fig. 2 shows the schematic cross section of the key devices in the aBCD1840 process. In the aBCD1840 process, LDCMOS transistors are provided as a power switch devices and EDCMOS transistors are also provided for high voltage driving circuitry. As shown in Fig.2, the n-channel LDMOS (nLDMOS) transistor has PBODY, while the p-channel LDMOS (pLDMOS) transistor has low voltage NW. Also, high voltage (20~40V) LDCMOS and EDCMOS transistors have the field oxide between the gate and the drain while low voltage (12~16V) LDCMOS and EDCMOS transistors do not. The 16V EDCMOS devices are used for EEPROM operational circuitry. Electrical parameters for the high voltage LDCMOS and EDCMOS transistors are listed in Table 2. For the high-side operation of all devices, the NBL layer and DTI are used in order to avoid the punch-through breakdown.

LDCMOS	Rsp [mΩ*mm²]	BV [±V]	VT [±V]
nLD40	45	59	0.91
nLD30	31.5	46	0.97
nLD20	18.5	32	1.00
nLD12	11.5	20	1.04
pLD40	126	56	0.80
pLD30	85	45	0.81
pLD20	48.5	34	0.82
pLD12	32.5	22.5	0.80
EDCMOS	**IDSAT [±uA/um]**	**BV [±V]**	**VT [±V]**
nED40	260	52	0.80
nED30	295	45	0.82
nED20	320	28	0.80
nED12	350	18	0.79
pED40	127	64	0.77
pED30	130	56	0.78
pED20	135	32	0.80
pED12	140	21	0.78

Table 2. Electric Parameters for high voltage LDCMOS and EDCMOS

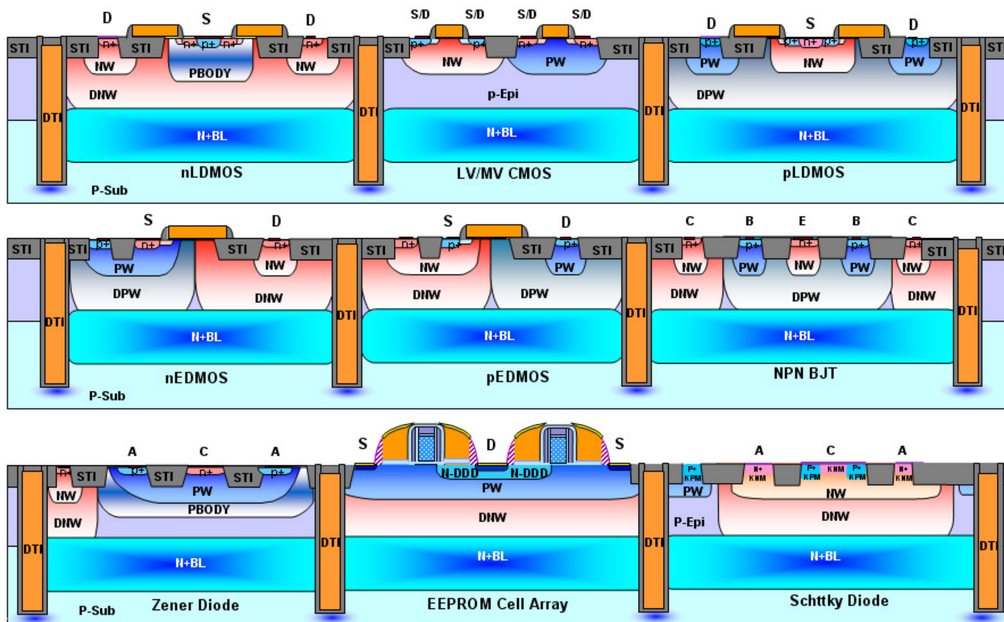

Fig. 2. Schematic Cross sections of aBCD1840 Active Devices

Fig. 3 shows the current - voltage characteristics of the 40V nLDMOS and pLDMOS. For the nLDMOS, a specific on resistance of Rdson = 45[mΩ*mm^2] at a breakdown voltage (BV) of 59V has been achieved while for that of pLDMOS is about 125 [mΩ*mm^2] at the BV of 56V. Fig. 4 shows a SEM cross sectional image of the nLDMOS transistor with PBODY.

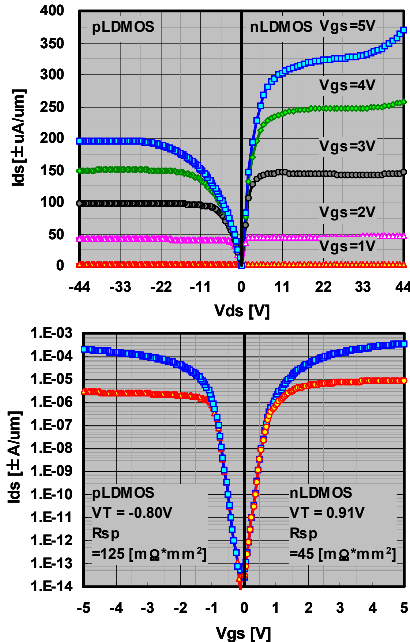

Fig. 3. I_V Characteristics of LDCMOS

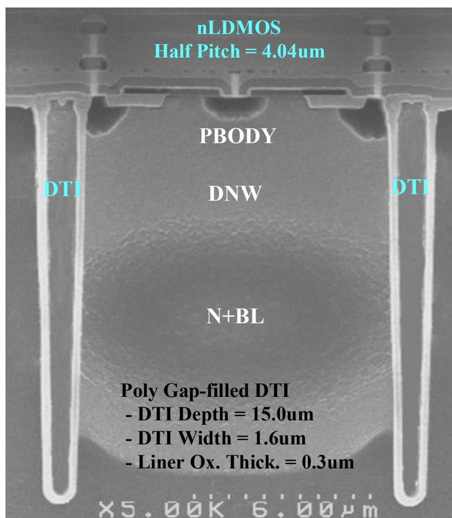

Fig. 4. SEM Micrograph of nLDMOS

Fig. 5 shows the current-voltage characteristics of the 40V nEDMOS and pEDMOS. For the nEDMOS the saturation current and BVdss are 260 [uA/um] and 52V, while those of the pEDMOS are 127 [uA/um] and 64V respectively.

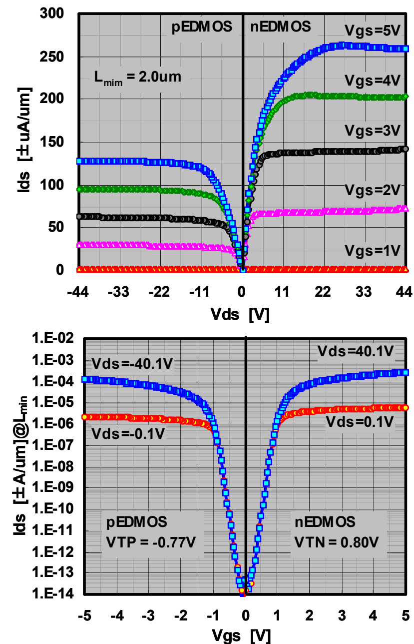

Fig. 5. I_V Characteristics of EDCMOS

As shown in Fig. 5, even at the minimum gate length, n/pEDMOS transistors have a fairly flat saturation region with no DIBL (Drain Induced Barrier Lowering), which demonstrates that they can be used for HV analogue blocks with satisfying analogue-circuit requirements. When compared to previously reported 0.18um BCD technologies, the LD- and EDCMOS transistors in aBCD1840 show much better electrical performance [1-3].

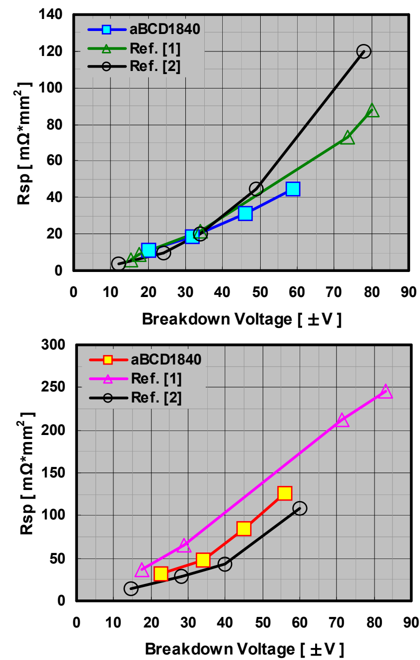

Fig. 6. FOM of nLDMOS and pLDMOS

Fig. 6 shows the Figure of Merit (FOM) between the

specific on-resistance and the breakdown voltage for the nLDMOS and pLDMOS. It shows that aBCD1840 technology has a competitive BV and Rdson performance to previous ones.

B. High Density EEPROM

Fig. 7 shows a TEM image of the SSTC type EEPROM cell along the bit line direction. The memory cell has low voltage p-well surrounded by deep n-well over NBL, STI, double layers of poly-silicon, and 2 layers of metals. As shown, the cell consists of three transistors: One transistor at the center for the floating gate and two transistors at the side walls for the select gates. The cell size is 0.95um^2 and only 4 photo mask process steps are used to form the cell. Both programming and erasing of the cell are performed by Fowler-Nordheim tunneling. The details of cell operation are given elsewhere [8].

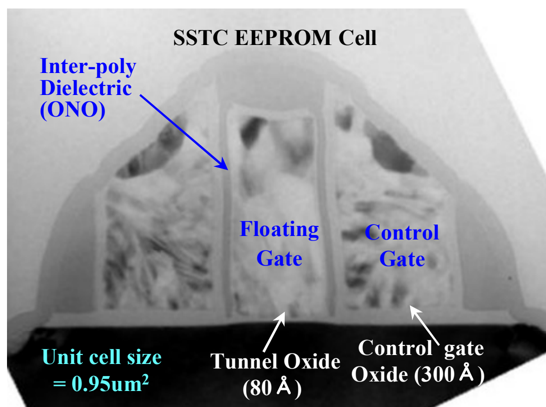

Fig. 7. TEM Micrograph of SSTC type EEPROM

Fig. 8 shows the Endurance characteristics of the threshold voltage distribution for a 1M (mega) macro cell based on 300K (kilo) program and erase stress cycles at room temperature.

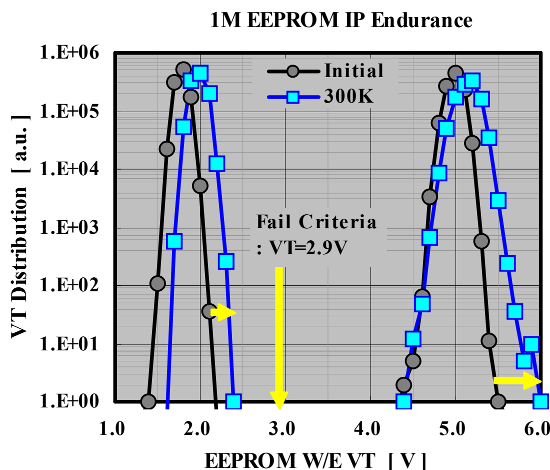

Fig. 8. Endurance Characteristics of 1M EEPROM

As shown, it has more than half a million cycles of endurance resistance. Over 10 years of Data Retention Life Time at 150℃ with 30K cycles of program and erase stressed samples has been demonstrated.

IV. SUMMARY

The aBCD1840 - advanced 0.18um/40V BCD technology of Magnachip - was developed by integrating an industry standard 0.18um backbone process with 5V CMOS, high voltage and power switch devices, BJT, high density EEPROM, and analogue components for proper combination of high voltage well junction isolation and deep and shallow trench isolation. High voltage devices such as LDCMOS and EDCMOS have been developed in full range of operating voltage from 12V to 40V with very competitive specific on-resistance and good output performance. As for options, MIM capacitor with 1~4 [fF/um^2], high poly resistor with 10 [kΩ/sq] and zero TC (Temperature Coefficient) resistors are available using an optional mask layers for each component.

The aBCD1840 technology is expected to be a very useful backbone process technology for applications in the large and small display areas, audio amplifiers, and mobile PMIC (power management IC) applications.

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