A 54-69.3 GHz Dual-Band VCO with Differential Hybrid Coupler for Quadrature Generation

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***Abstract*—This paper presents a 40nm CMOS transformer-based dual-band VCO with differential hybrid coupler for I/Q generation. The average phase noise of the combination over the 54 to 69.3GHz tuning range is -90dBc/Hz at 1MHz offset while the best FOM value is 177dB. Along the wide tuning range from 54 to 67GHz, the I/Q mismatch of the hybrid coupler is less than 3°. The area of the hybrid is only 60μm*65μm.**

I. Introduction

The high speed of advanced CMOS devices enables wireless applications at mm-wave frequencies. The IEEE-802.11ad standard covers the 57-66GHz frequency range for multi Gbps wireless communication. Covering this 9GHz band is challenging for the frequency synthesis of transceiver ICs, especially in direct conversion architectures, which, in addition to superheterodyne, requires the LO signal in quadrature format. Classical quadrature VCO (QVCO) approaches [1] suffer from phase noise degradation compared to differential VCOs due to the presence of the active coupling circuitry between the two VCOs and because they operate at a frequency where the tank impedance is not maximal. Further, the parasitics of the coupling network reduce the tuning range.

One of the problems for mm-wave VCOs is that varactors have a Q factor below 15, which complicates the trade-off between phase noise and tuning range. Several tuning range enhancing techniques have already been presented. For example, subharmonic injection locking [2] eases the trade-off between tuning range and phase noise by synchronizing with a lower frequency where varactors have higher Q. However, this requires two oscillators leading to a large power and area consumption. Moreover, specific calibration techniques are needed to guarantee locking. In [3], an LC-VCO combined with distributed components achieves a 7GHz tuning range and -90dBc/Hz phase noise at 1MHz offset. However, more tuning range is needed to compensate for PVT variations. Other techniques like an LC-tank using a slow-wave tunable transmission line [4] improves the tuning range at the cost of area, especially if a QVCO would be targeted instead of a VCO. In [5] a polyphase filter is used for passive I/Q generation. However, this solution is quite lossy and it requires capacitors that are comparable to parasitic capacitances and small resistors, leading to a poor predictability of the final phase accuracy. Moreover, the low impedance levels of a mm-wave polyphase filter limit the voltage swing and require strong buffering, leading to a large power consumption.

In this work, frequency synthesis and quadrature generation are realized independently. To achieve a wide tuning range transformer-based dual-band VCO is used. It covers a 15.3GHz band centered at 61GHz with good phase noise (-91.4dBc/Hz@1MHz offset). For quadrature LO generation, a differential hybrid coupler is used. Compared to previous on-chip implementations [11]-[13], this hybrid consumes less area. The phase error is lower than 3° within the 9GHz band of interest.

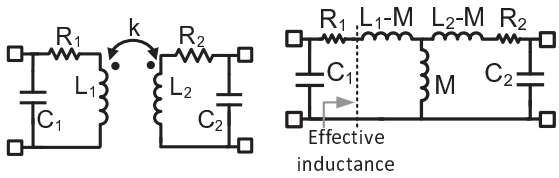

Fig. 1: Transformer-based resonator (a) and its equivalent circuit (b).

The outline of this paper is as follows. Section II focuses on the analysis and design of the dual-band VCO. Section III discusses the design of the compact on-chip hybrid. Section IV reports the measurement results. Section V concludes the paper.

II. Dual-band VCO

A. Review of a transformer-based dual-band VCO

Fig. 1a shows a transformer-based resonator with two potential oscillation modes. The load at the secondary winding can be reflected to the primary as Fig.1b indicates. For a simplified case when L_1=L_2=L and C_1=C_2=C, the low and high resonance frequencies, f_l and f_h respectively, are found to be $f_{l,h}=1/\sqrt{LC(1\pm k)}$, which indicates that a lower k factor brings the two frequencies closer together. Combined with capacitive tuning, the dual-band resonator becomes wideband. Compared to a switched-inductor technique, a transformer-based resonator has no switch in the signal path, which translates to better phase noise.

Fig. 2a presents a dual-band VCO based on a different resonance frequency seen from Z_{11} and Z_{12}[8]. By enabling either G_{m1} or G_{m2}, the VCO operates in a low- or high-frequency band. However, the required low k factor reduces the loop gain necessitating large transductance for G_{m2} to ensure startup. This results in both high power consumption and more parasitic capacitance. In the dual-band resonator of Fig.2b the $-G_m$ cell is always enabled [6]. For low-band operation, G_{m2} is switched off. When G_{m2} is activated, a negative magnetic flux at L_1 is induced, reducing the effective inductance seen by $-G_m$, yielding a higher oscillation frequency. Compared to

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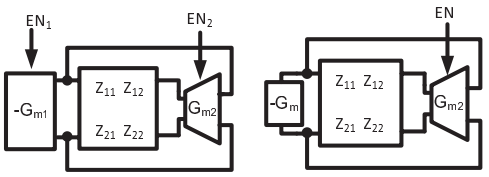
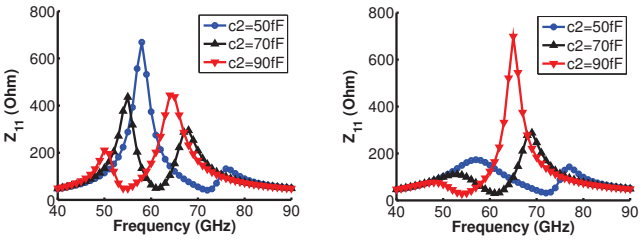


(a) (b)

Fig. 2: a) Dual-g_m transimpedance VCO. b)Single-g_m dual-band VCO.



(a) (b)

Fig. 3: Z_{11} at low-band (a) and high-band (b) operation.

the previous topology, the low coupling factor enables dual-band operation without degrading the loop gain, such that the $-G_m$ cell can be low power and small. This is the prototype of our implementation.

The analysis above remains valid for an asymmetric resonator when $C_1 \neq C_2$. The impedance of Z_{11} for high and low bands is shown in Fig.3 for different C_2 values. To make both sides oscillating around 60GHz, we choose L_1=L_2=100pH, C_1=70fF, R_1=R_2=4Ω and k=0.2. Further, g_{m2} is 8mS when the high band is activated. As Fig.3a shows, a smaller C_2 gives a higher center frequency for the low band since less capacitance is seen by Z_{11}. The impedance in the low band increases as C_2 decreases, which suggests that a smaller C_2 leads to a higher quality factor in the low band. On the other hand, when C_2 increases much, the impedance in the low band is lower than in the high band, such that the VCO oscillates in the high band. This can be intuitively explained as follows: for low-band operation, a small C_2 reduces the AC current in the secondary winding. As a result, the loss from R_2 is lower. When C_2 is much bigger than C_1, the oscillation frequency is determined by the load at the secondary winding as if C_1 is a parasitic capacitor. The impedance for the high band is shown in Fig.3b. A larger C_2 is preferred for a higher quality factor. The equivalent model for the high band is more complicated because of the feedback loop established by g_{m2}. Further quantitative analysis in [6] concludes that the quality factor improvement for one band will degrade the other one. For a dual-band VCO designed for wideband operation, such that the high band and the low band overlap, it is found that both bands need to be designed for similar quality factor.

B. 60GHz dual-band VCO design

Fig 4 shows the schematic of the dual-band VCO, which is based on the analysis in the previous section. The transformer has a coupling factor k of 0.2. Further, L_1 = 120pH and L_2 = 140pH. Their quality factor is 15 at 60GHz. A tail inductor of 90pH is used to enhance the loaded Q_{tank}[9]. A

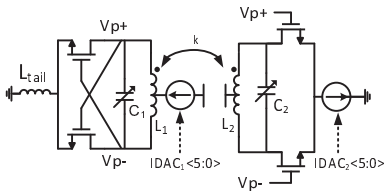


Fig. 4: Dual-band VCO schematic.

5-bit coarse tuning is used for C_1 and C_2 to lower the K_{VCO}. Both capacitances range from 27 to 40fF with an average Q of 14 around 60GHz. To limit the close-in phase noise caused by flicker noise, the cross-coupled pair is biased by a pMOS tail current source rather than an nMOS one. The current DACs ($IDAC_1$ and $IDAC_2$) control the DC current that is derived from a bandgap reference. Further, programmable RC filters (not shown) are used to suppress the noise from the bandgap reference.

According to the above analysis, the minimum C_2 value is used in the low band for low phase noise as Fig. 3a suggests, while the maximum value for C_2 is used to extend the lower frequency at the cost of phase noise. Similarly, the maximum C_2 value is used in the high band for better phase noise according to Fig. 3b and a lower C_2 is used to further push the VCO to higher frequencies.

III. ON-CHIP HYBRID COUPLER

A Lange coupler is often used for broadband quadrature generation. However, the transmission line based design is area consuming for on-chip implementation at 60GHz. To save area, a differential transformer-based hybrid is used. It is the differential equivalent of the single-ended quadrature coupler shown in Fig. 5. By doubling the circuit, a compact differential quadrature hybrid is obtained. The grounded capacitors are half of the ones in the single-ended version. The design equations for capacitors C_m and C_g are shown in Fig. 5. These capacitors consist of a MOM capacitance part (46fF for C_m and 33fF for C_g) and parasitic capacitance from preceding or succeeding buffer stages. Moreover, wide metal lines are used in the inductors, which have a lower sensitivity to PVT variation compared to small active or passive components. In this way, the phase error is more predictable from sample to sample. The quadrature circuit has four ports. The isolated port is terminated by a 50Ω polysilicon resistor. The transformer with k = $1/\sqrt{2}$ uses primary and secondary inductors of 110pH.

The hybrid outputs are connected via a transformer to pseudo-differential buffers (see Fig. 6). Due to the high impedance at the gate of transistors, the transformer has a 1:3 turn ratio for impedance matching.

For characterization of the system, a high-frequency output and a downconverted output are provided as follows. As quadrature measurements at mm-wave are difficult, only the I path is brought off-chip at mm-wave frequencies via a buffer, while the Q path has a dummy load. A passive mixer is used to downconvert the I/Q signal to measure the quadrature accuracy. To this end, an external single-ended LO signal is used, which is converted to a differential signal using an on-chip balun.

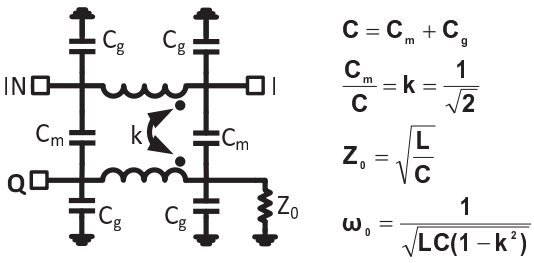
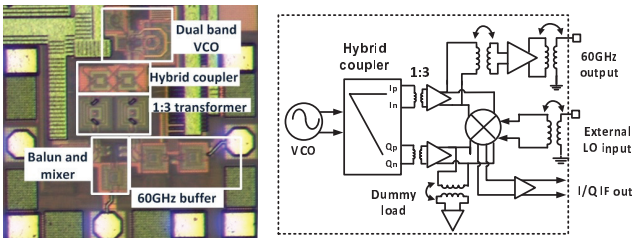


Fig. 5: Single-ended equivalent of the differential hybrid.



(a) (b)

Fig. 6: Chip micrograph (a) and (b) schematic of the complete circuit, including VCO, hybrid and test circuitry.

IV. Experimental Results

The chip is fabricated in a 1P10M 40nm CMOS process without ultra-thick metal layer option (see Fig. 6a). The size of the dual-band VCO and the differential hybrid coupler are 110μm x 90μm and 2 x 60μm x 65μm, respectively.

To obtain a specific oscillation frequency, several combinations of C_1 and C_2 can be used but the low band with minimal C_2 and the high band with maximal C_2 is preferred as is explained. As an illustration, a frequency of 55.8GHz has been realized with two values of C_2 (see Fig. 7). It is seen that a non-minimum C_2 value yields a phase noise penalty of 2dB at 1MHz offset. By using minimum and maximum C_2 values in the low and high band, the VCO covers a range from 55.5GHz to 62GHz (low band) and 61.9GHz to 67.8GHz (high band). Phase noise has been measured over the 57-66GHz unlicensed band for the 802.11ad standard. Among the four frequencies that need to be synthesized (58.32GHz + (n-1)×2.16GHz, n=1 to 4), phase noise is highest for channel 3 (n=3) and lowest for channel 1 (see Fig. 8 and also Fig. 9).

To further enlarge the tuning range, C_2 is also tuned, which extends both bands with 1.5GHz. The measured phase noise for tunable C_2 is marked with triangles in both bands in Fig. 9. Clearly, phase noise in the high band is worse than in the low band, partially because G_{m2} and I_{DAC2} are activated.

The negative G_m cell consumes 8mA in both bands, while the G_{m2} cell consumes 4mA when activated. The FOM ranges from -173dB to -177dB. In both bands, V_{DD} is 1V. The K_{VCO} varies from 0.7 to 1.2GHz/V along the fine tuning voltage.

When G_{m2} is off while a minimum value for C_1 and a large C_2 are used, the shift of the default oscillation mode to the high band is measured. This is consistent with the analysis on Fig.3a. The VCO oscillates at 67GHz instead of at 60GHz with

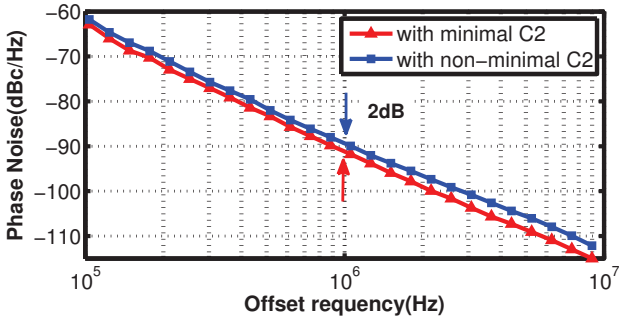


Fig. 7: Phase noise measured at 55.8GHz with (non)optimal $C_{1,2}$ combinations.

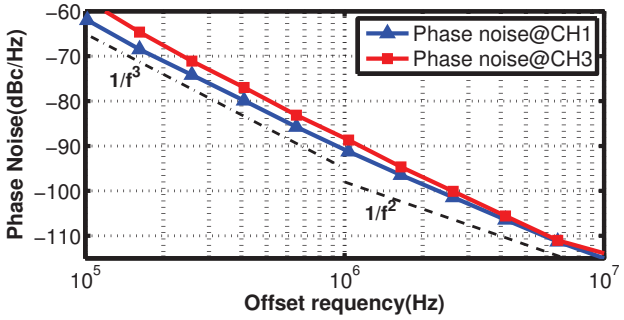


Fig. 8: Measured phase noise at channels 1 and 3 of the 802.11ad standard.

a phase noise of -87dBc/Hz at 1MHz offset. However, tuning range is limited because a small C_1 and a large C_2 are required to ensure a sufficient distinction of the tank impedance between the two bands in order to avoid two concurrent oscillations. It is not recommended to work in this mode.

Table I summarizes the performance of our circuit and compares it to other mm-wave VCO designs. With a small area consumption this VCO achieves the highest tuning range with comparable phase noise and FOM.

The hybrid coupler is implemented with top level metals. To reduce undesired couplings, all routing metal lines are orthogonal to each other. To measure the I/Q imbalance, both I/Q outputs are downconverted to 200MHz. The measured I/Q phase error along the VCO tuning range is shown in Fig.10. For the 9GHz band of interest, the maximum error is less than 3°. The measurement accuracy of amplitude mismatch and insertion loss is limited by the buffers. The simulated amplitude mismatch and insertion loss have a worst-case

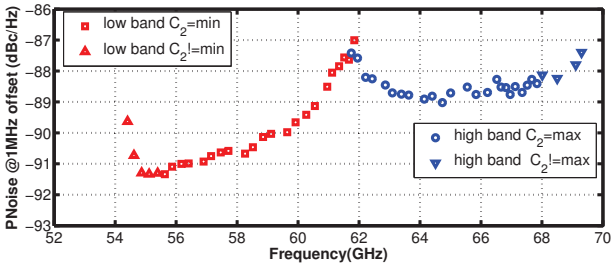


Fig. 9: Phase noise at 1MHz offset versus oscillation frequency.

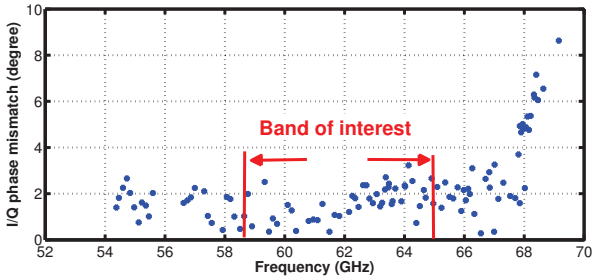


Fig. 10: Quadrature phase error versus frequency.

TABLE I: VCO performance summary and comparison to state-of-the-art.

REF	TMTT '10[3]	JSSC '12[4]	JSSC '09[7]	**This work**
Frequency (GHz)	52-61	43.2-53	55.7-61.1	**54-69.3**
TR(%)	17	22.9	9.3	**26**
Phase Noise (dBc/Hz)	-90/-99.4 @1MHz	-97.5/-99 @1MHz	-88/-91 @1MHz	**-87/-91.4 @1MHz**
Power(mW)	15	16	8.1	**8/12**
FOM* (dB)	-172/-182	-180	-174/-177	**-173/-177**
VDD(V)	1.2	1.2	0.7	**1**
Process	65nm	65nm	90nm	**40nm**
Area(mm^2)	0.05	0.0275	0.01	**0.012**

*FOM = PN(Δf) - 20log($f_0/\Delta f$) + 10log(P_{diss}/1mW)

value of 0.8dB and 2dB, respectively. Table II compares the proposed hybrid to related designs, which are all single-ended. Therefore, to compare the area we divide the area of our realization by two. This work consumes the least area and has a good I/Q accuracy within the band of interest. Further, Table III compares this work to other techniques to generate I/Q signals around 60GHz. We achieve the highest tuning range with relatively low area and core power.

V. Conclusions

For mm-wave LO generation in I/Q format over the 57-66GHz frequency band, we realized in 40nm CMOS a combination of a transformer-based dual-band VCO and an on-chip hybrid. This circuit has a tuning range from 54GHz to 69.3 GHz and phase noise from -87 to -91.4dBc/Hz at 1MHz offset. With an area of only 0.012mm^2 it consumes between 8mW and 12mW. Over the 57-66GHz frequency band the phase error is only 3°.

TABLE II: Hybrid performance summary and comparison to state-of-the-art.

REF	CICC '11 [10]	RFIC '11 [11]	SiRF '13 [12]	JSSC '09 [13]	**This work**
Frequency (GHz)	55-65	40-80	50-75	58-65	**54-67**
Phase Error(°)	2-4	$\pm 5^2$	3	13	$\leq$**3**
Amplitude mismatch (dB)	$\pm$1.5	$\pm 0.5^2$	0.3	1.5	**0.8**^{2}
Insertion Loss (dB)	0.7	1.5^2	$<$1	2.5/4	**2**^{2}
Area(μm x μm)	70 x 80	90 x 150	200 x 180	280 x 370	**65 x 60**^{1}
Process	65nm	45nm	90nm	90nm	**40nm**

1: Normalized to single-ended hybrid. 2: Simulated

TABLE III: Comparison to other quadrature LO generation approaches.

REF	JSSC '11 [2]	ISSCC '13 [14]	JSSC '11 [15]	**This work**
Quadrature generation	Sub-harmonic injection locking	In-phase injection locking	Hybrid (Single-ended)	**Hybrid Differential**
Frequency (GHz)	58-63	57.8-68.3	57.6-65.6	**54-69.3**
Phase Noise (dBc/Hz)	-95 @1MHz	-94 @1MHz	-112 @10MHz	**-87/-91.4 @1MHz**
Core Power (mW)	14.4$\sim$52.8	11.4	9	**8/12**
Area(mm^2)	$\sim$0.04	$\sim$0.04	n.a.	**0.02**
Process	65nm	65nm	65nm	**40nm**

Acknowledgments

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