Ge n-channel FinFET with optimized gate stack and contacts

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Abstract

Whilst high performance p-channel Ge MOSFETs have been demonstrated [1-4], Ge n-channel MOSFET drive current has been lagging behind mainly hampered by high access resistance and poor gate stack passivation [5-9]. In this work, we address these issues on a module level and demonstrate Ge enhancement mode nMOS FinFETs fabricated on 300mm Si wafers implementing optimized gate stack ($D_{it} < 2x10^{11}$ $eV^{-1}\cdot cm^{-2}$), n^+-doping ($N_d > 1x10^{20}$ cm^{-3}) and metallization ($\rho_c = 1x10^{-7}$ Ωcm^2) modules. $L_G \sim 40$ nm devices achieved $I_{on} = 50$ µA/µm at $I_{off} = 100$ nA/um, $S \sim 124$ mV/dec, at $V_{DD} = 0.5V$. The same gate stack and contacts were deployed on planar devices for reference. Both FinFET and planar devices in this work achieved the highest reported g_m/S_{sat} at 0.5 V to date for Ge nMOS enhancement mode transistors to the best of our knowledge at shortest gate lengths.

Ge modules for NMOS

n-Ge doping - Using an n^+/p junction with P implantation, activation and diffusion was studied for different annealing techniques. Secondary Ion Mass Spectrometry (SIMS) data after activation are shown in Fig. 1. Activation of P in Ge can be achieved at low temperature [10] but we find active doping concentration N_{act} to not exceed $1x10^{19}$ cm^{-3} irrespective of annealing time. As suggested in [11], this may be related to implantation damage-induced acceptor formation resulting in lower P activation. At medium temperature, P-vacancy clusters become mobile leading to a typical box-like profile and N_{act} of mid-10^{19} cm^{-3} (Fig. 1). The optimized process achieves abrupt and high N_{act} junctions yielding the best R_s-x_j envelope reported to date for Ge n^+/p junctions (Fig. 2) [12-17].

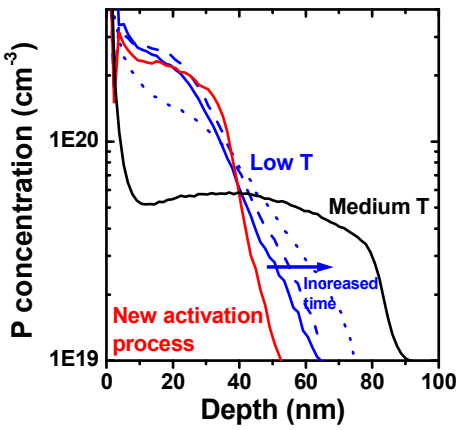


Figure 1: SIMS of phosphorus in Ge annealed using different annealing techniques. At low T we estimate $1x10^{19}$ cm^{-3} from R_s. The box-like profile at medium T is indicative of PV pair diffusion achieving N_{act} of mid-10^{19} cm^{-3}. Our new activation process provides high N_{act} and junction abruptness of ~ 4.5nm/dec.

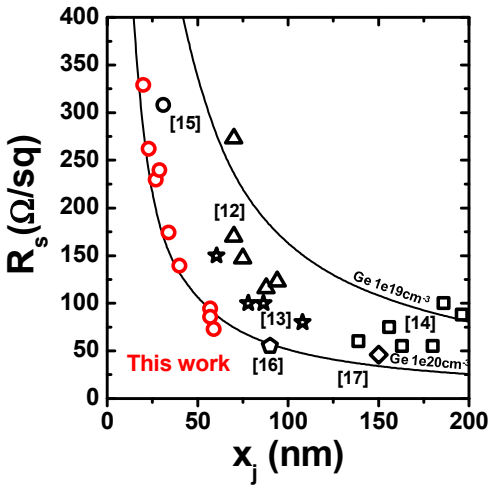
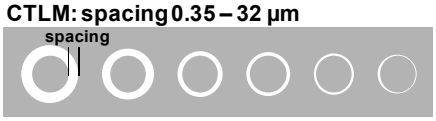


Figure 2: µ4PP R_s *vs.* x_j for optimized, scaled n-Ge junctions benchmarked with literature data [12-17]. Our data represent best R_s-x_j values to date following the $N_{act} = 1x10^{20}$ cm^{-3} trend line down to 23 nm junction depth.

n-Ge metallization - As Me/Ge contacts show strong pinning close to the Ge valence band [18], high N_{act} at the metal/Ge interface is crucial to promote tunneling through the Schottky barrier and to achieve ohmic contacts. We investigated NiGe/n-Ge contacts by circular transmission line method (CTLM) structures. After implantation, anneal and patterning (248nm lithography), Ni was deposited and NiGe was formed. The unreacted Ni was removed by a selective wet etch. We developed a new CTLM contact resistivity (ρ_c) extraction model based on Reeves model [19] that captures the parasitic metal resistance R_{ME} contribution (*i.e.* NiGe sheet resistance). Fig. 3 shows extracted parameters. We found that for P-doped Ge, increased Ni thickness leads to



Doping species	Ni	ρ_c ($\Omega\cdot cm^2$)	R_{sc} (Ω/sq)	R_{me} (Ω/sq)
P	thin	5.0e-6	148	8.5
P	thick	8.8e-5	133	3.5
As	thin	1.1e-7	95	8.5
As	thick	1.9e-7	93	3.5
B	thin	5.4e-7	38	9

Figure 3: ρ_c and sheet resistance of n+ Ge, R_{sc} determined from CTLM using new extraction model (not shown). NiGe sheet resistance, R_{me}, used as input parameter, is based on µ4PP measurements. Results for P are in line with [20]. The lowest ρ_c achieved was $1.1x10^{-7}$ Ωcm^2.

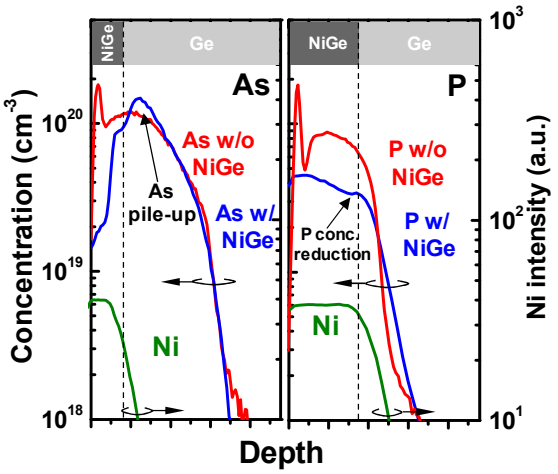


Figure 4: SIMS of As (left) and P (right) in Ge with or without NiGe formation. As piles up at the NiGe/Ge interface while the P concentration is reduced considerably.

higher ρ_c, while for As-doped Ge ρ_c remains low ($< 2x10^{-7}$ Ωcm^2). The effect is largely due to higher dopant concentration at the NiGe/Ge interface as shown in Fig. 4. The lowest ρ_c achieved was $1.1x10^{-7}$ Ωcm^2 which compares well with lowest values reported [20-23].

Ge gate stack - Interfacial treatments, high-κ optimization and treatments of the gate stacks reported in [3] were deployed in this work aiming for a device design with sub 1nm EOT scaling capability. Multi-frequency C-V for a 100x100 µm^2 MOSCAP with EOT = 1.3 nm is shown in Fig. 5. The small frequency dispersion in depletion to accumulation region is indicative of a low density of electrically active traps at and close to the dielectric/Ge interface. Low-T C-V analysis was used to extract D_{it} across the Ge band-gap (Fig. 6); the Hi-Lo method gave similar D_{it}; there is no dependence on EOT (Fig. 7). D_{it} ~ $2x10^{11}$ eV^{-1}cm^{-2} was found around mid-gap. The D_{it} levels achieved in this work are amongst the lowest reported on n-type Ge(100) and Ge(110) at scaled EOTs of 1-3 nm [24-25].

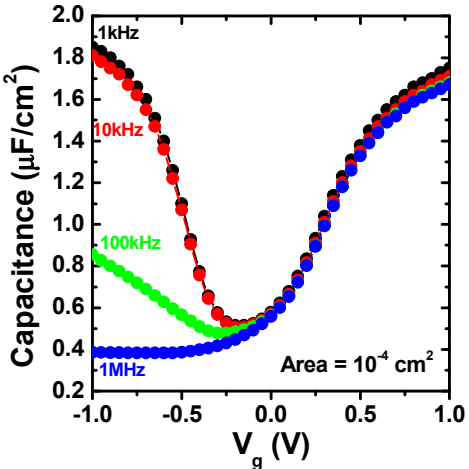


Figure 5: Multi-frequency C-V for a 100x100 µm^2 MOSCAP. The small frequency dispersion in depletion to accumulation region is indicative of a low density of electrically active traps at and close to the dielectric/Ge interface.

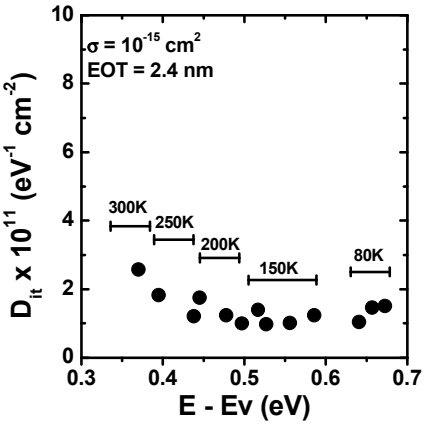


Figure 6: D_{it} *vs.* energy from conductance method at temperatures ranging from 80 to 300 K. D_{it} of $2x10^{11}$ eV^{-1}cm^{-2} was found around midgap.

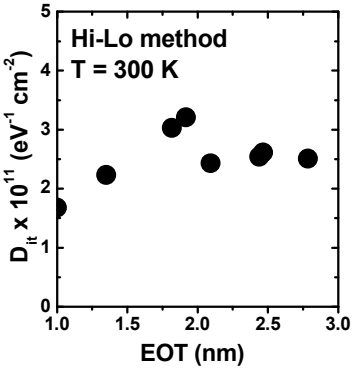


Figure 7: Midgap D_{it} dependence on EOT. D_{it} remains low at low EOT.

Ge enhancement mode NMOS Transistors

Enhancement mode n-channel Ge planar (001) FETs and (001)/⟨110⟩ FinFETs were fabricated using Ge-in-STI 300 mm Si wafers as in [1, 2] and the device process including aspect-ratio trapping as described in [1-3], respectively. Gate-to-channel capacitance (for several CETs) and C-V curves (for the same CETs) for the planar MOSFETs are shown in Fig. 8. Effect of annealing conditions for contacts on device performance becomes

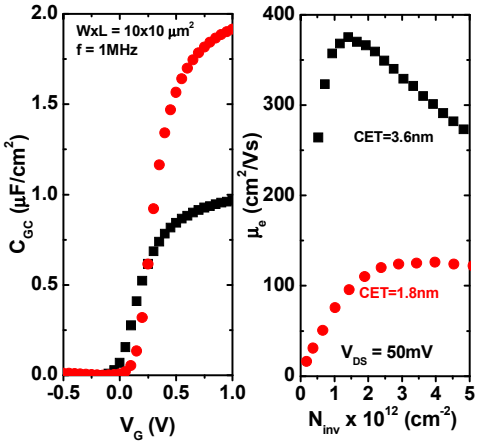


Figure 8: Gate-to-channel capacitance (for several CETs) and mobility curves (for the same CETs) for optimized gate dielectric (planar devices).

apparent from Figs. 9-11. Significant improvement in g_m (Fig. 9) and short channel effect (SCE) control (Fig. 10) is observed when optimized contacts are used. R_{ext} was extracted as 500 Ω·µm while for the reference devices R_{ext} ~60 kΩµm was estimated (Fig. 11). Further SCE immunity is achieved implementing the FinFET architecture (Fig. 10). Fig. 12 shows g_m and S as a function of L_g for the FinFETs. Sub-threshold swing of 76mV/dec at V_{ds} = 50 mV and L_G = 60 nm is achieved. Transfer and output characteristics of the best short-channel device are shown in Figs. 13-14. Our nGe planar and FinFETs are benchmarked in Fig. 15 and exhibit highest g_m/S_{sat} at shortest gate length and scaled EOT compared to published results for enhancement mode Ge nFETs on (100) or (111) surfaces [6-9].

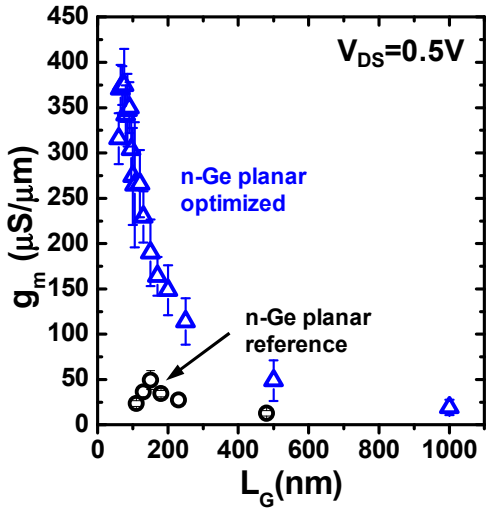


Figure 9: Peak-g_m at V_{ds} = 0.5 V as function of gate length for Ge n-channel planar FETs comparing reference and optimized devices.

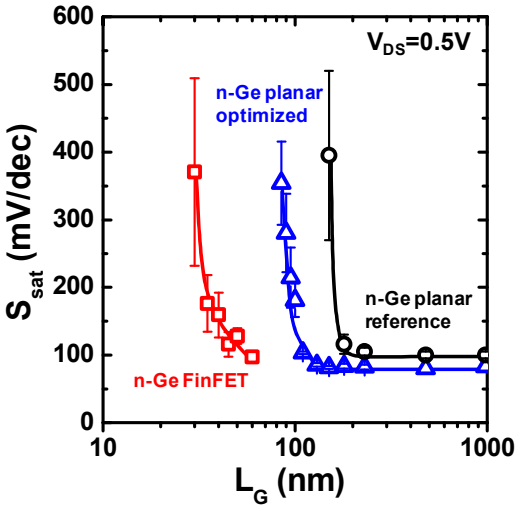


Fig. 10: Sub-threshold swing at V_{ds} = 0.5 V as a function of gate length for Ge n-channel planar FETs (reference and optimized) and FinFETs. Roll-up is improved when optimized contacts are implemented. FinFETs provide even better SCE control.

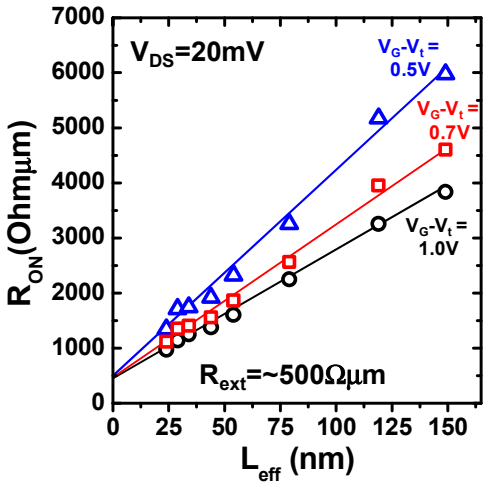


Figure 11: Average R_{on} (≡ V_{ds}/I_{ds} with $V_{gs}-V_t$ = 0.5, 0.7, 1.0V and V_{ds} = 20mV) *vs.* effective gate length L_{eff} of Ge planar devices. R_{ext} was determined as 500 Ωµm. For comparison R_{ext} of reference devices is ~60kΩµm.

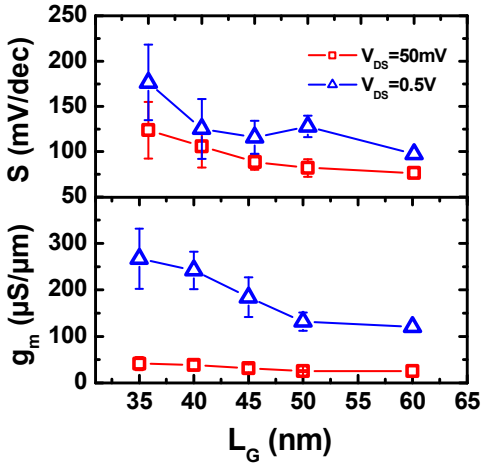


Figure 12: Sub-threshold swing and peak-g_m at V_{ds} = 50mV, 0.5 V as function of gate length for Ge n-channel FinFETs. At L_G = 60 nm, S = 78 mV/dec at V_{ds} = 50mV.

Conclusions

We report Ge n-channel FinFETs implementing optimized gate stack ($D_{it} < 2x10^{11}$ $eV^{-1}cm^{-2}$), n^+-doping ($N_{act} > 1x10^{20}$ cm^{-3}) and metallization ($\rho_c = 1x10^{-7}$ Ωcm^2) modules. Both Ge nMOS FinFETs and planar transistors fabricated on (001) substrates in this work achieved the highest performance and g_m reported to date for Ge enhancement-mode NFETs with 0.5V V_{DD} and I_{off} < 100nA/um at the shortest gate-lengths (~40 nm on Fin-FETs, ~90nm on planar transistors) and lowest S_{sat} (~120mV/dec) to the best of our knowledge with sub 1nm EOT scaling capability.

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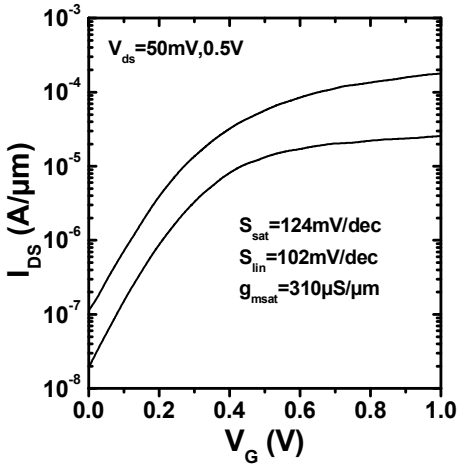

Figure 13: Linear and saturation (V_{ds} = 50 mV, 0.5 V) transfer characteristics of Ge n-channel FinFET (L_G = 40 nm). I_{on} = 50 µA/µm at I_{off} = 100 nA/µm (V_{DD} = 0.5 V)

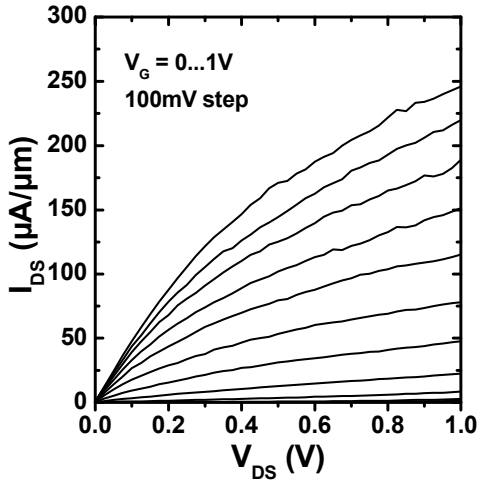

Figure 14: Output characteristics of Ge n-channel FinFET (L_G = 40 nm).

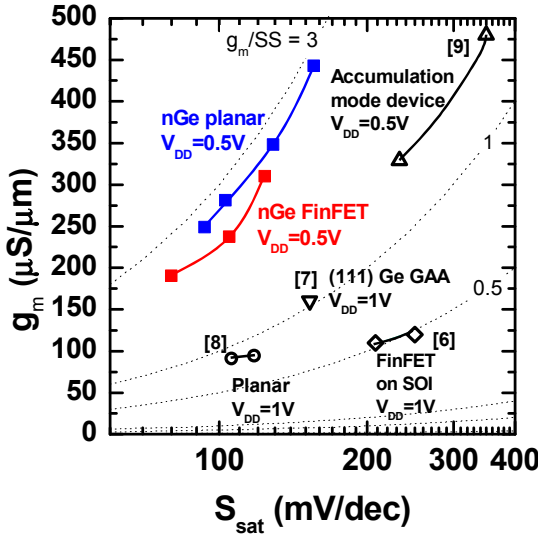

Figure 15: Extrinsic peak g_m *vs.* S_{sat} benchmark for Ge n-channel FETs [6-9], including our planar and FinFET data and accumulation mode nGe FET [9] at V_{DD}=0.5V and FinFET on SOI [6], Gate-All-Around (GAA) with (111) Ge side walls [7] and planar Ge nFET [8] all at V_{DD}=1V. Our data represent highest g_m/S for n-channel Ge FETs to date.

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