Monolithic Three-Dimensional Imaging System: Carbon Nanotube Computing Circuitry Integrated Directly Over Silicon Imager

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Abstract

Here we show a hardware prototype of a monolithic three-dimensional (3D) imaging system that integrates computing layers directly in the back-end-of-line (BEOL) of a conventional silicon imager. Such systems can transform imager output from raw pixel data to highly processed information. To realize our imager, we fabricate 3 vertical circuit layers directly on top of each other: a bottom layer of silicon pixels followed by two layers of CMOS carbon nanotube FETs (CNFETs) (comprising 2,784 CNFETs) that perform in-situ edge detection in real-time, *before* storing data in memory. This approach promises to enable image classification systems with improved processing latencies.

Keywords: imager, CNTs, CNFETs, monolithic 3D

Introduction

Real-time, low-latency object classification from images or video is critical for a myriad of next-generation applications ranging from autonomous driving to robotics to augmented reality [1-2]. However, such data-intensive applications are severely limited by the "communication bottleneck": where the performance (e.g., speed and energy-efficiency) of such systems are dominated not by capturing the image itself but instead by the rate at which data can be read from the pixel array, stored in memory, read from the memory by a processor, and then classified [3-4]. To overcome this challenge, significant work today focuses on integrating imagers, memory, and logic through chip-stacking, whereby heterogeneous chips are stacked and bonded over one-another, using through-silicon vias (TSVs) to connect vertical layers [5-6]. While TSV-based approaches can provide benefits, they face several limitations: (1) the imager material is limited to substrates that have similar thermal expansion rates as silicon to avoid failure during wafer bonding to memory or logic dies/wafers (which are made from silicon), (2) TSVs require large keep-out-zones (KOZ), limiting the fill-factor of the pixels, memory, and/or logic layers, and (3) TSV dimensions (on the order of μms) limit via density and thus bandwidth between vertical layers.

To overcome these challenges, we experimentally demonstrate a prototype *monolithic* 3D imaging system with layers of computing circuits fabricated *directly vertically over* the imager substrate without any die- or wafer-bonding. This eliminates the need for serially reading the pixel array data to/from memory before classification. By monolithically integrating layers of computing circuits (e.g., analog-to-digital converters and digital logic) directly in the back-end-of-line (BEOL) over the imaging pixels, such monolithic 3D imagers can capture and compute on all of the pixels in parallel with significantly lower latency (without requiring costly serial accesses to memory). This transforms the imager output from raw pixel values to highly-processed information: the output from the camera system itself is object detection, classification, *etc*. Moreover, compared to conventional chip-stacking, our monolithic 3D approach (1) can be fabricated over arbitrary imaging substrates (Si, Ge, III-Vs, etc.), (2) requires no KOZ and thus the imagers and logic can realize nearly 100% fill-factor, and (3) can realize >1,000× vertical interconnect density (and thus increase in data bandwidth between layers) (BEOL nano-scale vias (ILVs) used for monolithic 3D can be >1,000× denser than TSVs) [7].

Hardware Prototype

While realizing monolithic 3D is challenging with Si CMOS due to its high temperature process (>1,000 °C, which can damage bottom layer devices and interconnects), we naturally enable such systems by using CNFET CMOS [8]. We use CNFETs for upper-layers of logic because (1) their low-temperature processing (<300 °C) is within the BEOL thermal budget, and (2) CNFETs promise a ~10× benefit in energy-delay product (EDP) versus silicon CMOS [9]. Our hardware prototype is shown in Fig. 1. It consists of three monolithically integrated vertical layers: layer #1: a traditional Si imager using p-n junction photodiodes, layer #2: programmable digitization of the analog pixel output, layer #3: CNFET logic performing edge detection. As a demonstration, the prototype monolithic 3D imager is an 8×8 pixel array and comprises 2,784 CMOS CNFETs; all design and fabrication is wafer-scale (150 mm substrates) and VLSI- and silicon-CMOS compatible (process flow in Fig. 2 [10]).

Fig. 3 shows the circuit schematic of a monolithic 3D pixel cell, as well as the full imager architecture. Data from all Si pixels on layer #1 are read in parallel through conventional ILVs used in the BEOL to layer #2 (i.e., no TSVs). On layer #2, a CNFET load transistor (with an adjustable gate bias) converts the pixel current to a voltage (Fig. 3b). Again, in parallel, all pixel voltages are passed to layer #3 through ILVs, where CNFET CMOS logic then: (1) digitizes the voltage through a CNFET inverter, and (2) performs edge detection across the entire image (horizontal and vertical XOR operations are summed using OR gates to perform the edge detection). Thus, the imager output is edge detection rather than the raw pixel data (image output in Fig. 6). Although we implement edge detection on our monolithic 3D prototype, our approach demonstrates the feasibility of large-scale monolithic 3D imaging systems, e.g., with high-resolution imagers integrated directly underneath a computing system implementing a convolutional neural net for low-latency image classification.

Experimental Results

Fig. 4 and Fig. 5 provide measured characteristics of the sub-systems and circuits comprising the imager. Fig. 4 shows the digitized output response of a single monolithic 3D pixel cell comprising the Si pixel (layer 1), CNFET voltage converter (layer 2), and CNFET inverter for digitization (layer 3); by adjusting the biasing voltage, we can select the threshold for the digitization). Voltage transfer curves (VTCs: output voltage vs. input voltage) for all of the CNFET CMOS logic gates are shown in Fig. 5. Fig. 6 shows the output of the full imager. We physically mask off different regions of the imager and illuminate the system with light. An image of the mask and the subsequent readout from the imager shows functional edge detection for a variety of shapes.

Conclusion

We demonstrate a monolithic 3D imager comprising 3 vertically-integrated circuit layers: 2 layers of CNFETs over a conventional silicon imager substrate. While our hardware prototype performs edge detection, such systems pave the way for additional computing layers to perform critical tasks such as object detection or classification; transforming sensor outputs from raw data to actionable information.

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References. [1] Y. LeCun, Nature, 521, 436-444, 2015 [2] S. Ren, *NeurIPS*, 2015, 91-99. [3] M. Horowitz, *ISSCC*, 2014, 10-14. [4] B.M. Rogers, *ACM SIGARCH*, 37, 371-382, 2009. [5] X. Gagnard, *Microelectron. Eng.*, 87, 470-476, 2010. [6] H. Tsugawa, *IEDM*, 2017, 56-59. [7] M.M.S. Aly, *Computer*, 48, 24-33, 2015. [8] M. Vinet, *Microelectron. Eng.*,88, 331-335, 2011. [9] G. Hills, *IEEE TNANO*, 17, 1259-1269, 2018. [10] C. Lau, *ACS Nano,* 12, 10924-10931, 2018. [11] T. Srimani, *IEEE TNANO*, 18, 132-138, 2019. [12] nanointegris.com

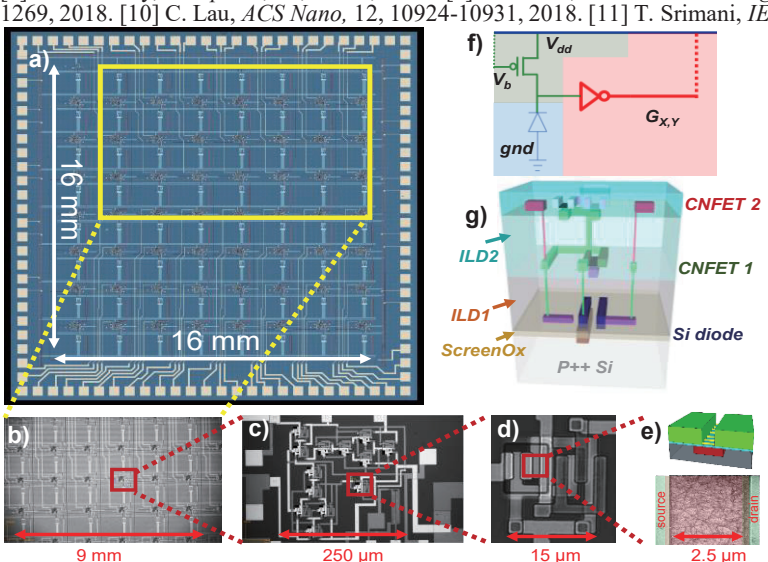


Fig 1: (a) 3D imager micrograph (b) magnified optical microscopy image of sub-circuit, (c) edge-detector logic block with load CNFET, (d) CMOS CNFET inverter and (e) a typical CNFET, (3D model with SEM of channel, false colored to match the model). (f) Schematic and (g) 3D model of a Si photodiode (layer 1, highlighted in blue) monolithically integrated with a load CNFET (layer 2, highlighted in green) for transducing the pixel current output to an adjustable voltage signal and a CMOS CNFET inverter (layer 3, highlighted in red) for digitizing the voltage output from layer 2.

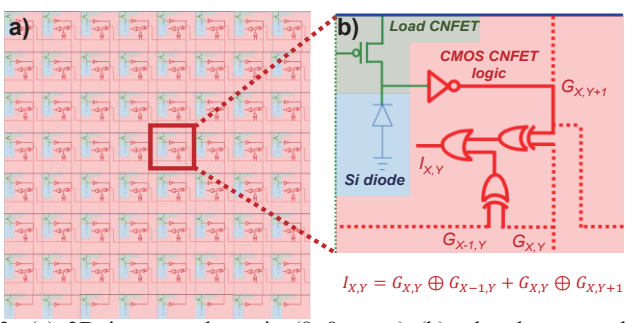
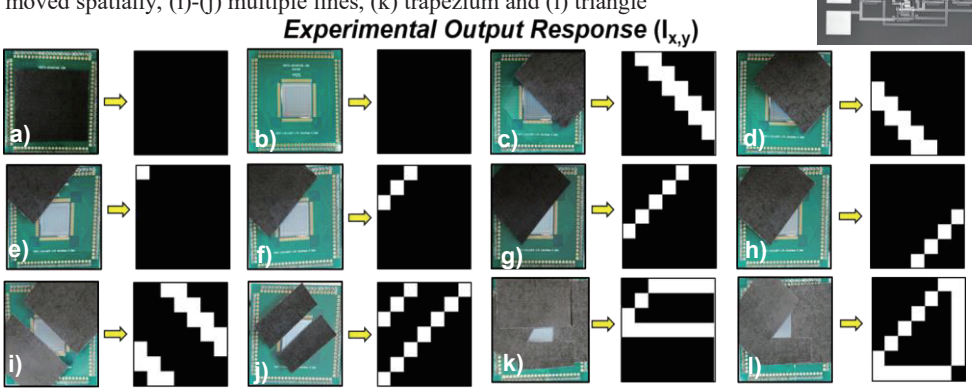


Fig. 3: (a) 3D imager schematic (8×8 array) (b) edge-detector sub circuit highlighting different layers of active devices showing bitwise horizontal and vertical XOR operation summed using OR gates for edge detection. Schematic is color-coded to highlight the different physical layers of devices to match Fig 1. Layer 1 (blue) comprises of an 8x8 array of p-n Si photodiodes, connected to layer 2 (green) consisting of PMOS CNFETs transducing the pixel current signal to an adjustable voltage output finally connected to layer 3 (red) with (a) inverters digitizing the output from layer 2 and (b) XOR and OR gates performing edge detection on inverter outputs. All logic gates in the circuit are made with CMOS CNFETs.

Fig 6: Experimental output response of the edge-detector circuit for (a)-(b) dark and illuminated backgrounds, (c)-(h) single lines in different directions moved spatially, (i)-(j) multiple lines, (k) trapezium and (l) triangle



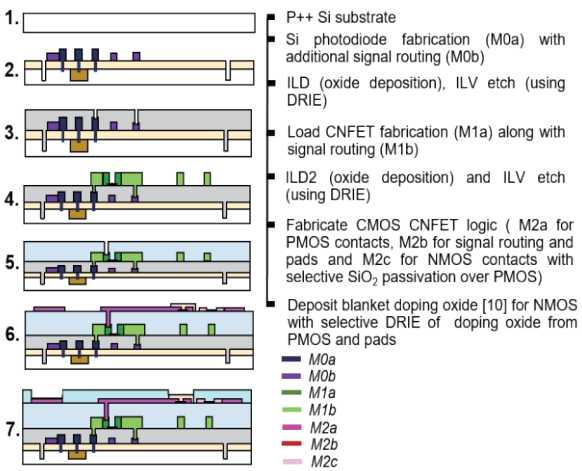


Fig 2: 3D imager process flow with description (right). All patterning is done using MLA-150 direct write photolithography and all metal deposition done using electron beam evaporation and lift-off. p-n Si photodiodes are fabricated by implanting Sb over a P++ Si wafer. Back-gate CNFETs[11] were fabricated by a gate-before-channel CMOS CNFET process [10] using solution based CNT deposition (99.9% pure semiconducting CNTs [12]).

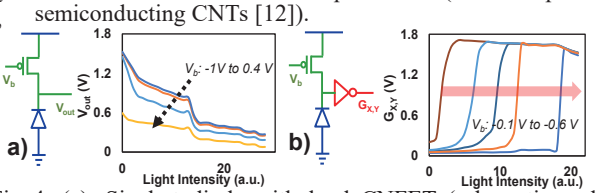


Fig 4. (a). Si photodiode with load CNFET (schematic and electrical response) (b). Si photodiode with the digitizer (schematic and electrical response). Individual circuit components color coded to match Fig 1.

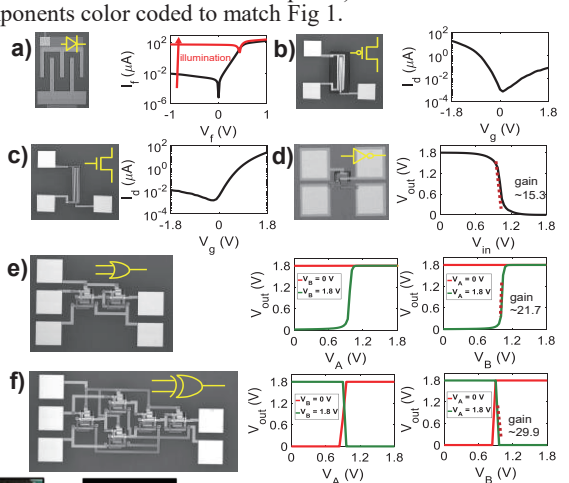


Fig 5: Individual circuit components – optical microscopy images (with corresponding circuit symbol) and typical electrical response (a) p-n Si photodiode (b) PMOS CNFET (c) NMOS CNFET (d) CMOS CNFET inverter (>97.7% signal swing) (e) CMOS CNFET OR gate (>98% signal swing) and (f) CMOS CNFET XOR gate (>99.86% signal swing). For (b) and (c) I_D-V_{GS} characteristics is measured at V_{DS} = -1.8 V