An Optimized Transformerless Photovoltaic Grid-Connected Inverter

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Abstract—Unipolar sinusoidal pulsewidth modulation (SPWM) full-bridge inverter brings high-frequency common-mode voltage, which restricts its application in transformerless photovoltaic grid-connected inverters. In order to solve this problem, an optimized full-bridge structure with two additional switches and a capacitor divider is proposed in this paper, which guarantees that a freewheeling path is clamped to half input voltage in the freewheeling period. Sequentially, the high-frequency common-mode voltage has been avoided in the unipolar SPWM full-bridge inverter, and the output current flows through only three switches in the power processing period. In addition, a clamping branch makes the voltage stress of the added switches be equal to half input voltage. The operation and clamping modes are analyzed, and the total losses of power device of several existing topologies and proposed topology are fairly calculated. Finally, the common-mode performance of these topologies is compared by a universal prototype inverter rated at 1 kW.

Index Terms—Clamping, common-mode voltage, full-bridge inverter, unipolar sinusoidal pulsewidth modulation (SPWM).

I. INTRODUCTION

TRANSFORMERLESS grid-connected inverters have a lot of advantages such as high efficiency, small size, light weight, low cost, etc. [1]–[6]. However, there is a galvanic connection between power grid and solar cell array. Depending on the inverter topology, this may cause fluctuation of the potential between the solar cell array and the ground, and these fluctuations may have a square wave at switching frequency. When energized by a fluctuating potential, the stray capacitance to ground formed by the surface of the photovoltaic (PV) array may lead to the occurrence of ground currents. A person, connected to the ground and touching the PV array, may conduct the capacitive current to the ground, causing an electrical hazard [4]. At the same time that the conducted interference and radiated interference will be brought in by the ground current, the grid current harmonics and losses will also increase [5].

The unipolar sinusoidal pulsewidth modulation (SPWM) full-bridge inverter has received extensive attentions, owing to its excellent differential mode characteristics such as higher dc voltage utilization, smaller current ripple in the filter inductor, and higher processing efficiency. However, the switching frequency time-varying common-mode voltage (whose amplitude is equal to a dc input voltage) is brought in. Therefore, a transformer (low frequency or high frequency) is needed to isolate the solar cell array from the grid in grid-connected applications, and at the same time, the high-frequency common-mode voltage endangers the insulation layer of the transformers [7], which increases its manufacturing cost. In order to remove this transformer from the unipolar SPWM full-bridge grid-connected inverter, a lot of in-depth researches, where new freewheeling paths are constructed to separate the PV array from the grid in the freewheeling period, have been done [6], [8]–[11]. A pair of switches between the two midpoints of the bridge leg [ac side, shown in Fig. 1(a)] has been added in [8] to construct a new freewheeling path in the freewheeling period. In [9], Gonzalez *et al.* bring a double clamping branch to the solar cell array side [shown in Fig. 1(b)], and the potential can be clamped in the freewheeling period by a capacitor divider in the input side. Only one additional high-frequency switch is brought to the positive terminal of the PV array [shown in Fig. 1(c)] to achieve the disconnection with the grid in the freewheeling period in [10]. Based on the high-frequency common-mode equivalent model of the full-bridge circuit derived by Gonzalez *et al.* [11] and Gubia *et al.* [12], it is necessary that the potential of the freewheeling path is clamped to half input voltage in the freewheeling period instead of disconnecting the PV array from the grid simply, and by which, the high-frequency common-mode voltage can be completely avoided in the unipolar SPWM full-bridge inverter. In [8] and [10], the potential of the freewheeling path cannot be clamped in the freewheeling period, and its level depends on the parasitic parameters of the path and the grid voltage amplitude. The clamping branch proposed by Gonzalez *et al.* [9] guarantees that the freewheeling path is clamped to half input voltage in the freewheeling period, but the output current flows through four switches in the power processing period, which increases the conduction losses.

Thin-film panels have a lot of advantages such as low cost and are suitable for building-integrated PV [13], [14]. However, its power density is lower than the conventional crystalline silicon module (which means that its conversion efficiency is lower). Thus, the stray capacitor of unit power module to the ground increases from 50–150 nF/kW for crystalline silicon module up to 1 μF/kW for thin-film module [4]. Unfortunately, the transformerless grid-connected inverters make the ground current suppression become much more challenging in applications of thin-film panels.

Considering both of the advantages and disadvantages of the existing topologies mentioned earlier, an optimized
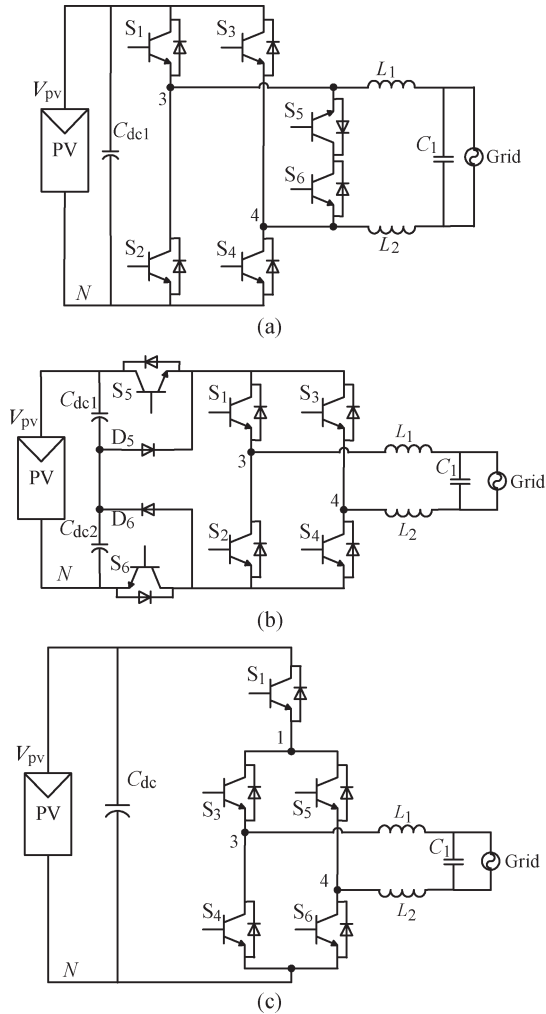
Fig. 1. Several transformerless grid-connected inverters. (a) Heric topology proposed in [8]. (b) Topology proposed in [9] has been named as H6 in this paper. (c) H5 topology proposed in [10].
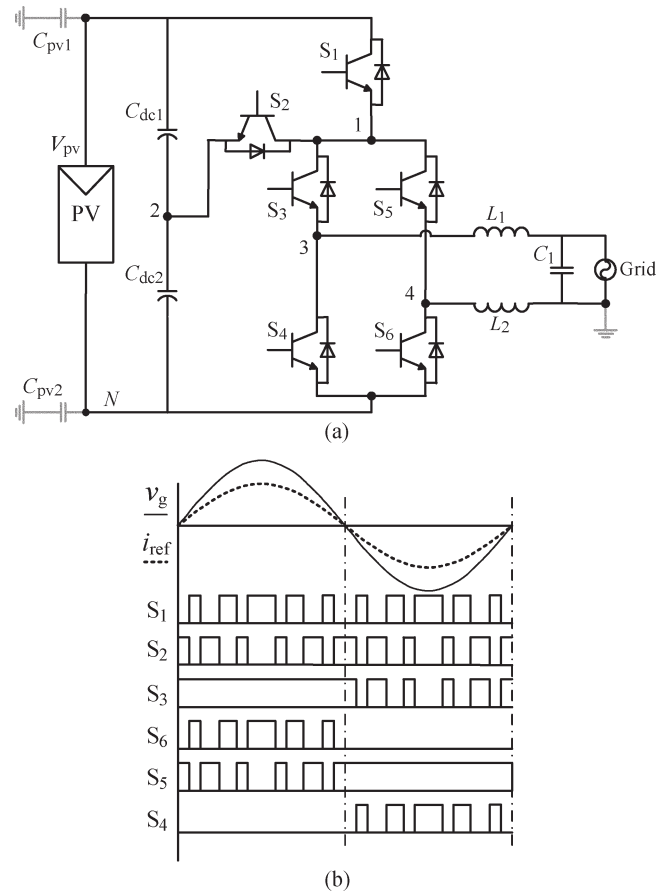

Fig. 2. Optimized transformerless PV grid-connected inverter. (a) Proposed circuit structure with PV parasitic capacitors. (b) Gate drive signal with unity power factor.

full-bridge structure has been proposed in this paper. Based on the structure in [10], a controllable switch and a capacitor divider are added to form a bidirectional clamping branch which guarantees that the freewheeling path is clamped to half input voltage in the freewheeling period and the output current flows through only three switches in the power processing period, so that the conduction losses can be decreased effectively. In addition, the blocking voltage of added switches is only half of the input voltage, owing to the clamping structure, which is beneficial to further improve the efficiency. The total losses of power device for several existing topologies and the proposed topology have been calculated and compared in this paper. Finally, the accuracy of the theoretical analysis and the validity of the clamping branch of the proposed topology are verified by a universal prototype inverter rated at 1 kW, and the common-mode performance of the optimized topology is also compared with those of several existing topologies. Because of its better ground current suppression performance and higher efficiency, this topology is suitable for high-power transformerless grid-connected inverters, particularly in thin-film solar cell applications.

II. OPERATION PRINCIPLE OF THE NEW CONVERTER

A. Structure of New Converter

In order to guarantee that the freewheeling path is clamped to half input voltage in the freewheeling period, two switches S_1 and S_2 and two capacitors C_{dc1} and C_{dc2} are introduced into the full-bridge inverter in this paper, as shown in Fig. 2(a). S_1 and S_2 are the high-frequency switches at the positive terminal of the solar cell array. $S_3 - S_6$ are switches of the full-bridge inverter. L_1, L_2, and C_1 make up the filter connected to the grid. The freewheeling path through S_3 and S_5 (including their antiparallel diodes or body diodes), with S_1, S_4, and S_6 off, guarantees that the potentials of points 1, 3, and 4 shown in Fig. 2(a) are equal (the potential of the freewheeling path is defined as this potential) and are clamped to the potential of point 2 by switch S_2.

B. Operation Principle Analysis

Grid-connected PV systems usually operate with unity power factor. The waveform of the gate drive signal for the proposed converter is shown in Fig. 2(b). In order to guarantee that the freewheeling path is completely clamped, S_1 and S_2 are switching complementarily, and then, S_2, S_3, and S_5 must be on while S_1, S_4, and S_6 are off in current zero-crossing. The main
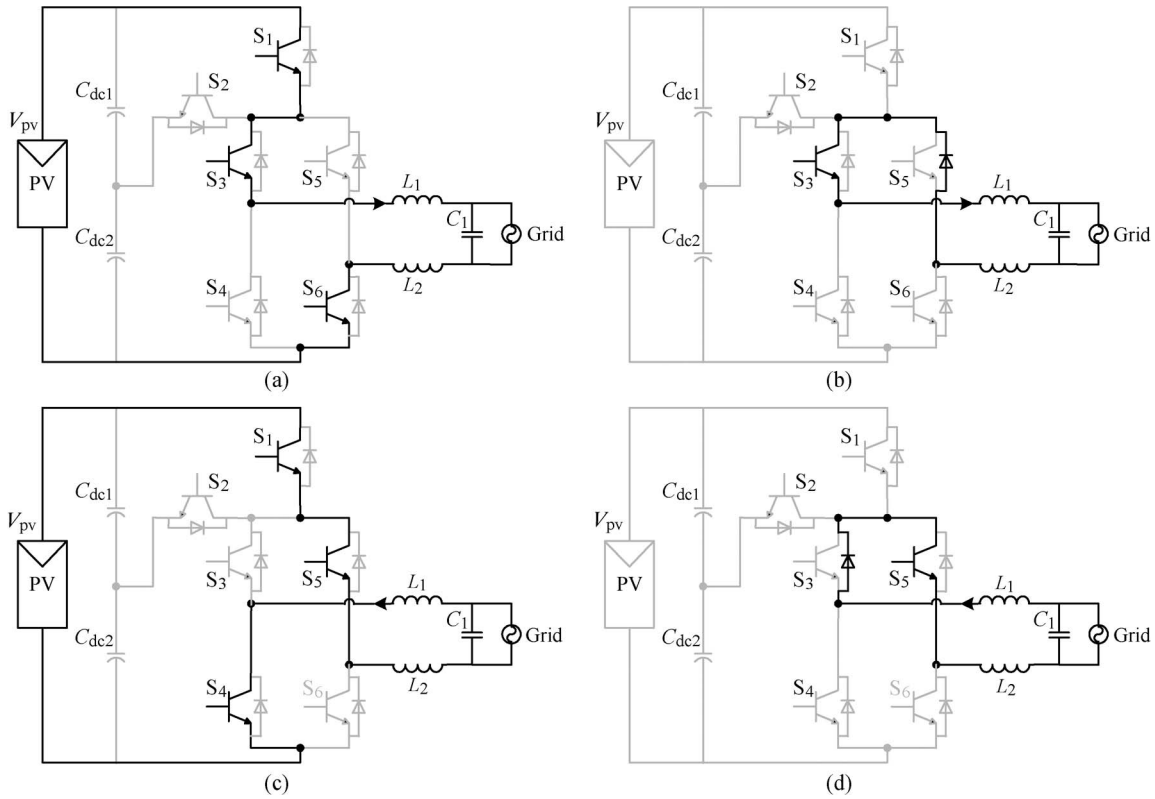
Fig. 3. Equivalent circuits of working mode. (a) Power processing mode and (b) freewheeling mode in the positive half period of the grid current. (c) Power processing mode and (d) freewheeling mode in the negative half period of the grid current.
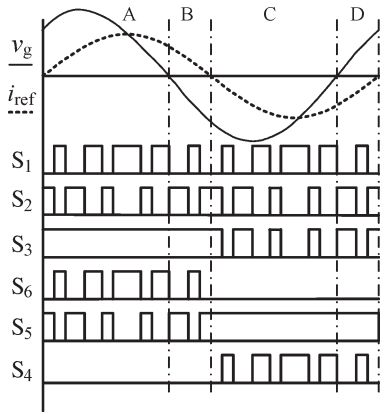

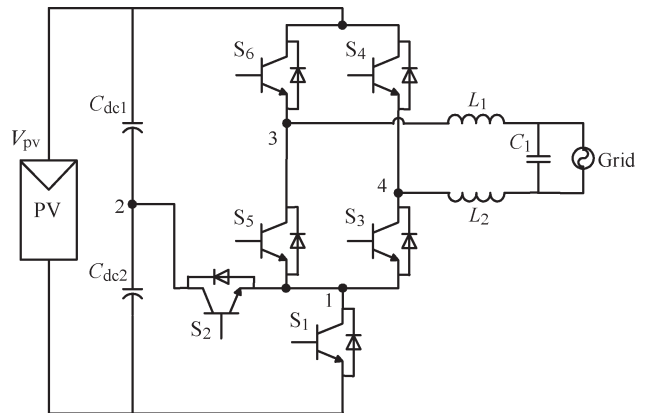Fig. 4. Gate drive signal of the proposed inverter with power factors other than unity.

Fig. 5. Alternative circuit structure.

operation modes of the converter are shown in Fig. 3, where power processing and freewheeling modes in the positive half period and negative half period of the grid current are given, respectively.

In addition, the optimized topology with unipolar SPWM described earlier can operate with power factors other than unity as shown in Fig. 4, and its operation analysis would be similar except that the grid voltage is reversed in phases B and D. Here, it is needed to point out that the drive signal is in phase with the grid current.

Similarly, an alternative topology has been proposed, shown in Fig. 5, which has uniform operation principle as Fig. 2(a).

III. CLAMPING BRANCH

A. Capacitor Divider

For single-phase PV grid-connected systems in a power range of up to 10 kW, the voltage level of solar cell array is relatively high, generally reaching 350–750 V dc, so that two electrolytic capacitors rated at 400 V are used in series in order to reduce the cost. In addition, the working voltage of the capacitors C_{dc1} and C_{dc2} must be reliably divided to guarantee that the capacitors work safely and the freewheeling path is clamped to half input voltage in the freewheeling period. The midpoint voltage may deviate due to the dispersion of the component and parasitic parameters [15]–[17].
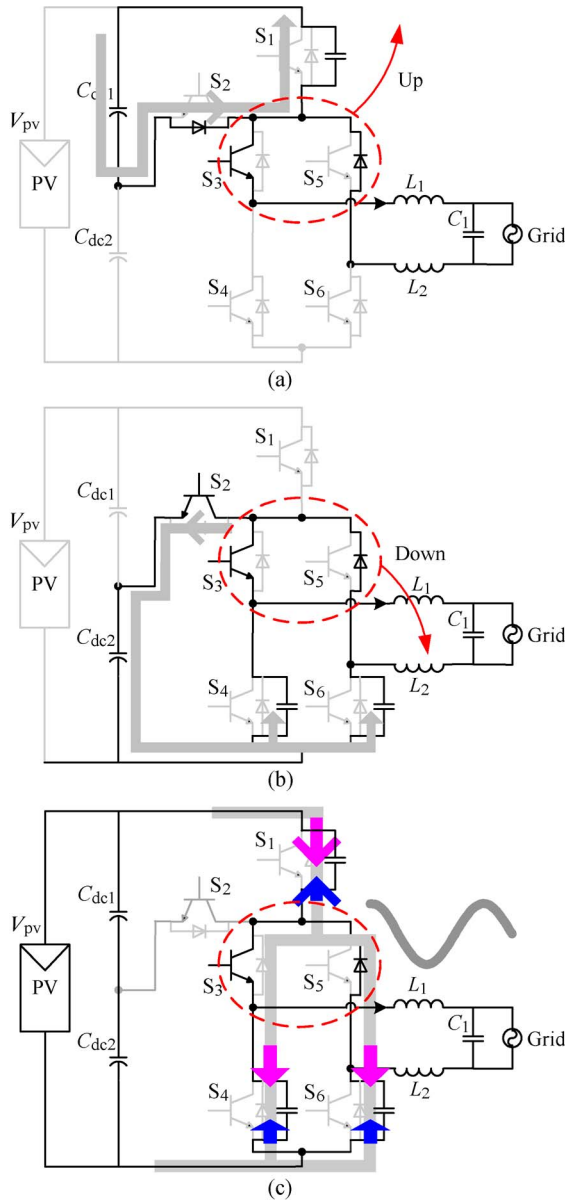
Fig. 6. Equivalent circuits in the clamped mode. (a) Potential down. (b) Potential up. (c) Potential fluctuates with grid voltage in the positive half period of the grid current.

This deviation can be suppressed by some means such as adding a resistor divider or an active voltage balancing circuit. In this paper, a simple resistor divider is used to balance the capacitor voltage.

B. Operation Principle of Clamping Branch

The equivalent circuit of the converter in the clamping period is shown in Fig. 6. It can be seen that, regardless of the grid current direction, if the freewheeling path potential falls, the current flows through the antiparallel diode (or body diode) of the clamp switch S_2 to step up this freewheeling path potential to $(1/2)V_{pv}$, as shown in Fig. 6(a); if the potential rises, the clamp switch S_2 will be on so that the potential falls back to $(1/2)V_{pv}$, as shown in Fig. 6(b). However, during dead time between the switches S_1 and S_2, the potential of the freewheeling
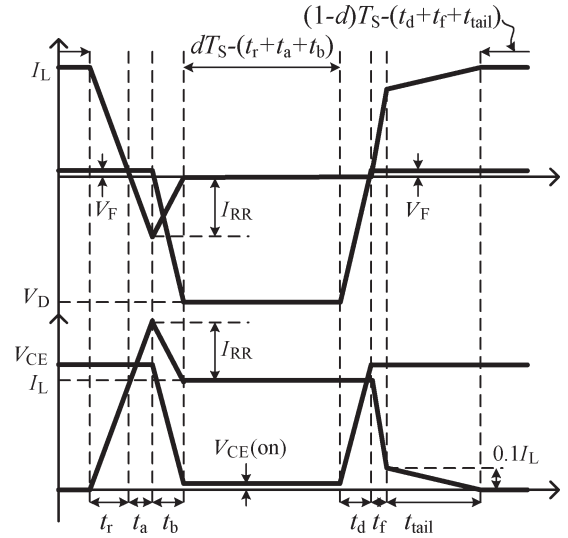

Fig. 7. IGBT's hard-switching waveforms for loss calculation.

path is not clamped effectively, as shown in Fig. 6(c), which fluctuates with grid voltage. In Fig. 6(c), the pink arrowhead represents that the potential will rise, and the blue arrowhead represents that the potential will fall.

IV. CALCULATION AND COMPARISON OF THE TOTAL DEVICE LOSSES OF SEVERAL EXISTING TOPOLOGIES

Estimation of power device losses is critical for predicting the maximum efficiency of power electronic circuits [18]–[20]. In this section, power device losses are calculated based on the unified circuit parameters (given in Table III), and the device losses of the topologies in [8]–[10] and the proposed topology named as "oH5" (shown in Figs. 1 and 2(a), respectively) are compared.

A. Losses for IGBT Turn-on and Diode Turn-off

Fig. 7 shows waveforms for the turn-on transient of an insulated-gate bipolar transistor (IGBT) and turn-off transient of a diode. In device's data sheets, the turn-on behavior is characterized by the rise time t_r, diode reverse recovery time t_a, and t_b. The turn-on loss of IGBT is calculated as [21]

$$W_{\text{IGBT,turn-on}} = \frac{V_{\text{CE}}(I_L + I_{\text{RR}})(t_r + t_a)}{2}$$
$$+ \frac{V_{\text{CE}}I_L t_b}{2} + \frac{V_{\text{CE}}I_{\text{RR}}t_b}{3} \quad (1)$$

where V_{CE} is IGBT's blocking voltage across the collector and emitter, I_L is the filter inductor current, and I_{RR} is the reverse recovery current.

The diode turn-off loss can now be computed as [21], [22]

$$W_{\text{Diode,turn-off}} = \frac{V_F(I_L + I_{\text{RR}})(t_r + t_a)}{2}$$
$$+ \frac{(V_D + V_F)I_{\text{RR}}t_b}{6} \quad (2)$$

where V_F is the ON-state voltage of the diode and V_D is the diode's blocking voltage across the cathode and anode.

B. Losses for IGBT Turn-off and Diode Turn-on

The IGBT's turn-off and the diode's turn-on behavior shown in Fig. 7 are also characterized by the IGBT's turn-off delay time t_d, fall time t_f, and tail time t_{tail}. The turn-off loss of IGBT is calculated as [18], [21]

$$W_{\text{IGBT,turn-off}} = \frac{V_{\text{CE}}I_L t_d}{2} + \frac{11 \cdot V_{\text{CE}}I_L t_f}{20} + \frac{V_{\text{CE}}I_L t_{\text{tail}}}{20}. \tag{3}$$

The diode turn-on loss can now be computed as

$$W_{\text{Diode,turn-on}} = \frac{9 \cdot V_F I_L t_f}{20} + \frac{19 \cdot V_F I_L t_{\text{tail}}}{20}. \tag{4}$$

C. On-State Losses for IGBT and Diode

The conduction losses of IGBT and diode can be calculated as

$$W_{\text{IGBT,on-state}} = V_{\text{CE}}(\text{on}) \cdot I_L \cdot [dT_S - (t_r + t_a + t_b)] \tag{5}$$

$$W_{\text{Diode,on-state}} = V_F \cdot I_L \cdot [(1 - d)T_S - (t_d + t_f + t_{\text{tail}})] \tag{6}$$

where $V_{\text{CE}}(\text{on})$ is the ON-state voltage of IGBT, d is IGBT's duty cycle, and T_S is the switching period.

D. Calculation Results

The device loss power can be derived by integral in a grid period

$$P_{\text{IGBT,loss}} = \frac{1}{T_g} \sum_{i=1}^{N} (W_{\text{IGBT,turn-on}}(i) + W_{\text{IGBT,turn-off}}(i)$$
$$+ W_{\text{IGBT,on-state}}(i)) \tag{7}$$

$$P_{\text{Diode,loss}} = \frac{1}{T_g} \sum_{i=1}^{N} (W_{\text{Diode,turn-on}}(i) + W_{\text{Diode,turn--off}}(i)$$
$$+ W_{\text{Diode,on-state}}(i)) \tag{8}$$

where T_g is the grid period, i represents one switching process, and N is the total switching time in a grid period.

Table I shows the voltage rate and distribution of the device's number in these topologies. International Rectifier's IRG4PSC71UD (600 V/60 A) IGBT with ultrafast soft recovery diode was chosen for the switches rated at 600 V. The 1200-V IGBT used was IRG4PSH71UD (1200 V/50 A), which is of the same family as the IRG4PSC71UD. The total device losses in different switching frequencies are listed in Table II under selected devices and shown as histogram in Fig. 8 with each component's percent. It can be seen that Heric [8] is with the least device loss and H5 [10] is the highest. Compared with H5, the oH5 proposed in this paper reduces the device loss significantly. In particular, the advantage of the efficiency of the optimized topology oH5 becomes more and more obvious as the switching frequency increases, and it is gradually close

TABLE I
ANALYSIS OF DEVICE OPERATION IN SEVERAL TOPOLOGIES

	Voltage rate	Heric	H6	H5	oH5
Device	600V	0	2	0	2
	1200V	6	4	5	4
Turn on/off loss	600V	0	2	0	1
	1200V	2	0	2	1
Conduction loss	600V	0	2	0	1
	1200V	2	2	3	2
Freewheeling loss	1200V trench	1	2	1	1
	1200V Diode	1	2	1	1
Reverse recovery loss	600V	0	0	0	0
	1200V	1	2	1	1
Gate loss	600V	0	2	0	2
	1200V	2	2	2	2

TABLE II
TOTAL SEMICONDUCTOR LOSSES OF SEVERAL TOPOLOGIES RATED AT
5 kW UNDER DIFFERENT SWITCHING FREQUENCIES

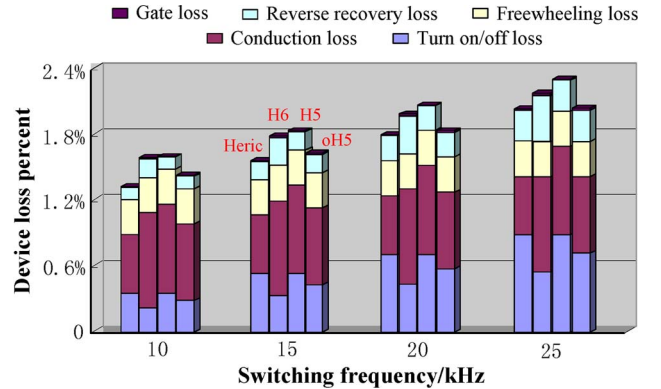| Switching frequency (kHz)	Heric (W)	H6 (W)	H5 (W)	oH5 (W)
10	66.603	79.307	79.640	71.470
15	78.102	88.103	91.436	81.880
20	89.894	98.895	103.228	91.886
25	101.686	108.353	115.020	102.094

Fig. 8. Total device loss distribution for a 5-kW rate.

to the Heric topology. The calculation results are in agreement with the theoretical estimation.

The comparison of total device losses is helpful for the selection of the high-efficiency topology in practice.

V. EXPERIMENTAL RESULTS

In order to verify the operation principle and performance comparison, a universal prototype inverter has been built in our laboratory, as shown in Fig. 9. The specifications of the converter are listed in Table III.

In Fig. 9, modules "Leg1U," "Leg1D," "Leg2U," and "Leg2D" are leg switches of the conventional full-bridge inverter. Modules "DC Bypass1," "DC Bypass2," and "Clamping Branch" are partially selected in H5, H6, and oH5 inverters according to the topology structure. Module "AC Bypass" is enabled in the Heric inverter. L_1, L_2, and C_1 make up the
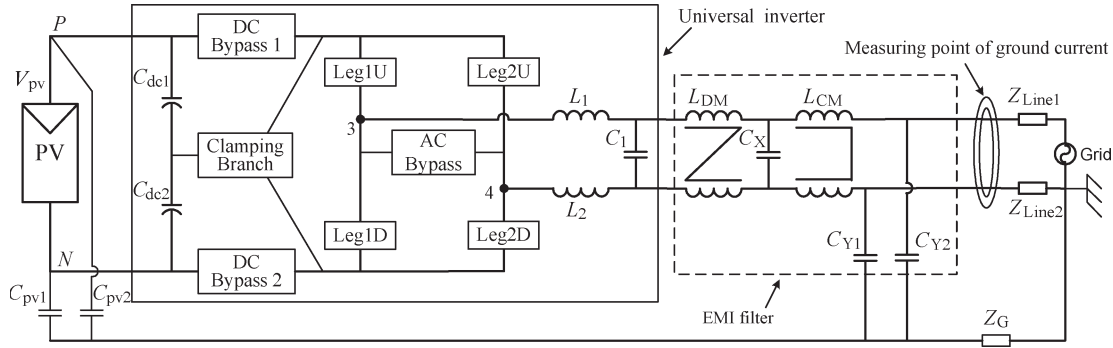
Fig. 9.   Test layout.

TABLE III
PARAMETERS OF UNIVERSAL GRID-CONNECTED
INVERTER RATED AT 1 kW

Parameter	Value
Input Voltage	340~700VDC
Grid voltage/frequency	240VAC/50Hz
Rated power	1000 W
Switching frequency	20kHz
DC-bus capacitor C_{dc1}, C_{dc2}	470μF/400V
MOSFET S_1~S_6	IXFN36N100
Filter inductor L_1, L_2	4mH
Filter capacitor C_1	6.6μF
Common-mode inductor L_{CM}	Core: 2×2W-43615-TC
	Wire: 2mm
	Turns: 10+10
Common-mode capacitor C_{Y1}, C_{Y2}	2.2 nF
PV parasitic capacitor C_{pv1}, C_{pv2}	0.1μF

grid-connected filter. C_X is a differential-mode capacitor in the electromagnetic interference (EMI) filter; L_{DM} and L_{CM} are differential- and common-mode inductors, respectively; and C_{Y1} and C_{Y2} are common-mode capacitors. The stray capacitors C_{pv1} and C_{pv2} between solar panels and the earth depend on the material and size of the solar panels, soil properties, air humidity, installation, etc. Z_{Line1} and Z_{Line2} are line impedances (mainly inductive). Z_G is the impedance between the grid ground and the chassis ground of the inverter.

In all tests, the PV parasitic capacitor, grid-connected filter, EMI filter, and measuring point of ground current are the same for performance comparison.

The common-mode voltage and the ground current waveforms of the four topologies in unified experimental conditions are shown in Figs. 10–13, respectively. The grid voltage v_g, grid current i_g, voltage v_{4N} of midpoint 4 to terminal N, common-mode voltage $v_{CM} = v_{3N} + v_{4N}/2$, and voltage v_{3N} of middle point 3 to terminal N are shown in subfigure (a) from top to down, respectively; subfigure (b) shows the grid voltage v_g, grid current i_g, ground current i_{Ground} at point of common coupling, and spectrum. Under the premise of filter inductor symmetric placement in phase line and neutral line, the ground current of the unipolar SPWM full-bridge inverter depends on the frequency and amplitude of the common-mode voltage v_{CM} [11], [12]. The values of ground current for Heric, H6, H5, and oH5 are 5.6, 0.7, 2.8, and 1.0 mA, respectively. It is

obvious that the ground current of H6 is the lowest and that the ground current of oH5 takes the second place. Both of the detailed common-mode voltage waveforms at the peak and vale of the grid current are shown in Fig. 14. It can be seen that the narrow pulsewidth in the black ring of the common-mode voltage waveform corresponds to the dead time between the switches S_1 and S_2. In this span, the freewheeling path potential rises because the clamp switch S_2 is still off. When S_2 is on, the freewheeling path potential will be quickly clamped to the midpoint potential of the capacitor divider. Due to this dead time, the common-mode characteristic of oH5 is worse than that of H6 as the clamp circuit of H6 is composed of diode's natural conduction whose performance only depends on turn-on speed of the diode. The experimental results are in agreement with the theoretical analysis well.

Considering the calculation results of total power device losses and the experimental results of the ground current suppression, it can be seen that the Heric topology has the minimum device loss but the worst common-mode characteristic, the H6 topology has the best common-mode characteristic but a higher device loss, and the proposed oH5 topology has a fine tradeoff between the device loss and the common-mode performance and is better than H5 in both of the efficiency and the ground current suppression, which can be seen from Fig. 10 and from the comparison of Figs. 12 and 13, respectively.

Fig. 15 shows the experimental waveforms. There are grid voltage v_g, grid current i_g, and inverter output voltage v_{34} (it is also the differential-mode voltage) from top to bottom. In this figure, the output voltage v_{34} has three levels as V_{pv}, 0, and $-V_{pv}$, so a good differential-mode characteristic has been achieved like the unipolar SPWM full-bridge grid-connected inverter with galvanic isolation. The gate drive signals and voltages across the drain and source of the switches S_1 and S_2 are shown in Fig. 16. It can be seen that the blocking voltages are both clamped to half of the input voltage. In addition, the current i_{D2} through S_2 is so small that it only has a little impact on the capacitor divider. In addition, the ringing on the voltage of S_2 is observed, which is due to the long conductor between drain of S_2 and point 1 for current waveform i_{D2} measurement. The long conductor winded on the current transducer with parasitic inductor induced the ringing on the voltage of S_2. Fig. 17 shows the midpoint voltage V_{2N} of the capacitor divider and the input voltage V_{pv}, from which it can be seen that the voltage is divided well.
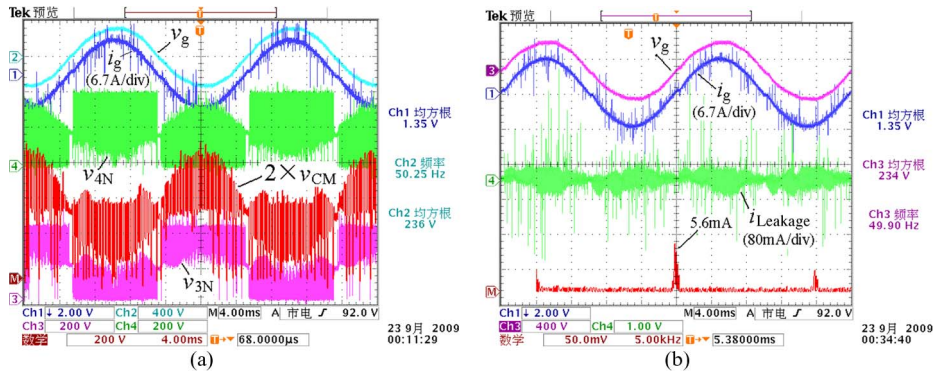
Fig. 10. Common-mode voltage and ground current waveforms in Heric topology. (a) Common-mode voltage (v_g: 400 V/div, i_g: 6.7 A/div, v_{3N} and v_{4N}: 200 V/div, v_{CM}: 200 V/div, and time: 4 ms/div). (b) Ground current (v_g: 400 V/div, i_g: 6.7 A/div, i_{Ground}: 80 mA/div, time: 4 ms/div, and M: 4 mA/div, 5 kHz/div).
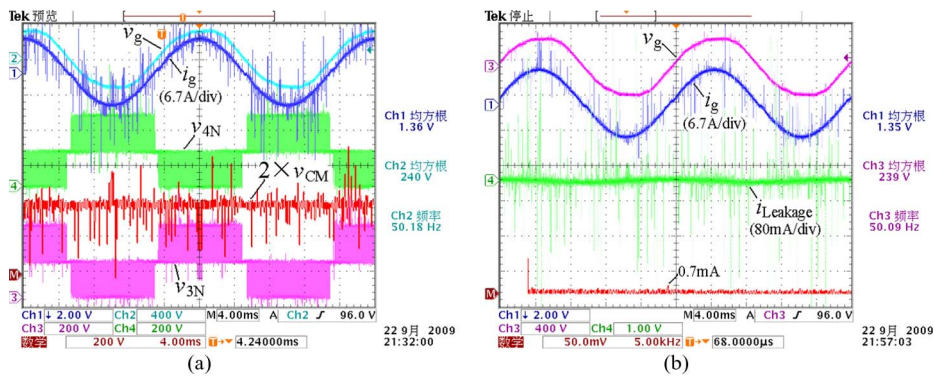

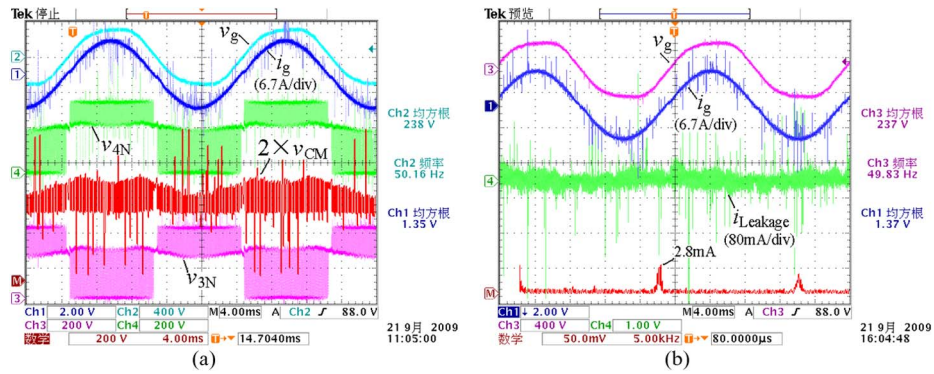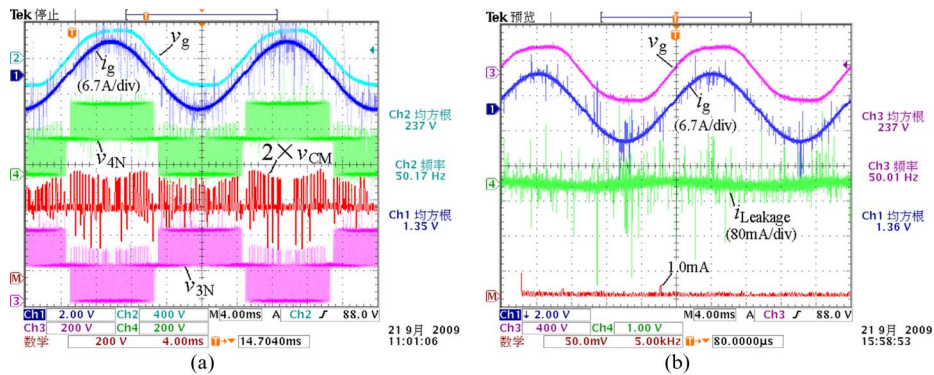Fig. 11. Common-mode voltage and ground current waveforms in H6 topology. (a) Common-mode voltage. (b) Ground current.

Fig. 12. Common-mode voltage and ground current waveforms in H5 topology. (a) Common-mode voltage. (b) Ground current.
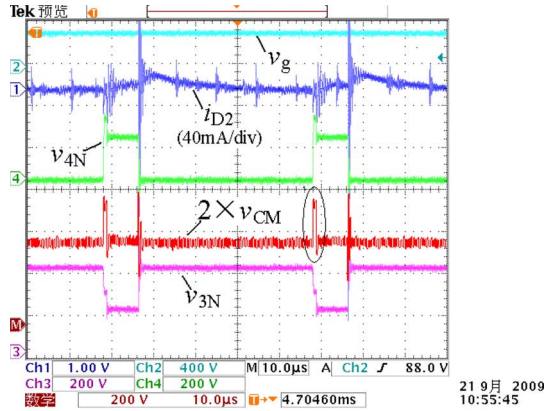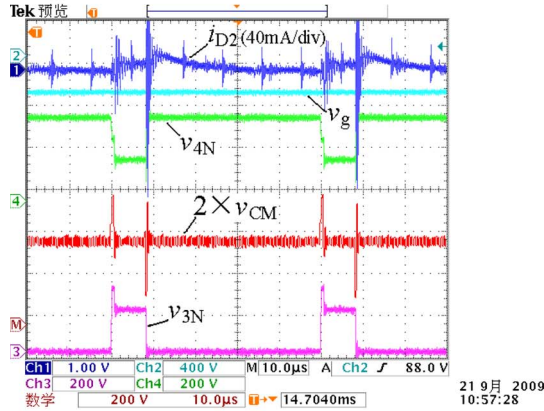

Fig. 13. Common-mode voltage and ground current waveforms in oH5 topology. (a) Common-mode voltage. (b) Ground current.
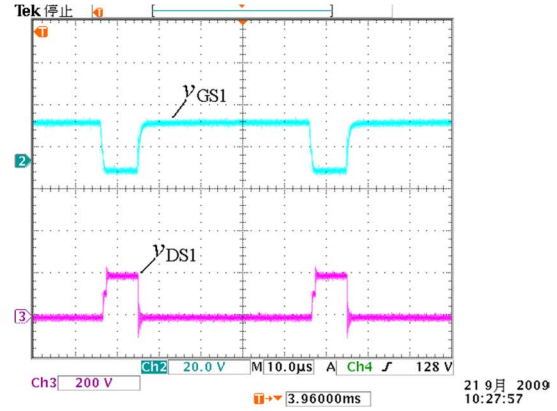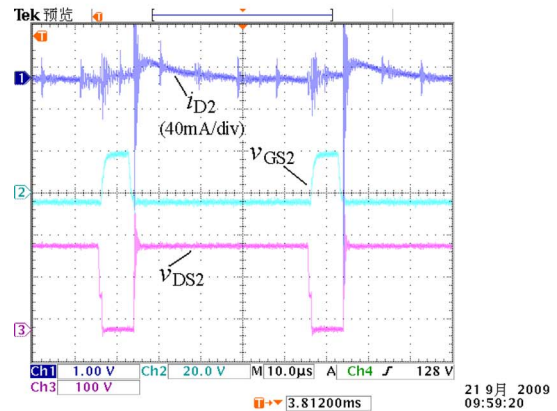
Fig. 14.　Detailed Common-mode voltage waveforms in oH5 topology. (a) At the peak of grid current (v_g: 400 V/div, i_{D2}: 40 mA/div, v_{3N} and v_{4N}: 200 V/div, v_{CM}: 200 V/div, and time: 4 ms/div). (b) At the vale of grid current.

Fig. 16.　Experimental waveform of power device in oH5 topology at $V_{pv} = 400$ V. (a) S_1 (v_{GS1}: 20 V/div and v_{DS1}: 200 V/div). (b) S_2 (i_{D2}: 40 mA/div, v_{GS2}: 20 V/div, and v_{DS2}: 100 V/div).
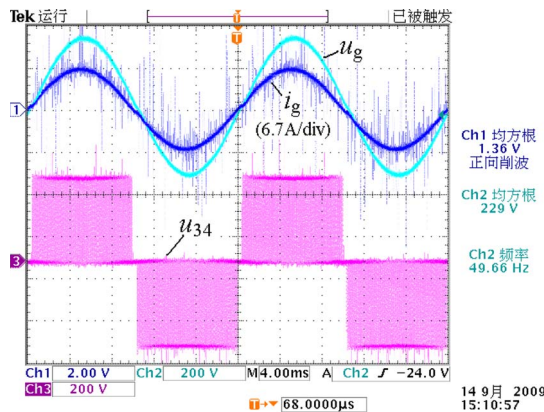

Fig. 15.　Differential-mode voltage waveform in oH5 topology at $V_{pv} = 400$ V (v_g: 200 V/div, i_g: 6.7 A/div, v_{34}: 200 V/div, and time: 4 ms/div).
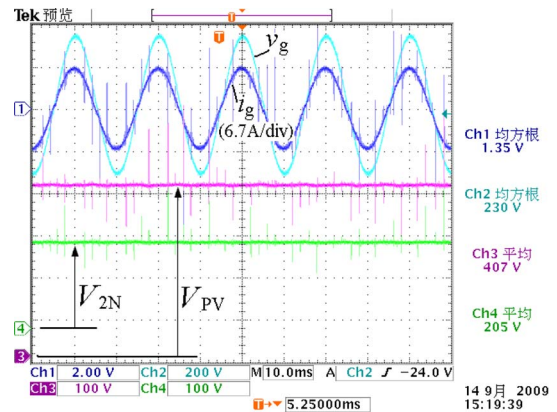

Fig. 17.　Experimental waveform of capacitor divider in oH5 topology at $V_{pv} = 400$ V (v_g: 200 V/div, i_g: 6.7 A/div, v_{pv} and v_{2N}: 100 V/div, and time: 4 ms/div).

VI. CONCLUSION

An optimized transformerless grid-connected PV inverter has been proposed in this paper, which has the following advantages.

1) The common-mode voltage is clamped to a constant level, so the ground current can be suppressed well.
2) The good differential-mode characteristic can be achieved like the unipolar SPWM full-bridge grid-

connected inverter with galvanic isolation, but with higher efficiency.
3) The blocking voltage of the added switches is only half of the input voltage.

These merits are verified and compared by a universal prototype rated at 240 V/50 Hz, 1 kW. It can be concluded that the proposed inverter is extremely suitable for high-power single-phase grid-connected systems with thin-film solar cell.

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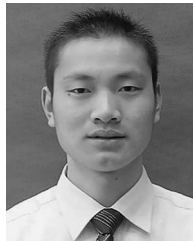
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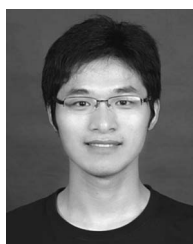
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