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VSC-HVDC Transmission with Cascaded Two-Level Converters

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SUMMARY

The two-level converter valve together with series-connected press-pack insulated-gate bipolar transistors (IGBTs) is a reliable and proven technology for transmission-scale converters. This has been put to use in a further development of high-voltage dc (HVDC) transmission employing voltage-source converters (VSCs). A cascaded two-level (CTL) converter consisting of several smaller two-level building blocks, also called cells, enables the creation of a nearly sinusoidal output voltage from the converter. The development of the CTL is the subject for this paper. Using technology modules developed and refined during the last 15 years, it has been possible to create a converter that addresses and solves many of the limitations of VSC-HVDC transmission while retaining all operational functionality. The technology is scalable up to the highest transmission voltages. Losses are reduced to roughly 1% per converter through a combination of methods. A method for removing the need for external protective equipment and circuitry in the valves is presented. The main control of the converter has been reused, although the control bandwidth, i.e., the speed, has been further improved.

KEYWORDS

High-voltage dc (HVDC), Voltage-source converter (VSC), Multilevel converter, Cascaded two-level (CTL) converter

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1. Introduction

1.1 Background

The first voltage-source converter (VSC)-based high-voltage dc (HVDC) transmission in operation, the Hellsjön–Grängesberg 3-MW test installation, was inaugurated in May 1997. Since then the technology has taken great strides and has arguably become one of two main alternatives for HVDC transmission, the other one being thyristor-based line-commutated converters (LCCs). The main advantages compared to the LCC alternative are smaller converter site size, small filters, possibility to use extruded polymeric cable system, fast active power reversal, and inherent dynamic reactive power support in each converter station.

The smaller station size facilitates easier siting, while the extruded polymeric cable system enables long stretches of land cable installation. The reactive power support capability inherent in the VSC concept enables connections to very weak networks, and even to networks lacking generation, without the need for extra equipment. This is in contrast to the LCC, which requires a certain minimum network strength to ensure stable operation of the ac/dc conversion process.

The largest VSC transmission currently in operation is *Estlink*, between Finland and Estonia, at 350 MW. Two 400-MW systems are currently under commissioning, in Germany (*NordE.On1*) and in the U.S. (*TransBay*). A 500-MW system was recently awarded to connect Ireland and Wales (*East West Interconnector*).

1.2 Limitations of VSC Transmission

High voltages – in the hundreds of kV – are necessary for low-loss high-power transmission. This calls for series connection of a large number of insulated-gate bipolar transistors (IGBTs) when two-level or three-level converters are used, which is challenging. A solution involving press-pack IGBTs with high-speed adaptive gate driving was developed in the mid-1990s; this solution has proven successful in service and under scaled laboratory conditions up to ±320 kV dc [1].

In subsequent stages of development, the switching frequency for two-level HVDC VSCs has been brought down from 2 kHz to about 1 kHz in order to reduce losses. It may be possible to go even further, but this would call for increased filtering, which would partly outweigh the benefits.

One further limitation of VSC technology is the current capability of the IGBT. Today, the largest available IGBT has a maximum turn-off current of 4000 A, effectively giving 1800 A dc transmission.

Multilevel VSC technology without IGBT series connection has been introduced on the market. Although promising in many respects, extra equipment is required in order to safely handle different fault scenarios.

1.3 Outline

This paper is structured as follows. The converter topology, main circuit and principle of operation are described in Section 2. Section 3 describes some important features of CTL valve design. An over-all description of the control system is given in Section 4, and finally some conclusions are offered in Section 5.

2. Converter Topology and Main Circuit

In principle, the CTL converter has a topology similar to that of the modular multilevel converter (MMC) [2]. A different name has been selected to highlight the fact that series-connected press-pack IGBTs are used in the valves, thus extending a technology which successfully has been used for high-voltage two-level VSCs to multilevel VSCs through cascade connection.

Each phase leg of the CTL converter is divided in two arms: positive and negative, which respectively connect the positive and negative poles of the dc bus to the converter's ac bus, see Figure 1. Each arm is built as a cascade of N two-level-converter cells. For a dc-bus voltage level of ±320 kV, N=38 cells per arm are typically required. The cascaded two-level cells in each arm are controlled to provide fundamental-frequency output voltage, related to the desired active- and reactive-power output, through switching of the individual cells, as will be described momentarily.

2.1 Cell Topology and Operating Principle

As seen in Figure 1, each cell consists of a half-bridge two-level converter with two valves, which in turn consist of IGBTs T1 and T2 and diodes D1 and D2. The valves can be switched in three different ways:

- By turning on T2 and turning off T1, the cell is said to be *inserted* and the cell output voltage equals the capacitor voltage. The capacitor then charges when the arm current is positive and discharges otherwise.
- By switching the valves vice versa, i.e., T1 is turned on and T2 is turned off, the cell will give zero output voltage. The capacitor is then *bypassed* and its voltage remains constant.
- If both valves are turned off, the cell becomes *blocked*, and current is conducted only through the diodes. The capacitor will then charge only when the arm current is positive. It will (ideally) not discharge.

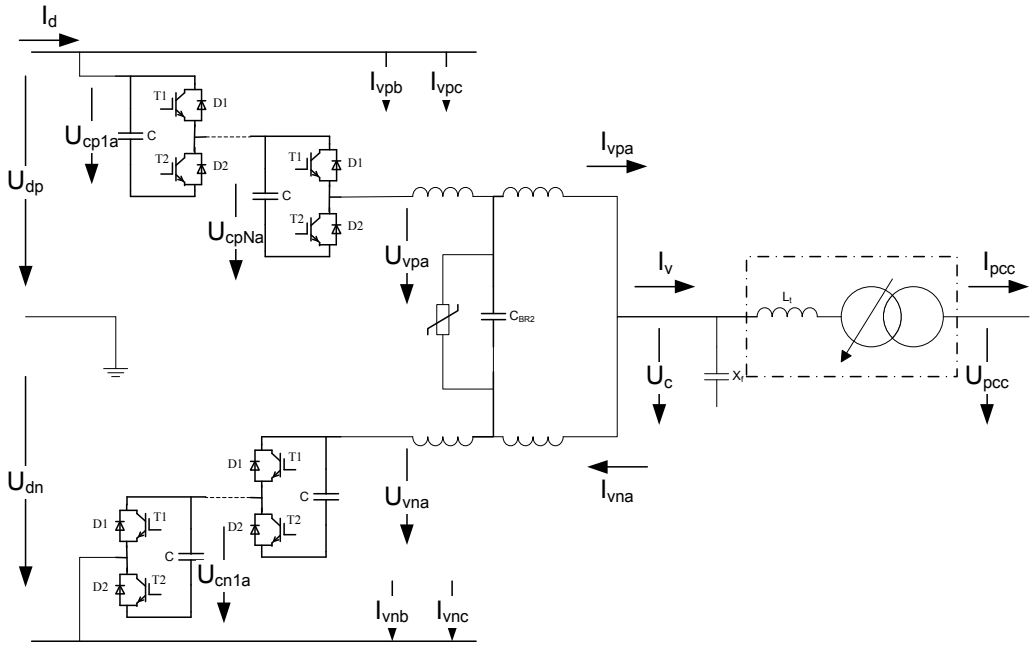

Figure 1: Single-line diagram.

Each cell is switched at a low switching frequency, typically about $f_{swc} = 150$ Hz, i.e., a pulse number about 3 for a fundamental frequency of 50 Hz. During normal operation, the cells are switched in a staggered fashion, as is further described in Section 4. Consequently, the *effective switching frequency per phase leg* becomes $f_{sw} = 2Nf_{swc} = 11.4$ kHz for N=38 cells per arm. This is in the range of 10 times the aforementioned switching frequency of a two-level VSC, which indicates that the dynamic response of a CTL converter is excellent.

Figure 2(a) shows the converter-voltage waveform with less than half the aforementioned voltage range, and consequently only N=17 cells per arm. Added to the sinusoidal modulation reference is a 3rd harmonic for extension of the voltage range to its maximum (this harmonic vanishes in the transformer and does not enter the grid). In the corresponding frequency spectrum in Figure 3(b) it is seen that all harmonic magnitudes (except the added 3rd) are below –40 dB, i.e., 1% of the fundamental.

2.2 Cell Capacitor and Cell-Voltage Ripple

The cell capacitor is a fundamental component of the CTL converter. It is integrated in the valve design, with the main purpose of serving as energy storage. The sum cell voltages of the two arms should each have a mean value of twice the pole-to-neutral dc-bus voltage, this in order to allow converter output voltages with maximum amplitude.

Since the cell capacitor is subjected to a fundamental-frequency current, there will be ripple superimposed on each cell voltage. The cell capacitance is selected as a trade-off between valve voltage requirements and capacitor size. Typically, the total cell capacitance corresponds to a stored energy of

30–40 kJ/MVA (where MVA refers to the converter rating), giving ripple in the range of 10%. The cell-voltage ripples have some interesting properties (with reference to the subplots in Figure 3):

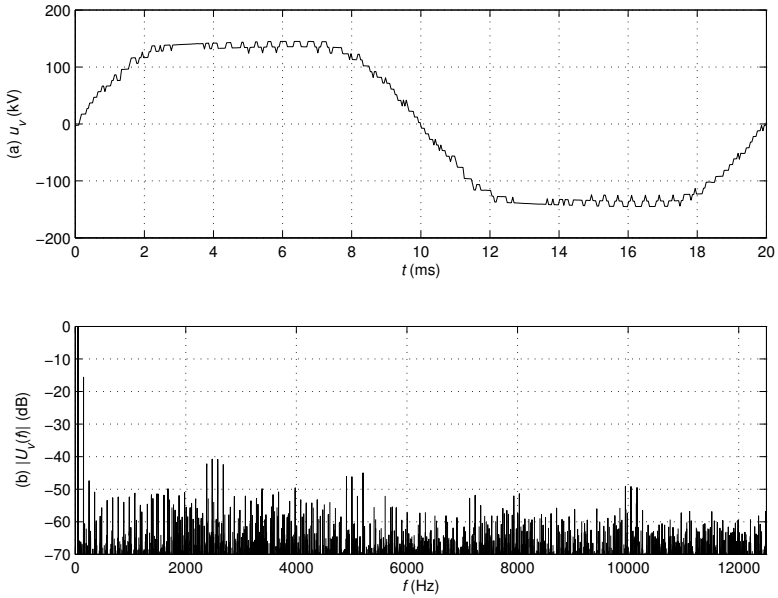

Figure 2: (a) One period of the converter voltage for fundamental frequency 50 Hz, pulse number 3.37, 17 cells/arm, and nominal cell voltage 17.6 kV. (b) Corresponding frequency spectrum.

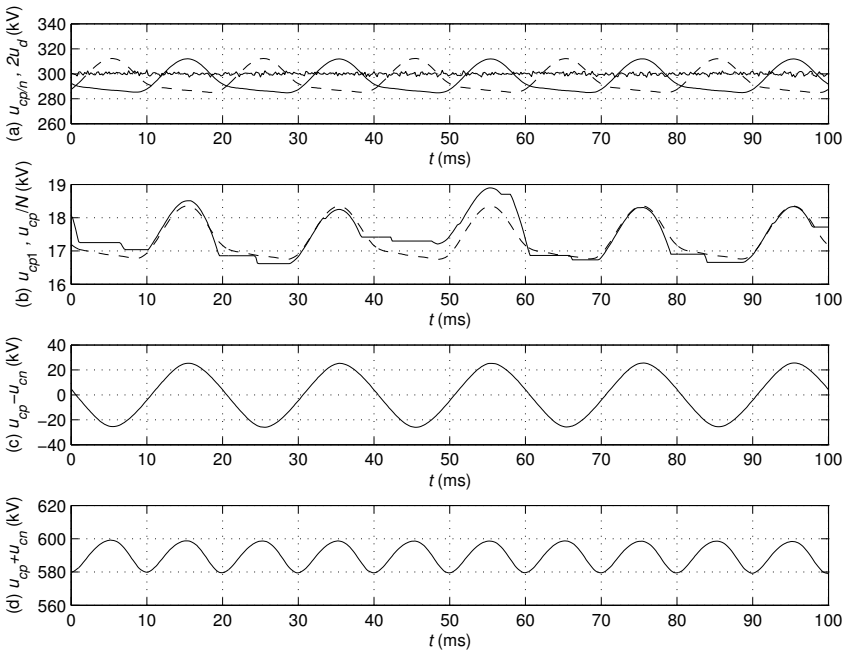

Figure 3: (a) Sum cell voltages for positive (solid) and negative (dashed) arms as well as two times the mean direct voltage (noisy due to switching harmonics). (b) Voltage of cell 1 in the positive arm with the mean cell voltage overlaid (dashed). (c) Differential-mode sum cell voltage. (d) Common-mode sum cell voltage.

(a) The ripples are predominantly of the fundamental and 2nd harmonic frequencies. Characteristic waveforms of the sum cell voltages of both arms are shown. Worth noting is also that dc-bus voltages (the figure shows their mean value) do not exhibit this ripple, because the ripples are positive and negative sequences and thus cancel at the star point on the dc side.

(b) Each individual cell-voltage ripple deviates only slightly from the mean ripple, i.e., 1/*N* of the corresponding sum cell-voltage ripple.

(c) The differential-mode sum cell-voltage ripple is mainly of the fundamental frequency.

(d) The common-mode sum cell-voltage ripple is mainly of 2nd harmonic.

2.3 Reactors and 2nd-Harmonic Filter

As shown in , each arm includes a reactor for the purposes of limiting parasitic currents and fault currents. The reactors are of standard air-core type.

By applying standard circuit laws, it can be shown that the common-mode sum cell voltage drives a circulating current, which closes between the converter phase legs but does not enter the grid. Since the common-mode sum cell voltage has a superimposed 2nd-harmonic ripple, cf. Figure 3(d), a parasitic 2nd-harmonic component tends to appear in the circulating current. If allowed to flow freely, this parasitic component would increase losses and current-rating requirements. Compensation can be made through active control [3], but at a voltage penalty, i.e., the maximum output voltage is reduced somewhat to allow room for control actions. To avoid this penalty, in the CTL converter the 2nd-harmonic component is suppressed using a parallel-resonant filter, realized through a near-center tap of the valve reactors together with a capacitor (C_{BR2}), as shown in .

The grid current of one phase will split evenly between the positive and negative arms. In addition, each arm current will contain a dc component corresponding to 1/3rd of the total dc-side current. Through the sharing of the grid current between the two arms, the corresponding reactive voltage drop will be half compared to a case with a common phase reactor at the point of common coupling (PCC). On the other hand, for a dc-side fault, the reactors are effectively placed in series, and will effectively limit the fault current together with the transformer and grid impedances.

2.4 Filter and Transformer

Thanks to the low harmonic content of the output voltage, see Figure 3, ac filters are normally not required to meet the typical restrictions on harmonic injection into the grid. Only a small capacitor for high-frequency attenuation is included on the converter bus (X_f in). Moreover, due to the low harmonic content, a standard transformer with Y/Y configuration can be used, where the converter-side star point is grounded through an arrester. This configuration will allow reduced voltage rating of the converter as well as efficient over-voltage protection for internal faults.

2.5 PQ Capability

Typical capability of active and reactive power output is shown in Figure 4. The key design parameters defining the power capability are the valve current limit, the direct-voltage and modulation-index limits, as well as the cell-voltage ripple.

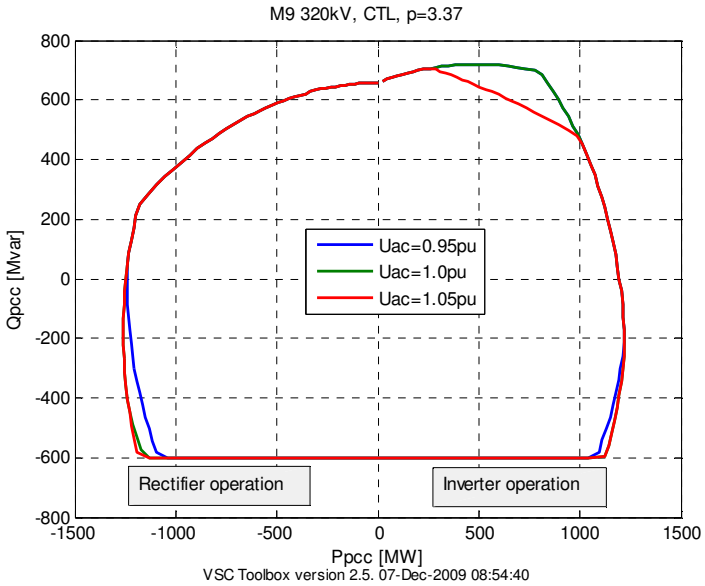

Figure 4: Example of active- and reactive-power capability.

2.6 Losses

Thanks to the usage of a low switching frequency per cell, the IGBT switching losses are significantly reduced compared to a two-level converter, as are the harmonic losses in the reactors. Furthermore, the conduction losses are reduced through use of state-of-the-art 4.5-kV SPT+ IGBT technology. The total converter station losses are in the range of 1%, as shown in the loss overview in Figure 5.

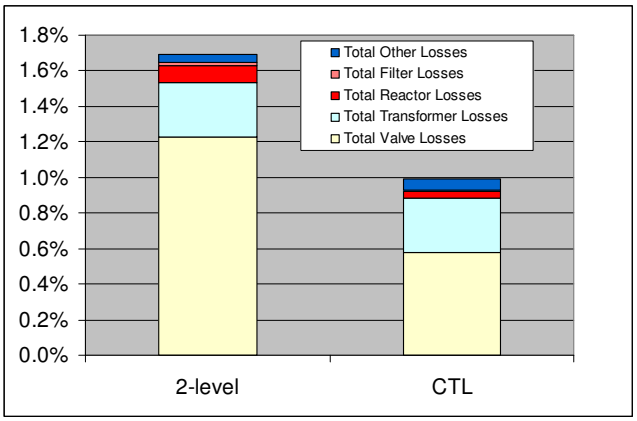

Figure 5: Typical converter losses.

3. Valves

In the CTL converter, the valve becomes the major piece of equipment in terms of complexity, space requirement, cost, and – still – losses. Multilevel converters can be realized in several different ways, with different types of cells with alternative mechanical and electrical solutions. We shall here discuss some aspects of two principal variants of half-bridge cells, namely, with series connection and without. An example of the former is shown in Figure 6.

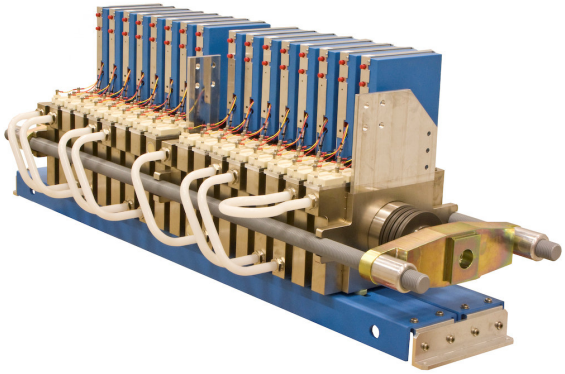

Figure 6: Cell module with two valves, each comprising eight series-connected press-pack IGBTs.

Typically, the highest failure rate of components in any converter valve is found in the power electronics part, including the IGBT and its corresponding driving and communication electronics. Passive components have orders of magnitude better reliability, partly because of lower complexity and partly because higher margins of safety can be applied without adversely affecting the cost of the converter.

Two major fault scenarios that could cause immediate problems for the continued service of the converter, unless well cared for in the design, are cell short circuit and dc pole-to-pole short circuit.

A cell short circuit can happen for a number of reasons, but the general sequence of events is as follows. One of the switches in the cell is conducting current while the other switch blocks the cell capacitor voltage. The insulation of the blocking switch breaks down causing a short circuit of the cell capacitor through the active switches. Typically, the breakdown occurs in one of the semiconductor chips of the IGBT module or on the edge of such a chip. In any case, it generally happens inside the IGBT module. The current derivative of this event is very high, since the cell is designed to have low inductance, in order to minimize switching stresses during normal operation for the IGBTs. Typical values per IGBT are 200-nH commutation inductance and 2-kV blocking voltage, giving a current derivative of 10 kA/µs. The current limit of the conducting IGBT is reached in less than one micro-

second, before any protective action can be taken. Within microseconds, the conducting switch fails because of the uncontrolled overcurrent. Within a few hundred microseconds, faster than any available mechanical protection device, the cell capacitor has discharged its energy, typically 20 kJ, into the fault.

Depending on the type of device used, an IGBT failure may lead to an open circuit. This is the case for industrial standard modules designed for, e.g., the traction and drives markets. Alternatively and much preferable, a stable short circuit is reached, which is the case with press-pack IGBTs designed for electric power-transmission applications. Open circuit in a transmission-class converter must be avoided, as otherwise the resulting arc and its associated energy dissipation will necessitate a trip of the converter every time an IGBT fails. Methods to avoid this have been presented, but the reliability in commercial operation remains to be proven.

In order to safely and securely avoid explosive discharge of the cell capacitor, series connection of devices is introduced also in the multi-level converter. With series connection and press-pack IGBTs, single devices can fail without leading to short circuit or any limitation of operation. When one IGBT fails, the healthy ones in the same switch simply accept the slight voltage increase and transmission continues. Press-pack IGBTs go to a short-circuit failure mode (SCFM), which means that no extra equipment is necessary to prevent arcing in the valve. During the next scheduled maintenance, the faulty IGBT can be replaced. Typical maintenance intervals are 1–2 years.

4. Control System

The control system of the CTL converter consists of two levels:

- an upper level which calculates the per-arm modulation references from various externally set orders[1] and measurements of system variables, and
- a lower level which performs modulation and cell-voltage control at each individual cell.

4.1 Upper-Level Control

The various blocks of the upper-level control are depicted in Figure 7. Brief descriptions of the blocks are given below, with reference to the figure.

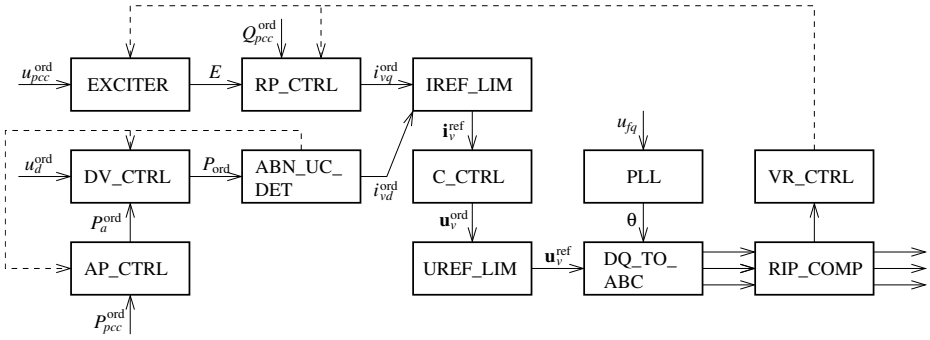

Figure 7: Block diagram of the upper-level control.

The innermost, and fastest, control loop is that for the output current. The current controller (C_CTRL) has as input and output signals the current reference and the voltage order, respectively. Since the effective switching frequency is very high, this loop is very fast, which is important in order to prevent overcurrent in fault situations.

The voltage order is limited in the block UREF_LIM to a reference which is realizable by the pulse-width modulation (PWM).

The upper-level control system operates in a so-called dq reference frame which is aligned with the converter-bus voltage. Synchronization is made by a phase-locked loop (PLL). The alignment has the effect that the d component of the output current becomes active-power producing and the q component reactive-power producing.

The voltage reference is in the block DQ_TO_ABC transformed to the stationary αβ frame using the PLL angle. The αβ-frame vector is then transformed to phase components.

[1] By "order" it is implied an externally set reference signal or an internal unlimited reference signal, whereas "reference" implies a reference signal which is limited to a physically realisable value.

The reference phase voltages are in the block RIP_COMP transformed to modulation references with compensation for the sum cell-voltage ripples. This is needed partly because the differential-mode sum cell voltage has fundamental-frequency ripple, cf. Figure 3(c).

The order for the active-power-producing d-direction current component is set by the direct-voltage controller (DV_CTRL). Both stations in a two-terminal HVDC transmissions use direct-voltage control to allow good fault ride-through capability.

One of the stations also uses an active-power controller (AP_CTRL), whose output is fed to the direct-voltage controller. Under normal operating conditions, the active-power controller adjusts the power transfer to follow its order.

When the maximum average cell voltage taken over all six arms is no longer within a prescribed tolerance band, the active power must be limited to prevent unacceptable over- or undervoltage, which is made in the block ABN_UC_DET.

Reactive power can be controlled directly, by comparing the reactive power at the PCC to its order. This is made by the reactive-power controller (RP_CTRL).

Alternatively, reactive power can be controlled indirectly, through control of the PCC-voltage magnitude. This is made through the emulation of an exciter (block EXCITER) for a synchronous machine, which has the PCC-voltage order as input signal..

The block IREF_LIM limits, if needed, the current order to the current reference, whose modulus does not exceed the maximum permissible current.

Finally, there is a voltage-reduction controller (VR_CTRL) which adds an increment to the exciter input. The purpose of this controller is to reduce the PCC-voltage magnitude when the overmodulation region is entered.

4.2 Lower-Level Control

The blocks of the lower-level control are distributed per arm as well as per cell. Using the modulation references that are fed from the RIP_COMP block of the upper-level control, the lower-level control performs two tasks:

- ***PWM***. The modulation references are compared to a triangular-wave carrier that is individual for each cell. The triangular waveforms are delayed from one cell to the next so that in normal operation, only one cell at a time is switched. When the modulation reference is larger than the carrier, then the cell is inserted; otherwise it is bypassed.
- ***Cell-Voltage Control***. The upper-level control ensures that the sum cell voltages in all arms converge to two times the dc-bus voltage. However, an additional control function is needed to ensure that each cell voltage does not drift away from its individual reference. This task is distributed to each cell, by adding an increment to the modulation reference. This increment – which is small enough not to cause distortion to the converter voltage – is set proportional to the error between the cell-voltage reference and the individual cell voltage. Distribution of the cell-voltage control allows individual cell-voltage references to be used. This in turn allows cells which have faulty positions to be assigned a lower voltage.

5. Conclusions

A robust converter concept with low losses, scalable upwards to any practically useful transmission voltage level, has been presented. An overview of the salient features of its main circuit, valves, and control features was given. The reliability concerns raised by previous versions of multilevel converters were addressed.

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