Impact of Sampling Frequency on Harmonic Distortion for Modular Multilevel Converter

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***Abstract*—This paper applies nearest level control (NLC) to the modular multilevel converter (MMC). Since there are a number of submodules (SMs) in high-voltage applications of MMC and all SM voltages are required to be measured and sorted, if the uniform sampling frequency is not high enough, the SM will not be triggered as quickly as possible. Thus, the converter-output voltage levels and voltage harmonics will be affected. A method to systematically analyze the voltage harmonics is presented, considering the uniform sampling frequency. In order to select a proper sampling frequency, two critical values, which significantly influence the output voltage levels and voltage total harmonic distortions, are calculated. Simulation results based on PSCAD/EMTDC proved the validity of the proposed modulation scheme and the importance of a properly selected sampling frequency.**

***Index Terms*—Harmonics, HVDC, modular multilevel converter (MMC), staircase modulation, uniform sampling frequency, voltage levels.**

I. Introduction

MODULAR multilevel converter (MMC) is an emerging and highly attractive topology for medium-voltage (MV) and high-voltage applications. There are three major multilevel converter topologies [1], [2]: 1) the neutral-point-clamped converter (NPC) [3], 2) flying capacitor converter (FC) [4], and 3) cascaded H-bridge converter (CHB) [5]. The MMC is derived from the CHB topology. However, the main difference between these two types of converters is that MMC uses a half-bridge submodule [SM, Fig. 1(b)], while a CHB uses a full-bridge SM.

MMC was first introduced in [6]. This topology is very suitable for voltage-source converter-based HVDC (VSC-HVDC) applications. Compared with the two-level VSC topology, MMC has three distinctive features as follows.

- The arm inductor is in series with the distributed energy storage capacitors, so the effects of faults arising inside or outside the converter can be reduced substantially by the arm inductor [7].
- Lower switching frequencies (<3 times the fundamental frequency) make the overall converter losses closer to the thyristor technology.
- The output voltage is smooth and nearly ideal sinusoidal, so only small or even no filters are required.

So far, the pulsewidth modulation scheme [5], [8], [9] and space-vector modulation scheme [10], [11] have been applied to MMC. But both schemes may involve high switching frequency, which lead to high switching losses and may not suit very high-power applications.

In order to reduce the switching losses, [12]–[16] presented an active-harmonic-elimination method (AHEM), which is a remarkable improvement of selective harmonic elimination (SHE) method. However, in HVDC transmission applications, the number of SMs of the converter is mainly determined by the dc bus voltage. Therefore, each converter arm consists of a large number of SMs (e.g., Trans Bay Cable Project with HVDC PLUS [7], [17], ±200 kV, 400 MW, about 200 submodules per arm), so the number of corresponding switching angles in SHE is much bigger than the five or seven used in [13]. As a result, a large amount of switching angles (maybe at least 200) needs to be computed and the complexity of the numerical algorithm increases. Besides, [1] considers that SHE-based modulations are limited to open-loop or low-bandwidth applications. Reference [2] mentioned the other two low-switching modulation methods for multilevel converters: nearest vector control (NVC) [18], [19] and nearest level control (NLC) [20]. The NVC and NLC are the same in essence [1] and can be realized online with high dynamic performance. But the implementation of NVC is not as straightforward since a numerical algorithm capable of finding the closest vector needs to be programmed [2]. In comparison, the advantage of the NLC method emerges along with the increase of SM numbers in MMC. Therefore, the NLC method is more simple and suitable for converters with a high number of levels.

This paper adopts nearest level control to the MMC topology with a large number of submodules in the very high power range. Since the number of SMs is considerably large, the quality of converter output waveform is closely related to the uniform sampling frequency. An analytical approach to calculate the harmonics of this particular staircase voltage waveform is presented, with the consideration of uniform sampling frequency. Two critical values of the sampling frequencies, which directly influence the number of output voltage levels and THDs, are calculated. Finally, a time-domain simulation model with 20 SMs per arm is implemented in PSCAD/EMTDC to validate the NLC modulation scheme in MMC and to demonstrate the important effect of the uniform sampling frequency on the output voltage THDs.

II. Basic Structure and Operation Principle of MMC

A. Basic Structure

The basic structure of an MMC is shown in Fig. 1(a). A three-phase MMC consists of six arms, each arm includes a total of n_{SM} submodules and one inductor. Two arms in the same phase comprise a phase unit.

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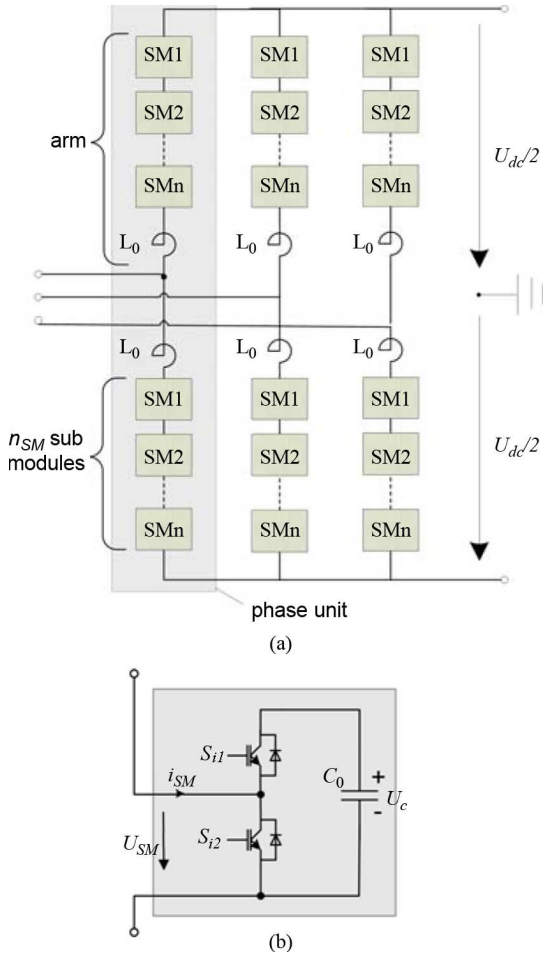

Fig. 1. Basic structure of MMC. (a) Three-phase structure of MMC. (b) Single submodule structure.

Fig. 1(b) is a single SM structure. The SM output voltage $U_{\rm SM}$ only has two values: $U_{\rm SM} = U_c$ when the upper insulated-gate bipolar transistor (IGBT) is switched on and the lower one is switched off; or $U_{\rm SM} = 0$ when the lower IGBT is switched on and the upper one is switched off. This means each SM only has two states in normal operations: switched on or switched off.

In this way, the arm voltage can be handled by controlling the discrete input variable: $n_{\rm on}$, which denotes the total number of on-state SMs in one arm. It is assumed that the voltages of each SM capacitor in the same arm are approximately equal and are kept constant (this can be achieved by the voltage-balancing algorithm described in Section III), then the actual arm voltage u_{ij} can be described as

$$u_{ij} = n_{on\_ij} \cdot U_c \quad (i = p, n;\ j = a, b, c) \tag{1}$$

where the subscript pj denotes the upper arm of phase j while nj denotes the lower arm of phase j.

B. Operation Principle

Fig. 2 is the equivalent circuit of MMC. L_s is the equivalent inductor of the ac system, L_T is the leakage inductor of the converter transformer, L_0 is the series arm inductor, and R_0 denotes

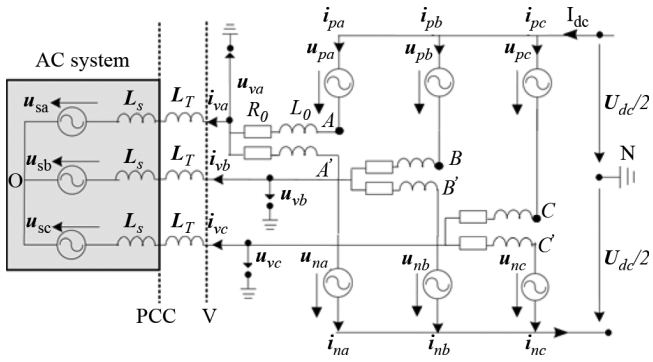

Fig. 2. Equivalent circuit of MMC.

the arm losses. According to [21], the MMC is characterized by the following equation (here, the inner dynamics of MMC are not considered for simplification)

$$u_{vj} = e_j - \frac{R_0}{2} i_{vj} - \frac{L_0}{2} \cdot \frac{di_{vj}}{\rm dt} \quad (j = a, b, c) \tag{2}$$

where u_{vj} is the converter output voltage of phase j at point V, i_{vj} is the line current of phase j at point V, and e_j is the imaginary inner alternating voltage generated in phase j and can be expressed as

$$e_j = \frac{u_{nj} - u_{pj}}{2}. \tag{3}$$

According to (2), if the inner alternating voltage e_j is regarded as the input variable, the converter output voltage u_{vj} and the line current of the ac system i_{vj} can be directly controlled, then the widely used current vector control based on dq coordinates [22], [23] in two-level VSC topology can be adopted to MMC. If the control objectives are the active and reactive power of the point of common coupling (PCC) (Fig. 2), half of the arm inductor value $L_0/2$ should be added to the feedforward part of the inner current loop as $\omega_0(L_T + L_0/2)$.

In order to generate the desired inner alternating voltage e_j (which means (3) should be satisfied), and to keep the dc bus voltage stable at the same time (which means $u_{pj} + u_{nj} = U_{\rm dc}$), it is reasonable to define the reference voltage of the upper and lower arm $u_{pj\_\rm ref}$ $u_{nj\_\rm ref}$ as

$$u_{pj\_\rm ref} = \frac{U_{\rm dc}}{2} - e_j \tag{4}$$

$$u_{nj\_\rm ref} = \frac{U_{\rm dc}}{2} + e_j. \tag{5}$$

The desired inner alternating voltage e_a (taking phase a for example) is assumed to be a sine wave

$$e_a(t) = E_a \sin\omega_0 t = \frac{k}{2} \cdot U_{\rm dc} \cdot \sin\omega_0 t \tag{6}$$

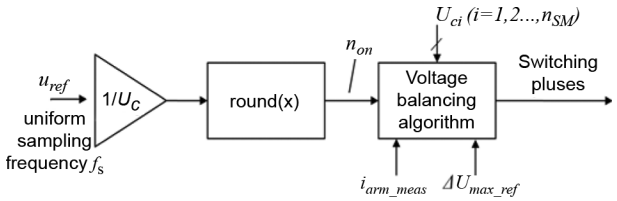

Fig. 3. Control diagram of the NLC method.

where E_a is the peak value of the inner alternating voltage and k is defined in [24] as the amplitude modulation index

$$k = \frac{E_a}{\frac{U_{\rm dc}}{2}}. \tag{7}$$

III. Modulation Scheme and Voltage Balancing

A. Modulation Scheme

The reference voltages of the arm $u_{pj\_\rm ref}$ and $u_{nj\_\rm ref}$ are realized through a specific modulation scheme. There are three low-switching frequency modulation algorithms to be considered for multilevel converters [1], [2]: selective harmonic elimination [12], [13], [25]; nearest vector control [18], [19]; and nearest level control [20]. However, a large amount of switching angles in the SHE method is computed offline and stored in tables, so in the case of HVDC with a high number of submodules, the SHE-based method is relatively complicated. In comparison, the NLC method might be much simpler to facilitate the modulation process. Due to the conceptual and implementation simplicity of the NLC method, the aim is to use it in converters with a high number of levels [2]. And if the number of submodules is large enough, the harmonics amplitudes and voltage THDs could be reduced to a low range.

The control diagram of the NLC method is depicted in Fig. 3. It is important to mention that in digital-signal-processing systems, the uniform sampling frequency f_s of the reference voltage $u_{\rm ref}$ must be taken into account, because when the number of SMs to be controlled is very large, the required sampling frequency f_s in the uniform sampling method should be high enough to make sure that all of the SMs can form the voltage levels as much as possible [Fig. 4(a), each SM generates one voltage level, so each voltage step is U_c]. Otherwise, if the sampling frequency is low, the voltage step will increase [see Fig. 4(b), the first and third voltage steps are $2U_c$]. According to Fig. 4, the voltage reference $u_{\rm ref}$ is not a smooth sine wave. Actually, it is a staircase waveform with the sampling interval $T_s = 1/f_s$ (blue line in Fig. 4). After the sampled reference voltage $u_{\rm ref}$ is obtained, it is divided by the value of the capacitor voltage U_c to find the closest voltage level (here, U_c is considered to be a constant). Now the problem is reduced to decide how many SMs should be switched on. This is performed using the function $\mathrm{round}(x)$. The function returns the nearest integer of the input number (e.g., $\mathrm{round}(3.4) = 3$, $\mathrm{round}(3.6) = 4$). Thus, the total number of SMs to be switched on $n_{\rm on}$ is derived in each arm.

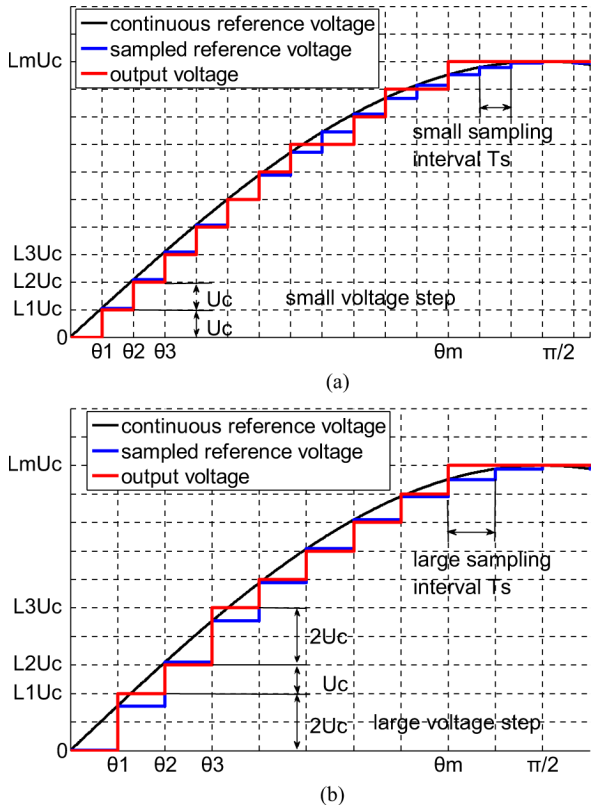

Fig. 4. Output voltage of the NLC method with a different sampling frequency. (a) Small sampling interval. (b) Large sampling interval.

B. Voltage Balancing

Then, the voltage balancing algorithm is applied to distribute the arm energy among each SM equally. The generation of switching pulses is based on fast monitoring the voltages of each SM capacitor U_{ci}, $(i = 1,2,\ldots,n_{\rm SM})$ and the direction of arm current $i_{arm\_\rm meas}$. The principles of the balancing algorithm are as follows [26].

- When the arm current charges the capacitors, the submodules with the lowest storage capacitor voltages will be switched on to form the desired arm voltage.
- When the arm current discharges the capacitors, the submodules with the highest storage capacitor voltages will be switched on to form the desired arm voltage.

In order to choose the SM with the highest or lowest voltage, this balancing algorithm needs to sort the SM voltages in one arm. To avoid unnecessary switching operations, a predefined SM voltage deviation band $\Delta U_{\max\_\rm ref}$ is used. If the actual maximum SM voltage difference $\Delta U_{\max}$ exceeds this predefined value

$$\Delta U_{\max} = U_{c\_\max} - U_{c\_\min} > \Delta U_{\max\_\rm ref} \tag{8}$$

where $U_{c\_\max}$ and $U_{c\_\min}$ denote the maximum and minimum SM voltages at a certain instant in one arm, respectively. Then the aforementioned balancing algorithm will be performed.

Otherwise, if (8) is not satisfied, the switching principles are as follows.

- If extra SMs need to be switched on during the following control cycle (i.e., $\Delta n_{\rm on}$ is positive), no switching is applied to those SMs currently in on-state. The conventional balancing algorithm mentioned before will only be applied to those SMs currently in off–state.
- If some SMs that are currently in on-state need to be switched off during the following control cycle (i.e., $\Delta n_{\rm on}$ is negative), no additional SMs that are currently in off-state will be switched on. The conventional balancing algorithm mentioned before will only be applied to the SMs currently in on-state.

Based on the voltage balancing algorithm and the switching pulses generation principles from before, the number of switching operations and the total losses of the converter can be reduced significantly.

IV. Harmonics Analysis

To calculate the harmonics of the staircase output voltage, we should assume that the voltage of each SM capacitor U_c is kept constant. Then, Fourier series expansion is used. The theoretical method to analyze the harmonics of the staircase waveform has been reported in [27]. But the result is based on an infinite sampling frequency for the reference voltage. In other words, each SM corresponds to one voltage level. If every voltage level is equal, the staircase output voltage can be expressed as [27]

$$v_{\rm output} = \frac{4U_c}{\pi} \sum_{h=1,3,5}^{\infty} \left[\frac{1}{h} \cdot \sum_{i=1}^{m} \cos(h\theta_i) \cdot \sin(h\omega_0 t) \right] \quad (9)$$

where θ_i $(1 \le i \le m)$ is the ith switching angle (Fig. 4). m is the total number of voltage levels in a quarter period of time and h is the harmonic order.

But as shown in Figs. 4(b) and 5(a), if the voltage levels are unequal, (9) is not suitable.

In this case, the sampling frequency f_s must be considered because the actual sampling frequency in the digital control system cannot be infinite. As a result, a single output voltage level may contain more than one SM capacitor voltage U_c, especially when $n_{\rm SM}$ is large and f_s is not high enough [Fig. 4(b)].

To analyze the waveform in Fig. 4, the following assumptions should be made:

- the waveform is odd and half-wave symmetry, so there are not any even-order harmonics;
- amplitude modulation index $k \le 1$.

Based on (4) and (5), and neglecting the dc component $U_{\rm dc}/2$, the sampled reference voltage can be expressed as

$$u_{\rm ref}(t) = \frac{k}{2} U_{\rm dc} \sin(\omega_0 t) = U_{\rm ref} \sin(\omega_0 n T_s) \quad \left(0 \le n \le \frac{\frac{\pi}{2}}{\omega_0 T_s} = \frac{f_s}{4f_0},\ n = 0,1,2,3,\ldots\right) \quad (10)$$

where $U_{\rm ref}$ is the peak value of $u_{\rm ref}$, n is a discrete variable, ω_0 is the radian fundamental frequency, and $T_s = 1/f_s$ is the sampling interval as shown in Fig. 4.

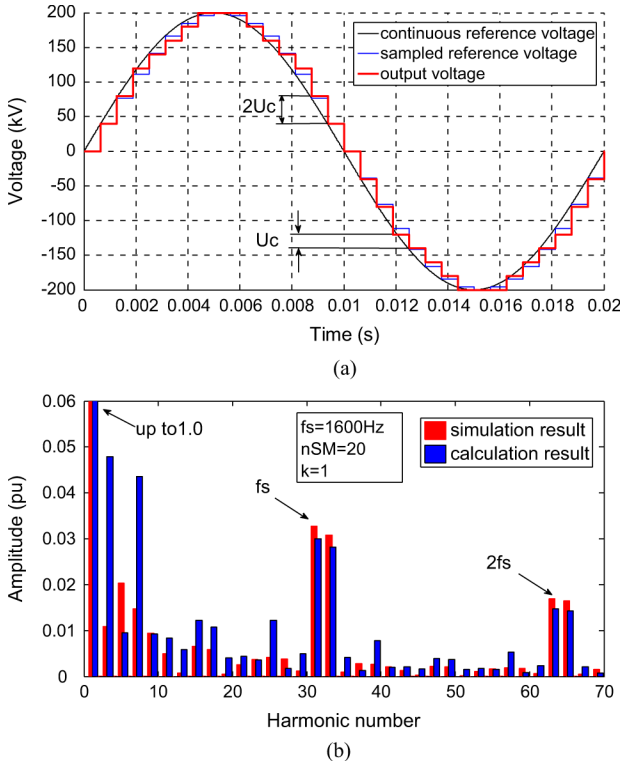

Fig. 5. Output voltage with the NLC method and voltage spectrum. (a) Voltage waveform with uniform sampling. (b) Simulated and calculated spectrum.

At a given sampling interval T_s, in order to find all of the switching angles θ_i in Fig. 4, define

$$\Delta L = \text{round}\{U_{\rm ref} \sin(\omega_0 n T_s)\} - \text{round}\{U_{\rm ref} \sin[\omega_0 (n-1) T_s]\} \quad (11)$$

which means the voltage step $U_{\rm step}$ contains a number of ΔL submodule voltages U_c ($U_{\rm step} = \Delta L \cdot U_c$) at the nth sampling interval.

Then, for different values of n, the corresponding switching angle θ_i can be acquired

$$\begin{cases} \theta_i \text{ does not exist} & (\text{if } \Delta L = 0) \\ \theta_i = \omega_0 n T_s & (\text{if } \Delta L \ge 1). \end{cases} \quad (12)$$

So the Fourier series expansion of the output voltage is given by

$$v_{\rm output} = \frac{4U_c}{\pi} \sum_{h=1,3,5}^{\infty} \frac{1}{h} \cdot \left[\sum_{i=1}^{m} (L_i - L_{i-1}) \cos(h\theta_i) \right] \cdot \sin(h\omega_0 t) \quad (L_0 = 0) \quad (13)$$

where θ_i $(1 \le i \le m)$ is the ith switching angle in a quarter fundamental period, which is calculated by (12); L_i $(1 \le i \le m)$ is the corresponding number of on-state SMs at θ_i, so $L_i U_c$

is the corresponding voltage level (Fig. 4); and h is the harmonic order.

Fig. 5 is the staircase output voltage and the corresponding spectrum simulated and calculated. The simulation result is based on numerical fast Fourier transform (FFT) analysis, while the calculation result is based on (13). The simulation result shows a close agreement with the calculation. Note that there are two sidebands at $f_s = 1600$ Hz $(h = 32)$ and $2f_s = 3200$ Hz $(h = 64)$, respectively. This result demonstrates that the sampling frequency in the NLC method has a similar effect of the carrier frequency in the PWM modulation scheme.

V. Voltage-Quality Evaluation

First, we must distinguish two concepts:

$n_{\rm SM}$: the number of submodules per arm; it is determined by the dc bus voltage $U_{\rm dc}$ and the steady-state capacitor voltage U_c as $n_{\rm SM} = U_{\rm dc}/U_c$.

$n_{\rm level}$: the number of output voltage levels, which directly affects the waveform quality.

If $n_{\rm SM}$ is small (5 or 7 etc.), the $n_{\rm level}$ can be directly calculated as

$$n_{level} = n_{\rm SM} + 1. \tag{14}$$

But when MMC is extended to a very high voltage range, the number of cascaded SMs is considerably large (e.g., 200 per arm in the Trans Bay Cable Project [17]). So the effect of sampling frequency should be considered, and (14) is no longer correct. In this case, $n_{\rm level}$ is determined by three major factors:

1) the sampling frequency f_s (as shown in Fig. 4);
2) the number of submodules $n_{\rm SM}$;
3) the amplitude modulation index k.

A. Impact of Sampling Frequency f_s

Fig. 6 shows the relationship between the number of output voltage levels $n_{\rm level}$ and the sampling frequency f_s given $n_{\rm SM} = 20$ and $k = 1$. It is concluded that the voltage levels $n_{\rm level}$ and then the total harmonic distortions (THD) are determined by the sampling frequency f_s, if $n_{\rm SM}$ and k are supposed to be constant. From Fig. 6, there are two critical values of the sampling frequency:

f_1: the lower limit of f_s, when $f_s < f_1$, $n_{\rm level}$ will decrease significantly and be linear with f_s;

f_2: the upper limit of f_s, when $f_s > f_2$, $n_{\rm level}$ will keep constant and every SM will compose a voltage level.

In conclusion, the relationship between $n_{\rm level}$ and f_s is

$$n_{\rm level} = \begin{cases} \frac{f_s}{2\cdot f_0} + 1 & (f_s < f_1) \\ n_{\rm SM} + 1 & (f_s > f_2) \end{cases} \tag{15}$$

where f_0 is the fundamental frequency. It is important that when $f_s < f_1$, $n_{\rm level}$ just completely depends on f_s and is not influenced by $n_{\rm SM}$.

These two critical values f_1, f_2 serve as the useful indicators when selecting the sampling frequency of the controller f_s. It is shown that the amplitudes of harmonics will increase rapidly with the decrease of f_s, in the condition of $f_s < f_1$. Certainly, it is unnecessary to choose $f_s > f_2$ from the viewpoint of reducing voltage harmonics, because in this frequency range, all of the SMs are fully utilized and rising sampling frequency will not lead to a remarkable reduction of the voltage THD.

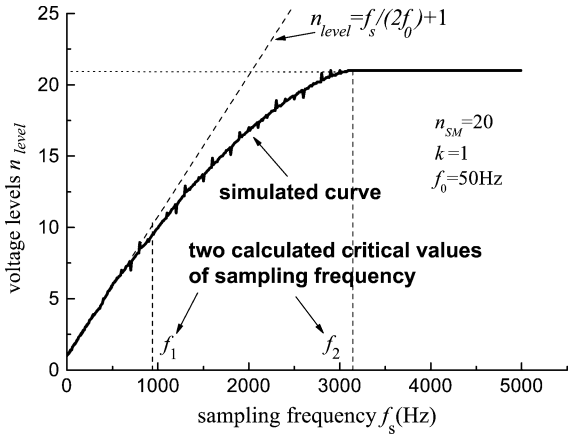

Fig. 6. Voltage level number as a function of the uniform sampling frequency.

To calculate the two critical values of the sampling frequency f_1, f_2 shown in Fig. 6, a sinusoidal voltage output waveform described in (10) is considered. In one sampling interval T_s, the change of the reference voltage is

$$\begin{aligned} du_{\rm ref} &= \frac{k}{2} U_{\rm dc} \cdot \omega_0 \cdot \cos(\omega_0 t) \cdot dt \\ &= \frac{k}{2} U_{\rm dc} \cdot \omega_0 \cdot \cos(\omega_0 t) \cdot T_s \\ &= k U_{\rm dc} \cdot \pi \frac{f_0}{f_s} \cdot \cos(\omega_0 t). \end{aligned} \tag{16}$$

The lower critical value f_1 means that the minimum voltage change during one sampling interval T_s is just equal to a single capacitor voltage U_c. This occurs at the flattest point of a sine wave ($\omega_0 t = \pi/2$; here, we use $\omega_0 t = \pi/2 - \omega_0 T_s$ as an approximation for the convenience of calculation)

$$du_{\rm ref}|_{\rm min} = k U_{\rm dc} \cdot \pi \frac{f_0}{f_s} \cdot \cos(\omega_0 {\rm t})|_{\omega_0 t = \pi/2 - \omega_0 T_s} = U_c \tag{17}$$

$$\Rightarrow k \cdot n_{\rm SM} \cdot \pi \cdot \frac{f_0}{f_s} \sin \frac{2\pi \cdot f_0}{f_s} = 1. \tag{18}$$

If we suppose $f_s \gg 2\pi \cdot f_0$, the above equation can be simplified as

$$2k \cdot n_{\rm SM} \cdot \frac{\pi^2 \cdot f_0^2}{f_s^2} = 1 \Rightarrow f_1 = \pi \cdot f_0 \cdot \sqrt{2k \cdot n_{\rm SM}}. \tag{19}$$

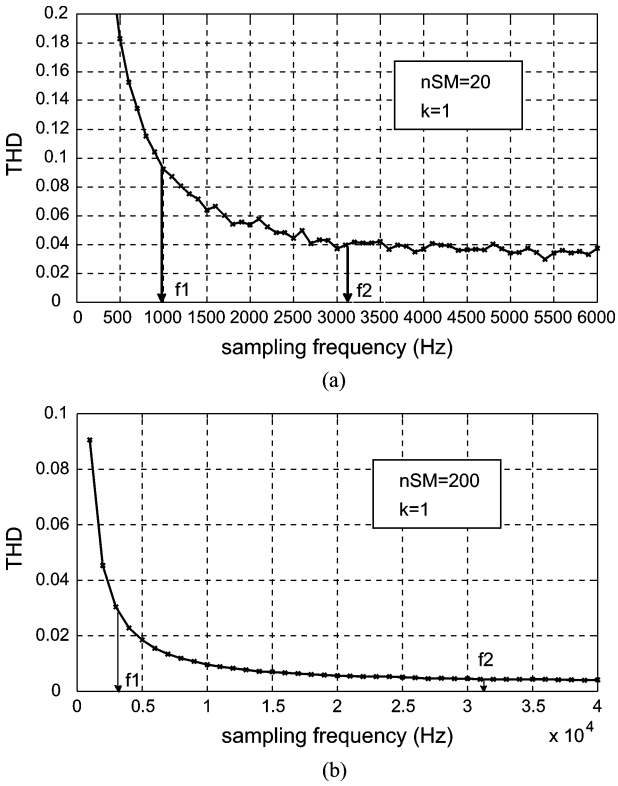

Fig. 7. THD of the line-to-line voltage as a function of sampling frequency. (a) $n_{\rm SM} = 20$. (b) $n_{\rm SM} = 200$.

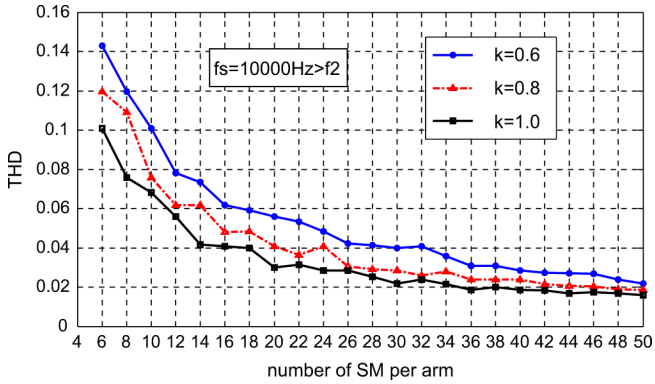

Fig. 8. THD of the line-to-line output voltage as a function of $n_{\rm SM}$.

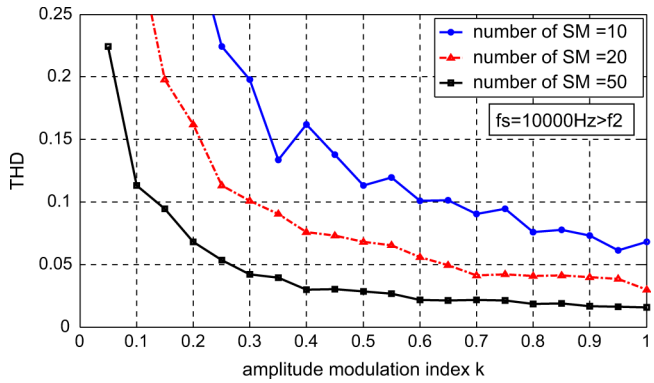

Fig. 9. THD of the line-to-line output voltage as a function of k.

Similarly, if we set $\omega_0 t = 0$, the upper critical value of the sampling frequency f_2, which means every SM is utilized to form a voltage level, can be calculated as

$$du_{\rm ref}|_{\max} = kU_{\rm dc} \cdot \pi \frac{f_0}{f_s} \cdot \cos(\omega_0 t)|_{\omega_0 t=0} = U_c \quad (20)$$

$$\Rightarrow f_2 = \pi \cdot f_0 \cdot k \cdot n_{\rm SM}. \quad (21)$$

For example, if $n_{\rm SM} = 20$, $k = 1$, $f_0 = 50$ Hz, then the two critical values f_1, f_2 can be calculated by using (19) and (21): $f_1 = 993$ Hz and $f_2 = 3142$ Hz, which is very close to the simulated results as shown in Fig. 6.

To evaluate the output voltage quality, the total harmonic distortion (THD)

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} v_{l-l,n}}}{v_{l-l,1}} \quad (22)$$

can be used. The relationship between the line-to-line voltage THD and the sampling frequency is depicted in Fig. 7. It shows a saturation characteristic similar to the one in Fig. 6. Obviously, there is a linear relationship between the voltage THD and the sampling frequency f_s when $f_s < f_1$. We can conclude that when f_s is beyond the upper critical value f_2, the voltage THD decreases slowly, compared to the frequencies lower than f_2. This is very helpful in choosing a proper sampling frequency to make the voltage THD under an acceptable tolerance.

B. Impact of Submodule Numbers $n_{\rm SM}$

The number of SMs per arm $n_{\rm SM}$ is determined by the dc bus voltage and the voltage rating of a single IGBT module ($n_{\rm SM} = U_{\rm dc}/U_c$). The quantity of $n_{\rm SM}$ also influences the THD of the output voltage. In fact, the value of $n_{\rm SM}$ implies the possible maximum output voltage levels, as shown in Fig. 6 when f_s exceeds the upper critical value f_2. To evaluate the influence of $n_{\rm SM}$ on output voltage THD, f_s should be larger than f_2 to eliminate the effect of the sampling frequency. Fig. 8 is the line-to-line output voltage THD with different $n_{\rm SM}$ values. Note that the sampling frequency $f_s = 10000$ Hz $> f_2$ [here, $k = 1$, $f_0 = 50$ Hz, $n_{\rm SM} = 50$, so $f_2 = 7854$ Hz according to (21)].

C. Impact of the Amplitude-Modulation Index k

The relationship between the line-to-line output voltage THD and the amplitude-modulation index k, which is defined in (7), is shown in Fig. 9.

It shows that the voltage THD increases significantly when $k < 0.5$, although the value of $n_{\rm SM}$ comes up to 50. This is because when k decreases, the effective quantity of SMs utilized to form the output voltage levels reduces. Consequently, the amplitude-modulation index should not be set to a small value when the converter is in normal operation. In other words, low amplitude of the ac output voltages generated by the converter is not acceptable.

TABLE I
MAIN CIRCUIT PARAMETERS OF THE MMC MODEL

Items	Values	Comments
Active power P	40MW	1.0pu
AC system voltage U_s	10kV	
AC system inductance L_s	1.58mH	SCR=5at PCC
Transformer ratio	10kV/23kV	Y_0/Δ
Transformer leakage inductance L_T	4.21mH(secondary side)	0.1pu
Number of SMs per arm n_{SM}	20	
SM capacitor voltage U_c	2kV	
SM capacitance C_0	0.013F	
Arm inductance L_0	4mH	0.095pu
dc bus voltage U_{dc}	±20kV	1.0pu
Modulation index k	0.9	
Voltage deviation band $\Delta U_{max\ ref}$	0.05kV	2.5%U_c
Sampling frequency f_s	4000Hz	

VI. PSCAD/EMTDC SIMULATION RESULTS

To verify the proposed modulation method and to evaluate the corresponding output voltage quality, a detailed model based on the time-domain simulation tool PSCAD/EMTDC is developed. System configurations are the same as Figs. 1 and 2. The simulation parameters are shown in Table I. The SM capacitor steady-state voltage U_c is set to 2 kV, which means the well-proven standard IGBT component can be used. In order to enhance the simulating efficiency, the number of SMs per arm is set to 20.

Simulated waveforms of two cycles at the steady-state condition are depicted in Fig. 10. The line-to-line output voltage at point $V u_{va,L\_L}$, u_{vb,L_L}, u_{vc,L_L} [Fig. 10(a)] is sinusoidal. Compared with the two-level VSC topology, the line currents [Fig. 10(b)] are very smooth without the installation of filters. Unfortunately, the arm currents [Fig. 10(c)] contain a double-frequency component at 100 Hz [24], so they are not sinusoidal. This undesired component can be reduced by increasing the value of arm inductors and by applying advanced controls. The distortion of arm currents does not affect the converter output characteristics at the ac side. Fig. 10(d) is the upper and lower arm voltages in phase a. The number of voltage levels is less than $n_{\mathrm{SM}}+1=21$ because the modulation index $k=0.9<1$. Fig. 10(e) is the voltages of 20 SM capacitors in phase a. The capacitor voltages are controlled by the voltage balancing algorithm proposed in Section III. The maximum voltage deviation among each SM in one arm is about 0.05 kV, which is consistent with the predefined value $\Delta U_{\max\_\mathrm{ref}}$. The total voltage ripple of a single capacitor is kept within an acceptable range (about ±5%).

Furthermore, different values of the sampling frequency f_s are simulated. The THD of the line-to-line output voltage at point V is shown in Fig. 11. Obviously, f_s plays an important role in the determination of output voltage THD. The results are compared in two cases.

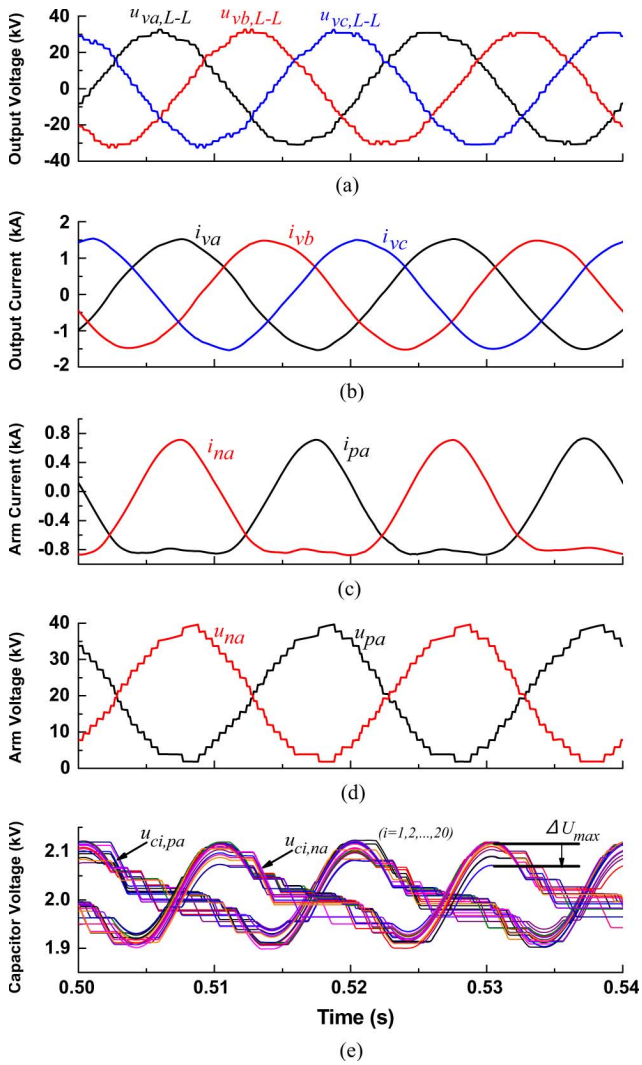

Fig. 10. Simulated waveforms in steady state. (a) Line-line voltages at point V. (b) Line currents at point V. (c) Arm currents of phase a. (d) Arm voltages of phase a. (e) SM capacitors' voltages.

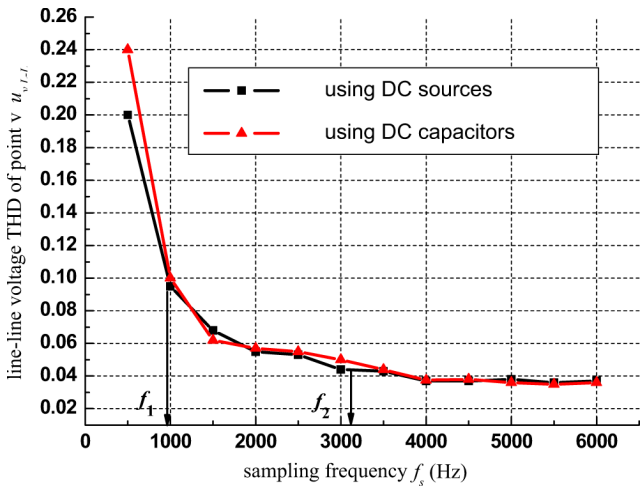

Fig. 11. Simulated THD with dc sources and dc capacitors.

Case 1) The SM capacitor voltages are kept constant (using dc voltage sources).

TABLE II
SWITCHING FREQUENCY WITH A DIFFERENT VOLTAGE DEVIATION BAND

maximum SM voltage difference ΔU_{max_ref} (kV)	0.01	0.05	0.1
Device switching frequency f_{eq_NLC} (Hz)	518	228	178

Case 2) The SM capacitor voltages are variable (using dc capacitors in Table I).

Simulation results of THD show little differences in two cases, especially when the sampling frequency is higher. This demonstrates that the harmonic analysis method described in Sections IV and V is correct by assuming a constant capacitor voltage U_c.

VII. COMPARISONS OF DEVICE SWITCHING FREQUENCY

To demonstrate the low-switching character of the NLC method with voltage balancing, the comparison of the switching frequency is made with different values of voltage deviation band $\Delta U_{\max\_\mathrm{ref}}$. Since each IGBT is not switched at a constant frequency in the NLC method, so the switching numbers per second of the IGBT is counted in PSCAD/EMTDC, and the average device switching frequency f_{eq-NLC} of a single IGBT is calculated. The results are listed in Table II, with different values of $\Delta U_{\max\_\mathrm{ref}}$, which is defined in (8). Table II shows that the NLC method used in MMC can reduce the average device switching frequency significantly.

VIII. CONCLUSION

In this paper, the nearest level control method for MMC with a large number of submodules is presented and validated. The harmonics of the converter output voltages are analyzed by theoretical calculations and dynamic simulations. Both of the results point out that the uniform sampling frequency of the reference voltage has a significant effect on the output voltage levels and THDs in MMC topology with the NLC modulation. Two critical values of the sampling frequency, which influence the voltage levels, are calculated. They are useful indicators when selecting a proper sampling frequency for the controller in the preliminary design stage of MMC.

The impacts of the number of submodules per arm and the amplitude-modulation index are also studied. They are the other two factors to determine the voltage THDs.

The detailed PSCAD/EMTDC model proved the validity of the investigation. Simulation results demonstrated the importance of the sampling frequency to determine the output voltage levels and THDs.

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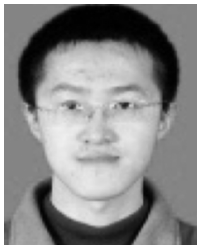

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